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# Low RF losses up to 110 GHz in GaN-on-silicon HEMTs

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## Abstract

We report on low RF losses at the interface between the epitaxial structure and the silicon substrate (less than 0.8 dB/mm up to 110GHz) of AlN/GaN high electron mobility transistors (HEMTs) grown on silicon substrate. This state-of-the-art performance makes GaN-on-Silicon HEMTs competitive with GaN-on-SiC in terms of parasitic RF losses. Furthermore, a maximum dc output current close to 1 A/mm together with low leakage current of 1  $\mu$ A/mm and low trapping effects are achieved while using a short gate length of 0.2  $\mu$ m. The large signal measurements confirmed the high quality of the epitaxy and the device processing as well as the low parasitic RF losses. This is reflected by a high output power density of 4.5 W/mm achieved at 18 GHz.

## Introduction

Owing to its outstanding properties, GaN-based High Electron Mobility Transistors (HEMTs) are a promising candidate for high frequency high power applications. For high frequency applications, GaN is generally grown on SiC substrate not only because of its high thermal conductivity but also due to the resulting low RF losses (less than 0.5 dB/mm up to 100 GHz). However, SiC substrates are expensive. Therefore, for applications requiring low cost devices, the silicon (Si) substrate could be an attractive solution.

Compared to SiC substrate, the parasitic RF losses are generally much higher (it can easily reach several dB/mm) when using Si substrate. This is mainly due to the intermixing between the nucleation layer and the Si substrate resulting in the presence of a conductive layer at the interface [1] and consequently a significant capacitance under RF conditions. The parasitic capacitance degrades the output power performance of the device and considerably affect the circuit design and modelling. Improvement of the RF losses on Si substrate is therefore a challenge in order to achieve low cost devices operating at high frequency with high output power. In this work, a double heterostructure (DHFET) grown on Si substrate is studied. Low RF losses close to GaN-on-SiC values are shown up to 110 GHz; which allowed reaching high output power density well above 4 W/mm at 18 GHz.

## Results and discussion

200 nm gate length AlN/GaN DHFET devices capped with in-situ SiN and grown on highly resistive silicon substrate (111) by the company EPIGAN have been fabricated and studied. More details about processing can be found in [2,3].

DC measurements have been carried out using a Keysight A2902A static modular source and monitor. A current density of 0.9 A/mm is obtained at  $V_{DS} = 10$  V and  $V_{GS} = +2$  V (Fig.1.). Moreover, a negligible threshold voltage shift as a function of  $V_{DS}$  is observed on the transfer characteristics confirming a good electron confinement. An excellent device pinch-off is obtained with a very low off-state leakage current below 1  $\mu$ A/mm. The low leakage current is maintained up to high voltage with a resulting breakdown voltage around 100 V (see Fig. 2) at  $V_{GS} = -5$  V.

The maximum transconductance  $G_m$  is around 300 mS/mm at  $V_{DS} = 10$  V and  $V_{GS} = -1$  V. At these biases, the cut-off frequency ( $f_T$ ) and maximum frequency oscillation values ( $f_{max}$ )

extracted from the scattering (S) parameters are about 40 GHz and 110 GHz, respectively. The S parameter measurements have been performed with a Rhode and Schwarz ZVA67GHz.

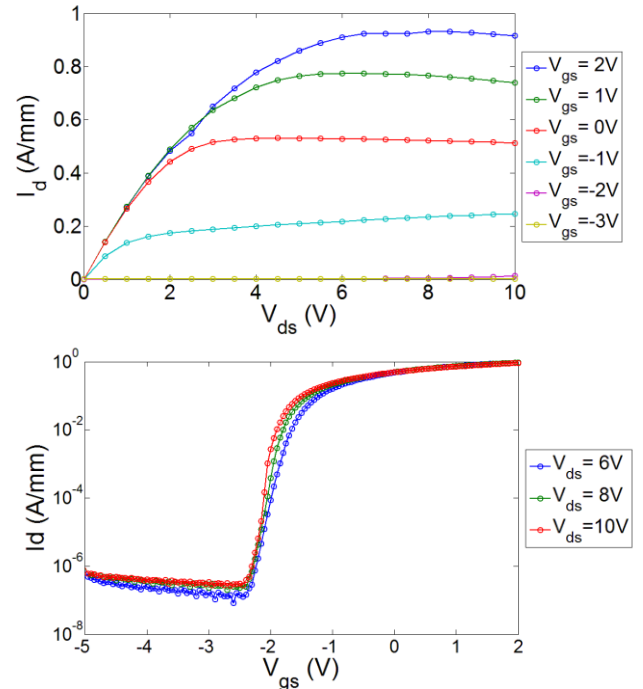


Figure 1. Typical DC output and transfer characteristics of an AlN/GaN DHFET.

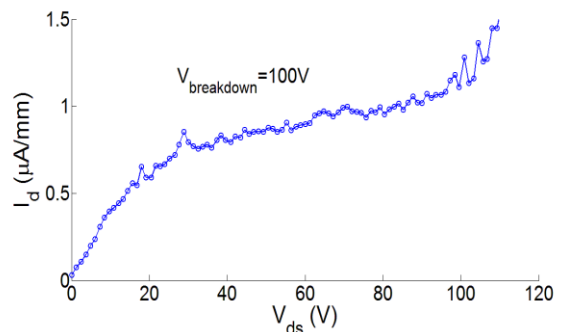
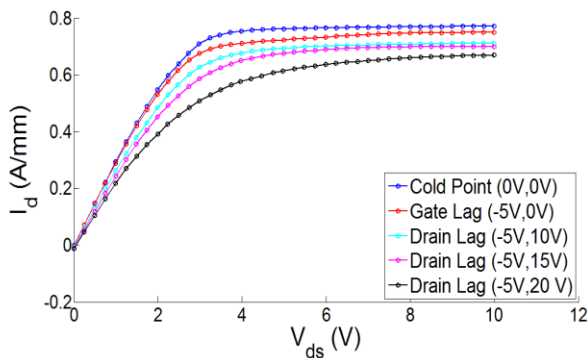


Figure 2. Off-state characteristic at  $V_{GS} = -5$  V of an AlN/GaN DHFET

Pulsed measurements using a pulse duration of 500 ns and a duty cycle of 5% have been achieved at various quiescent bias points in order to highlight the trapping effects. The “cold” polarization is used as a reference ( $V_{GS}=0$ V,  $V_{DS}=0$ V). The second quiescent bias point ( $V_{GS}=\text{pinch-off voltage}$ ,  $V_{DS}=0$ ) emphasizes the gate lag effect while ( $V_{GS}=\text{pinch-off voltage}$ ,  $V_{DS}=10$ V, 15V, and 20V) reveal the drain lag effects. The measurement are performed at open channel ( $V_{GS} = +1$ V).

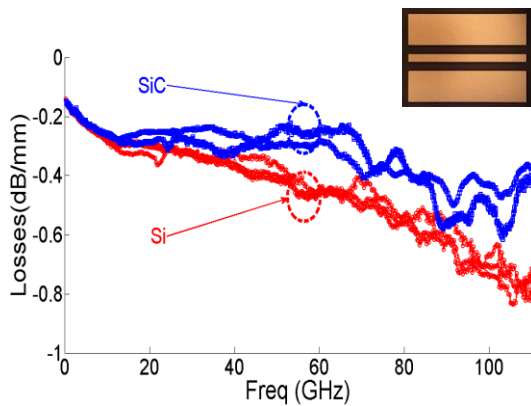
As seen in Figure 3, about 3% gate lag is observed and less than 15% drain lag is noticed up to  $V_{DS} = 20$ V. The low trapping effects under high electric field demonstrates the good quality of the epitaxy and the device processing.



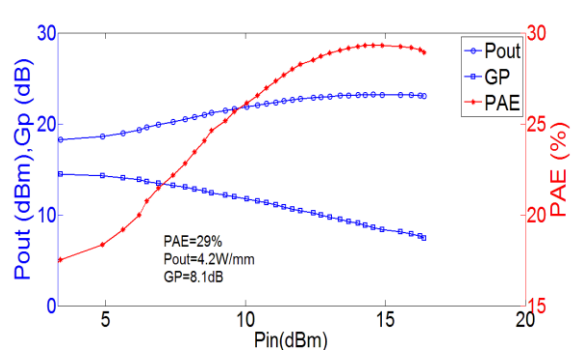
**Figure 3.** Output Pulsed I-V characteristic of a  $2 \times 50 \mu\text{m}$  AlN/GaN DHFET at  $V_{GS} = +1\text{V}$

The buffer / silicon interface quality is also confirmed by the losses through the transmission lines (TLs). TLs have been measured up to 110 GHz using a Schottky converter ZVA110 associated with L2RM calibration. Several lines of different sizes (1 mm and 2 mm) have been measured on Si and SiC substrates.

Up to 110 GHz, state-of-the-art losses below 0.8 dB/mm are achieved on Si substrate. Fig. 4 shows that the TL losses on Si substrate almost match the one observed on SiC substrate.



**Figure 4.** RF Losses up to 110 GHz extracted from 1 mm transmission lines (shown in the inset) for GaN-on-Si and GaN-on-SiC substrate



**Figure 5.** Pulsed power sweep at 18GHz of  $2 \times 50 \mu\text{m}^2$  AlN/GaN DHFET on a highly resistive silicon substrate at  $V_{DS} = 30\text{V}$

Finally, large signal measurements have been performed in pulsed mode (1  $\mu\text{s}$  pulse width) at 18 GHz using an automatic active load pull system developed in our laboratory [4]. Devices have been biased at  $V_{GS} = -0.3\text{V}$  and  $V_{DS} = 30\text{V}$ . It can be pointed out that drain biases as high as 30 V can be applied on these short devices owing to their high breakdown voltage. Figure 5 shows the power gain ( $G_p$ ), the output power ( $P_{out}$ ) and the power added efficiency (PAE). A maximum output power density of 4.5 W/mm is obtained combined with PAE of about 29% and a Power Gain of 8.1 dB. These high power

performance reflects the low RF losses that generally plague the intrinsic RF performance of GaN-on-silicon transistors.

## Conclusions

This work highlights the high quality of GaN-based epilayers grown on silicon substrate. State-of-the-art RF losses below 0.8 dB/mm above 100 GHz are observed, which is close to GaN-on-SiC substrate values. The low gate and drain lag effects associated to high power performances at 18 GHz also confirmed the quality of the epitaxy and the fabrication process.

Therefore, these results prove the viability of high performance GaN-based electronic devices on silicon substrates operating at high frequency.

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