

# Millimeter-wave high power GaN transistors: the race for better efficiency

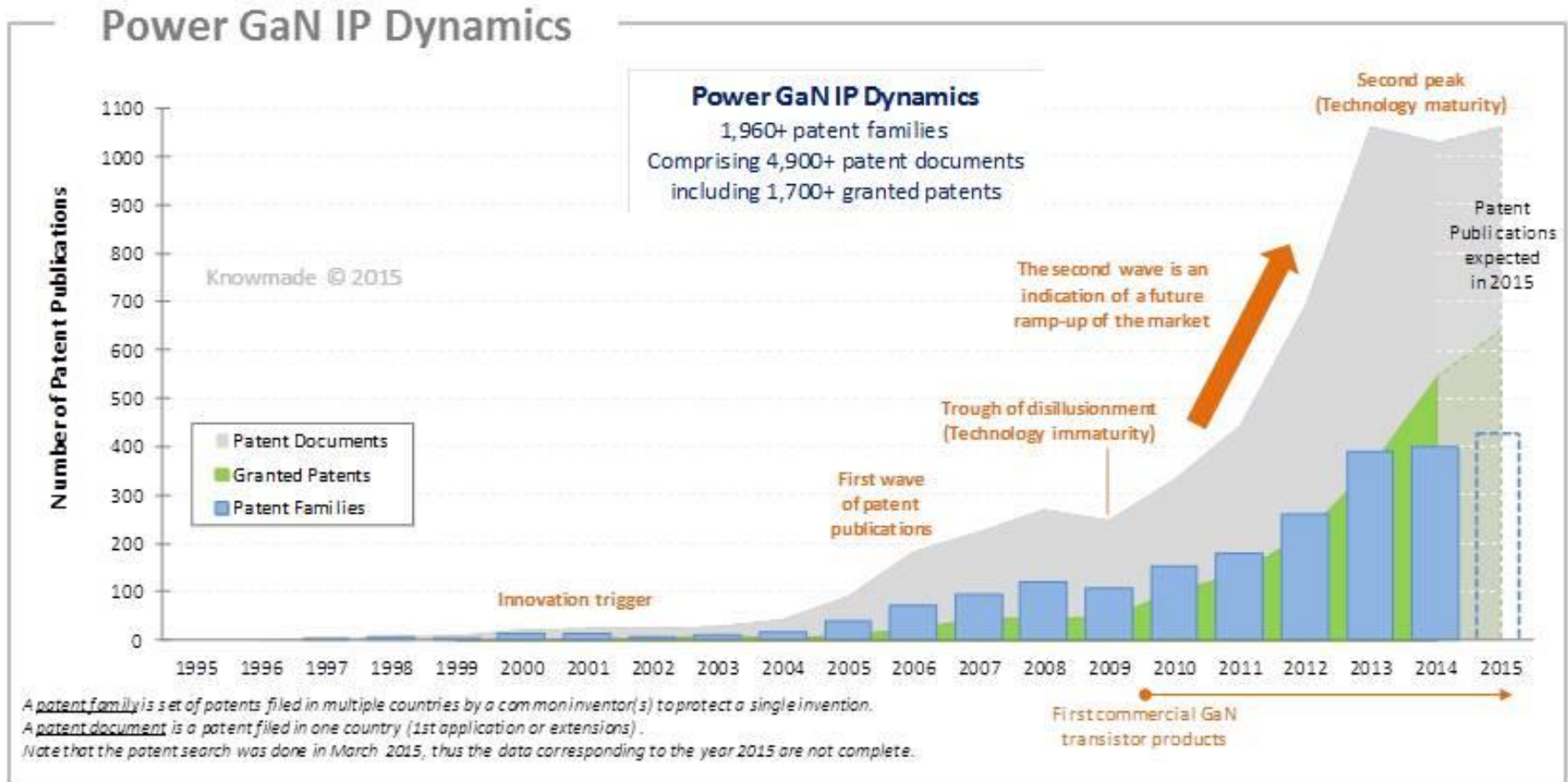
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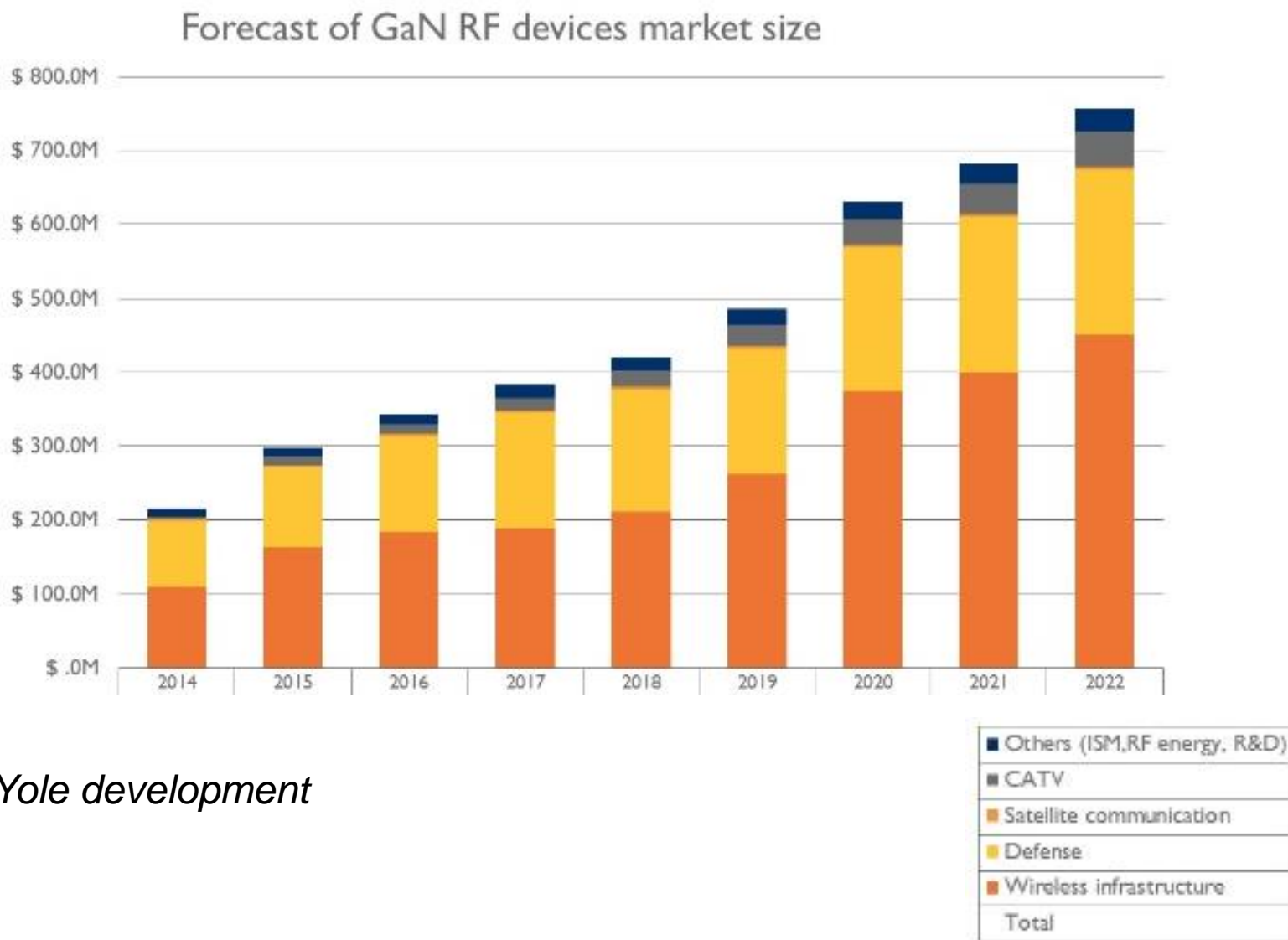
# OUTLINE

- Introduction
- Device design and characteristics for high PAE & robust Ka band GaN devices
  - Key features of the solution we propose
- Conclusion

# GaN is the semiconductor of the 21<sup>st</sup> century and should last for the next 30 years



# RF power market predictions



# K<sub>a</sub> band GaN PAs: a key device for space applications



*Artist's rendition of the new Eutelsat Quantum class satellite. Credit: Airbus Defence and Space*

Need to speed up transmission  
of high-rate science data from  
space missions



operating in Ka-band

Space market is going to evolve in future years thanks to the constant improvements of the GaN technology and the possibility to develop high efficiency and reliable SSPA for Ka-band applications.

The introduction of Ka-band GaN SSPA into the payload in replacement of existing TWTA is therefore of strategic interest.

# Why do we need high efficiency SSPAs?

TWT amplifier with necessary electronic power conditioner

*Courtesy NASA*



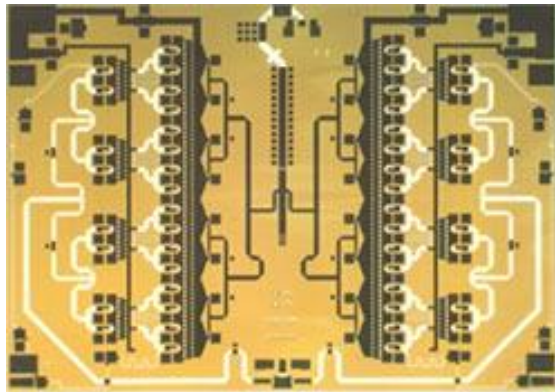
cover the majority of the amplifying stage on-board of satellites

BUT very large size !

Width & Height :

½ meter x 1 meter

Many required in payload architectures



Northrop Grumman GaAs-based PHEMT MMIC

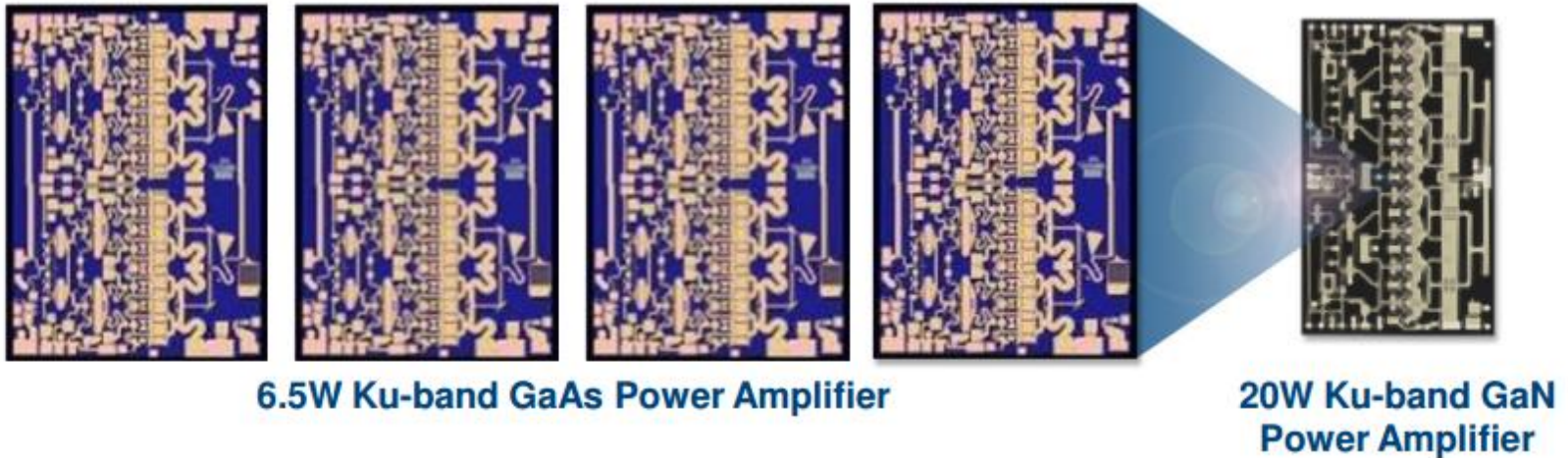
Width & Height :

Couple of mm x Couple of mm

100+ smaller than TWTAs  
BUT lower power capabilities &  
lower efficiency

# GaN devices delivered on their promises

- Significant advantages over GaAs technology or TWT
  - Small size + high robustness ( $T^{\circ}C$ , damp conditions) make GaN transistors the preferred choice for next generation SSPA



- In order to be the TWT killer, GaN will have to show extremely high power **and efficiency** also at higher frequency.
- **High power density (e.g. high operating voltage) of a single GaN device has to be maintained while increasing frequency of operation.**

# What is the current situation for RF GaN devices ?

- Commercial qualified power devices up to Ku band



And others...

- Qualification (e.g. high reliability) has been possible by reducing the electric field peak
  - using FP
  - and lower %Al into the barrier layer



# State-of-the-art of K- and Ka-band MMICs from foundries

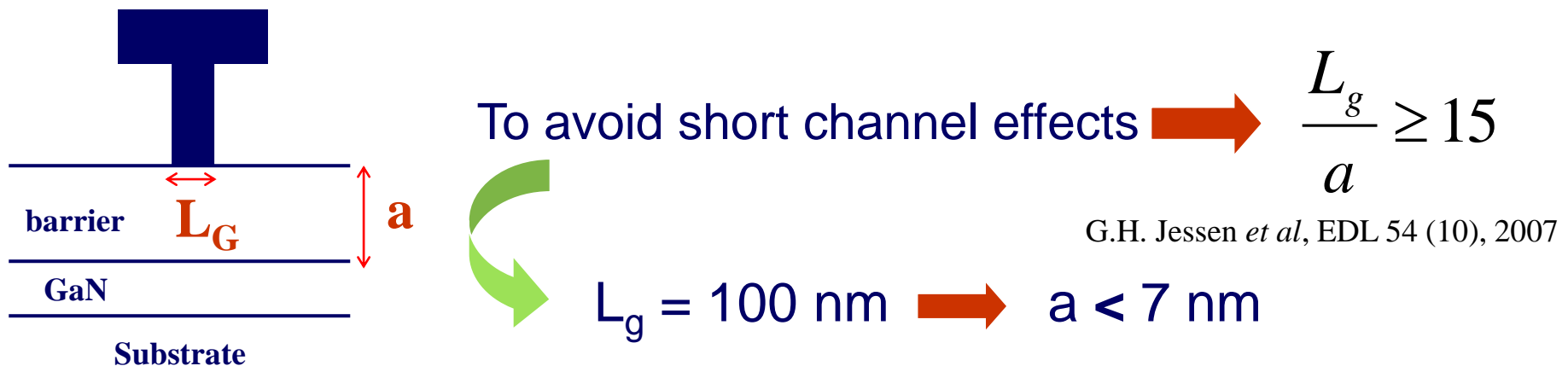
Vendor	Foundry	Frequency	Results	Periphery	Power density (W/mm)	$L_g$ (nm)	Year
Northrop Grumman	Available	18-23 GHz	6 W and PAE >30 % at $V_{DS}=28$ V, 20 dB gain	N/A	>3.4	200	2014
Northrop Grumman	Available	27-31 GHz	13 W and PAE = 25.5 % at $V_{DS}=28$ V, 19.5 dB gain	N/A	>3.4	200	2015
Toshiba	N/A	29-31 GHz	15 W, PAE=20%, 15 dB gain	N/A	N/A	N/A	2013
Qorvo	Available	29-31 GHz	8 W at 20 V, PAE=23-29%, gain=22-29 dB	14 cells (8x50 $\mu$ m)	>1.4	150	2015
Qorvo	Available	6-18 GHz	10 W at 20 V, PAE=20%, gain=25 dB	N/A	N/A	150	2016
IAF	Available	18-20 GHz	10 W, PAE = 30%, gain=20 dB	1 <sup>st</sup> stage 2x6x90 $\mu$ m 2 <sup>nd</sup> stage 4x8x100 $\mu$ m	>3	250	2016
OMMIC	Available	30 GHz	5.5 W, PAE = 32%, gain=20 dB	3 stage	3.3	100	2016
HRL	Available	40 GHz	0.5 W at 14 V, PAE = 10%, gain = 7dB	N/A	N/A	20	2016

**While achieving high Power density (> 3 W/mm), the PAE is still limited to about 30% in Ka band**

## Limiting factors of GaN device PAE

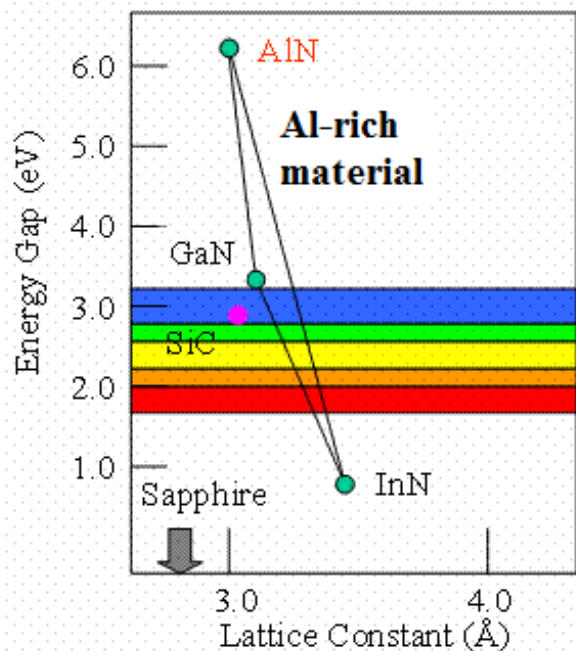
- High gain at frequency of operation (i.e. high frequency performances)
- Low  $R_{ON}$  (minimizing the losses)
- Self-heating (i.e.  $T_{channel}$ ) affecting the effective electron mobility under high bias
- Trapping effects both from surface and buffer to avoid dc to RF dispersion

- For Ka band and above (35 GHz +), the power gain becomes an issue with standard AlGaN barrier by using  $L_G \leq 0.15 \mu\text{m}$



- For high frequency, the electric field is needed
- No “derating” in terms of electric field anymore !

# AlN/GaN heterostructure



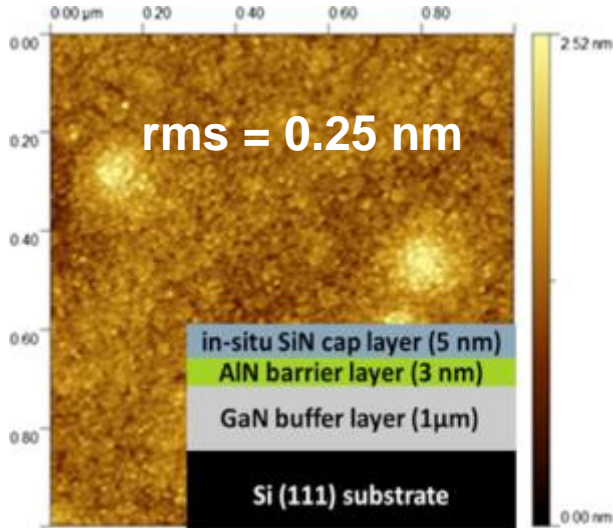
## An old idea but difficult to achieve:

Use of the widest III-N bandgap (AlN), theoretically the most attractive material to maintain high polarization while using ultrathin barrier

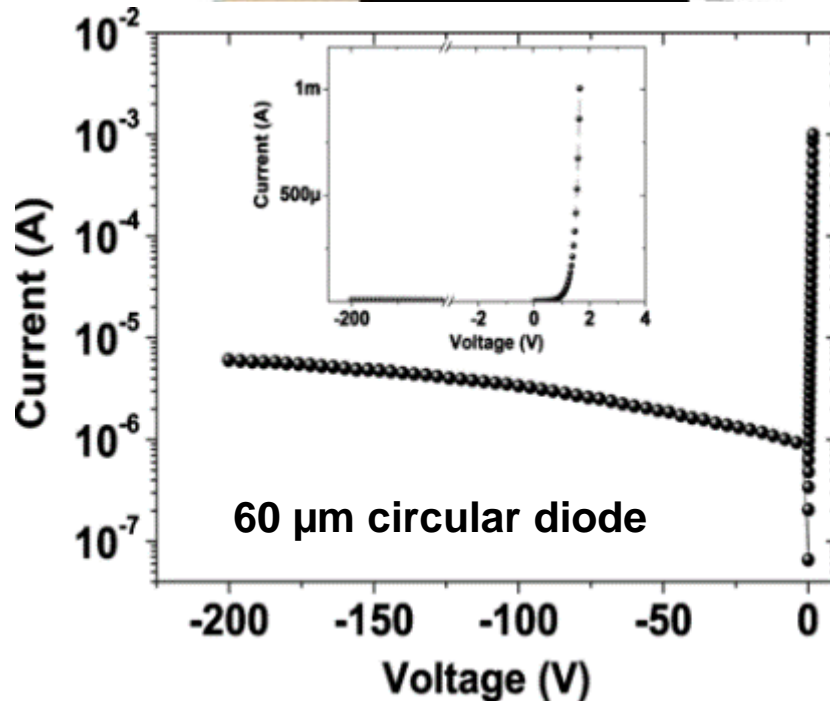
## Challenges:

- Leakage through / on top of the ultrathin barrier
- Leakage following extra PECVD SiN passivation
- Leakage due to punch-through effects (electron injection into the buffer)
- Trapping effects: surface close to the 2DEG

# Low gate leakage through only 3 nm AlN barrier

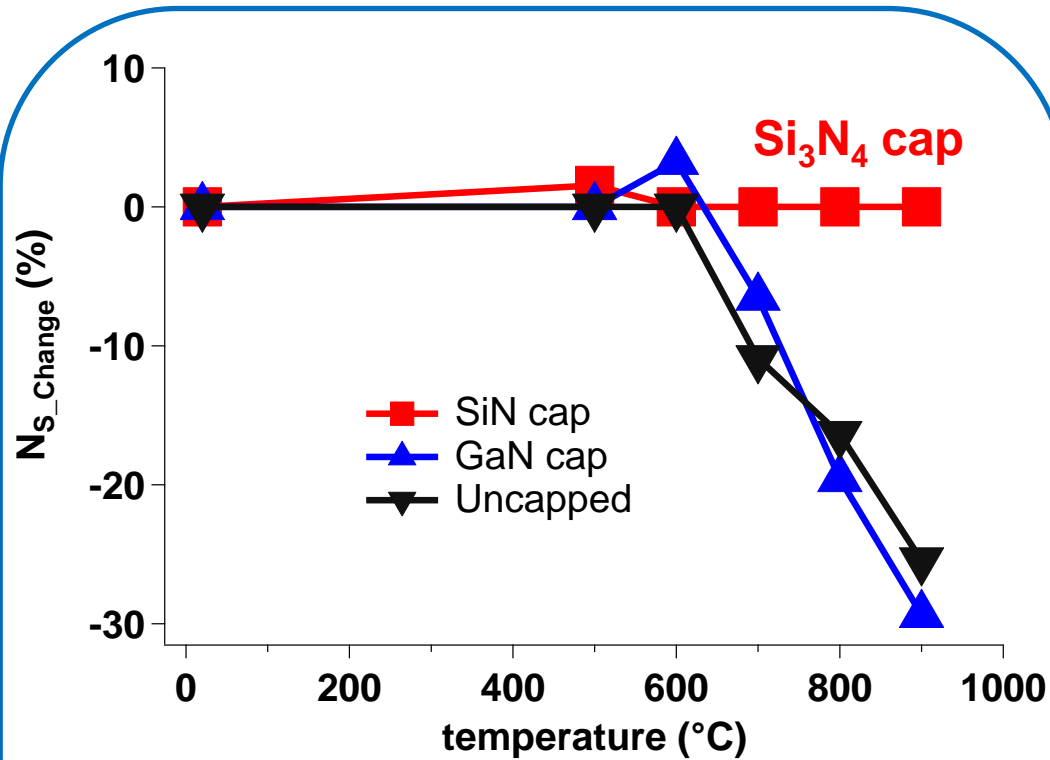


- High surface quality owing to the in-situ SiN preventing strain relaxation

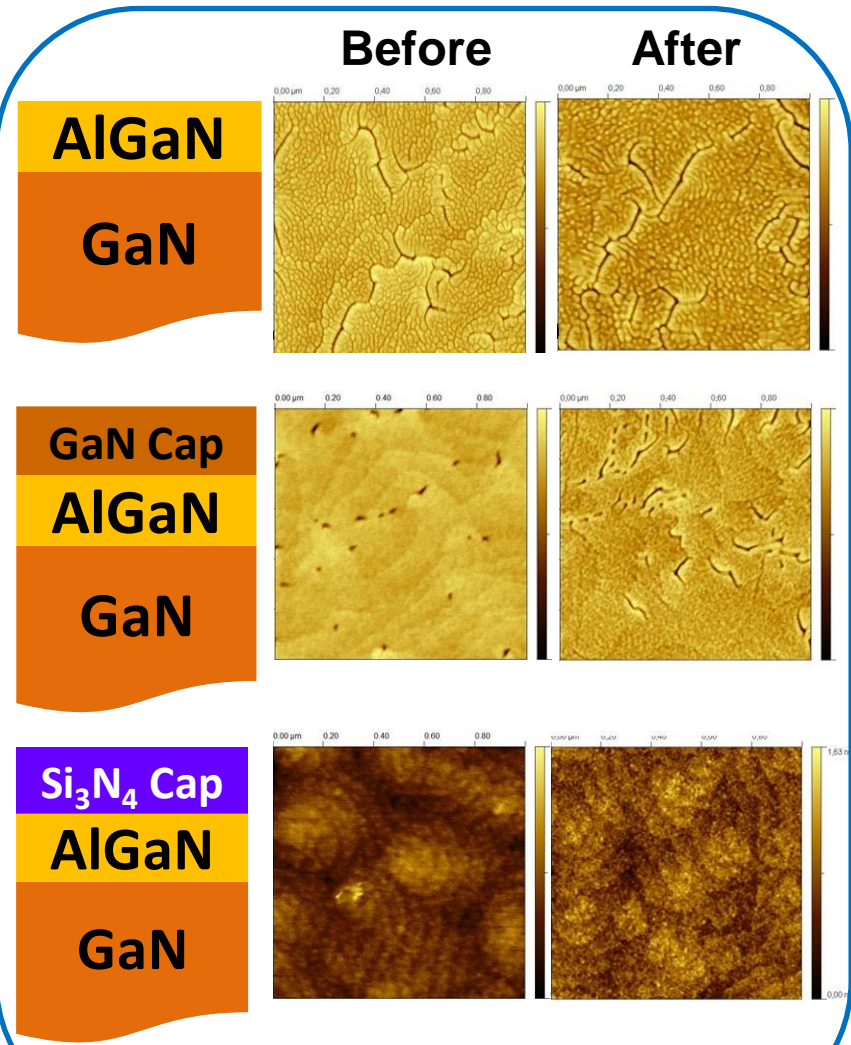


- Low Schottky gate leakage deposited directly on the AlN barrier layer (see forward diode)

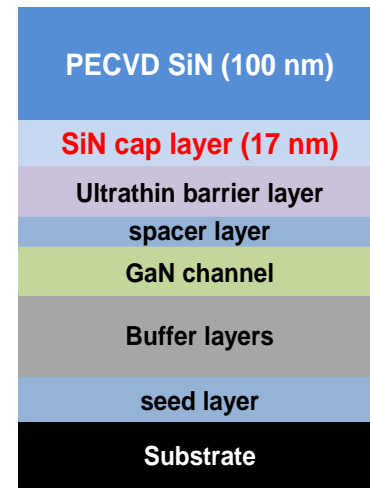
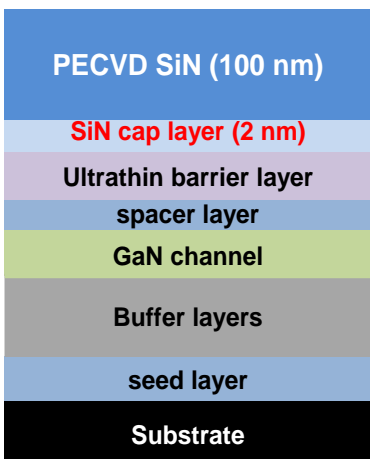
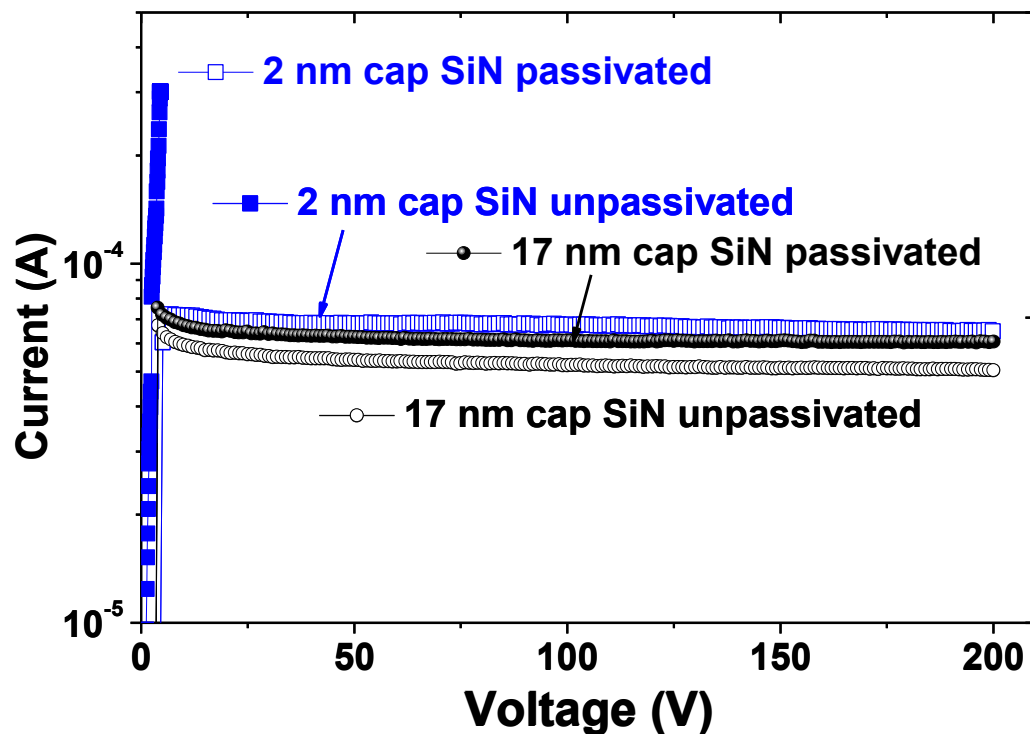
# Benefit of in-situ SiN cap layer



**EXPERIMENT** : The temperature was ramped up in vacuum to 900°C using a step of 100°C for 30 min. After each step Hall measurement was performed at RT.



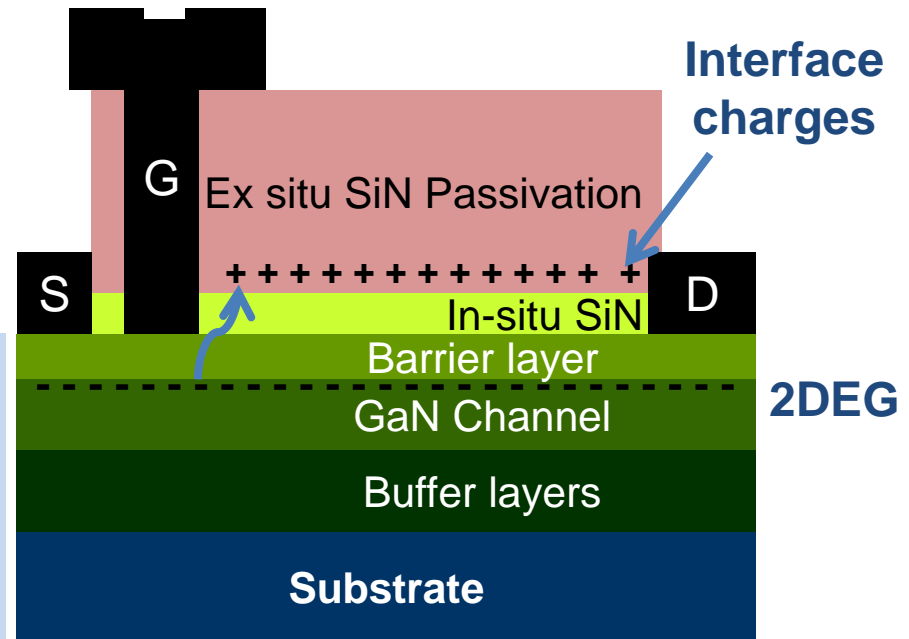
# 60 $\mu\text{m}$ circular diodes w and w/o 100 nm PECVD SiN passivation



- after SiN PECVD passivation: Strong and systematic degradation of gate leakage and early breakdown when using thin SiN cap layer of couple of nm.
- Almost no degradation of gate leakage when using thicker SiN cap layer.

# Proposed leakage current mechanism after full passivation

Electron injection at the MOCVD SiN / PECVD SiN interface under high electric field creating a conducting path at this location



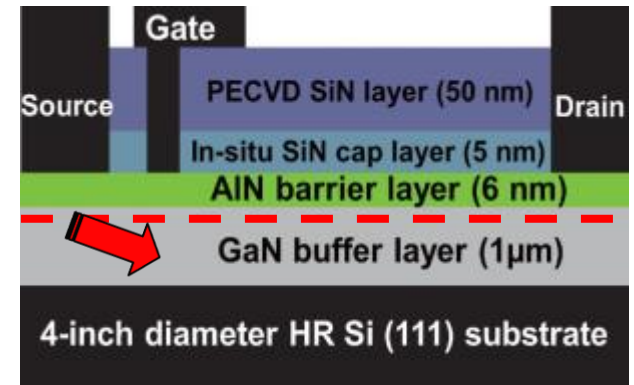
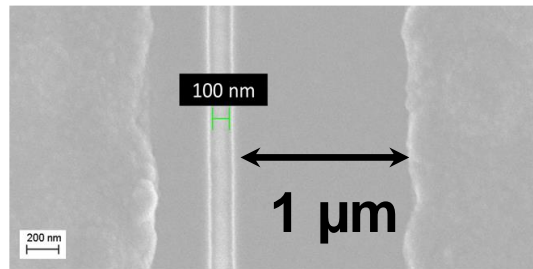
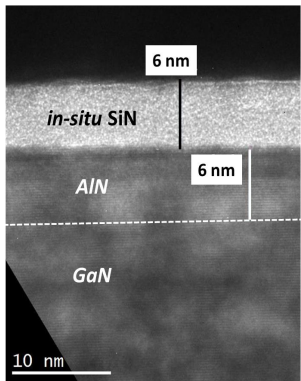
**A critical in-situ SiN cap layer thickness is needed to prevent the electron injection under high electric field**



# Buffer confinement for high voltage operation

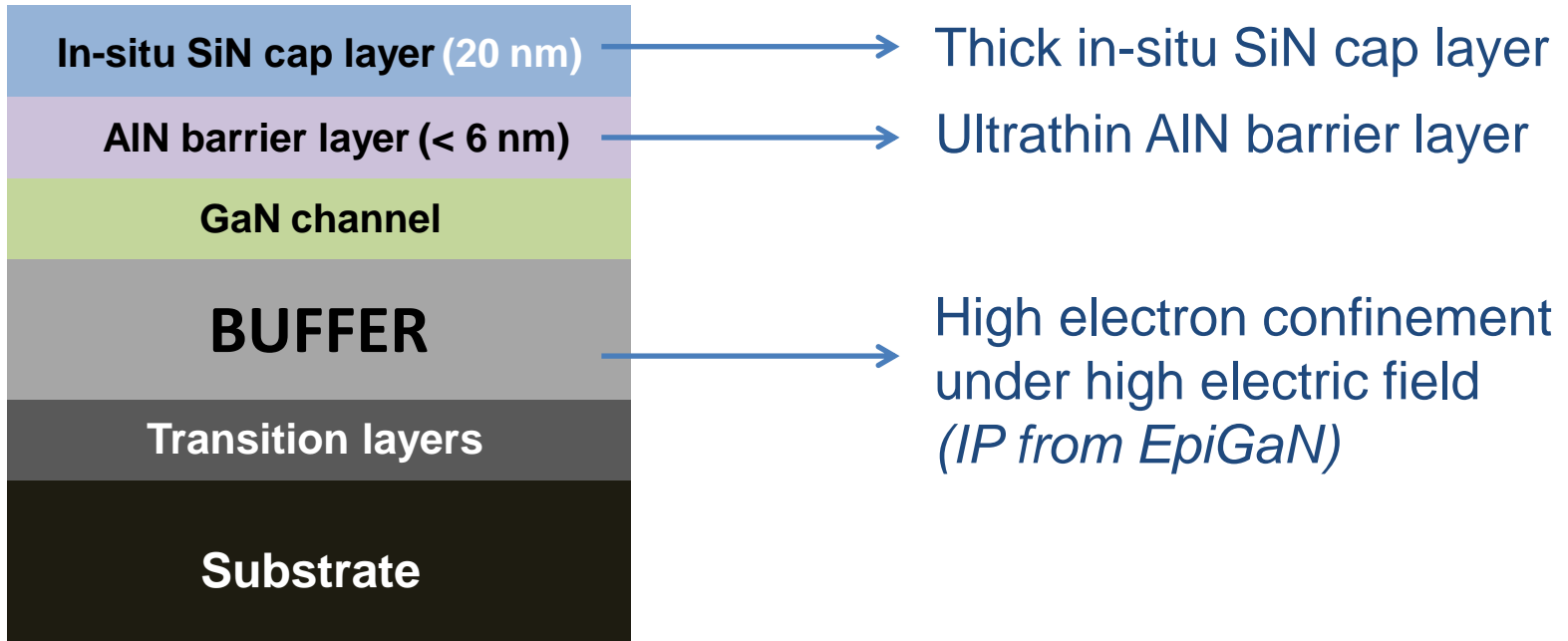
What about high voltage operation when using ultrashort GaN devices?

Ultrathin barrier + High  $N_s > 2 \times 10^{13} \text{ cm}^{-2}$  + Short  $L_{GD} \text{ \& } L_G$  +  $V_{DS} > 20 \text{ V}$  = Extremely high electric field



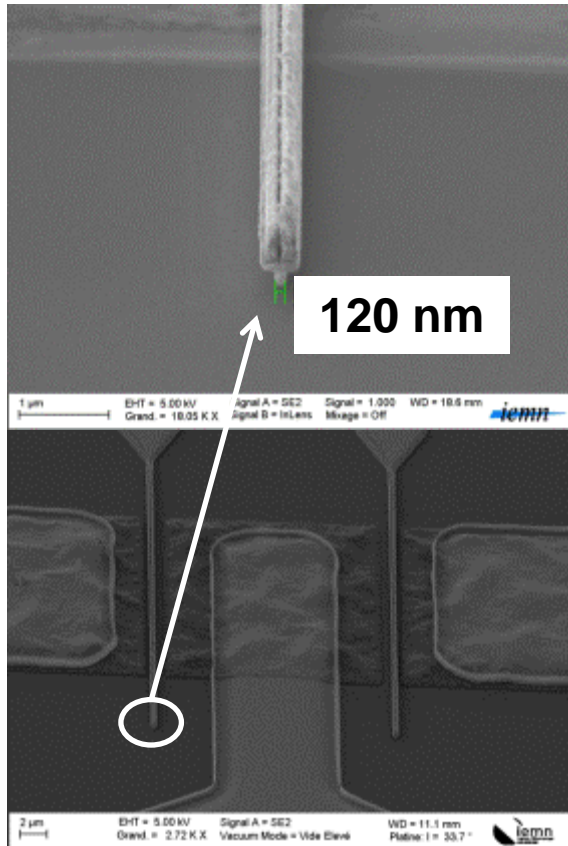
Poor electron confinement can be expected even if the material and processing are of high quality

# Device technology

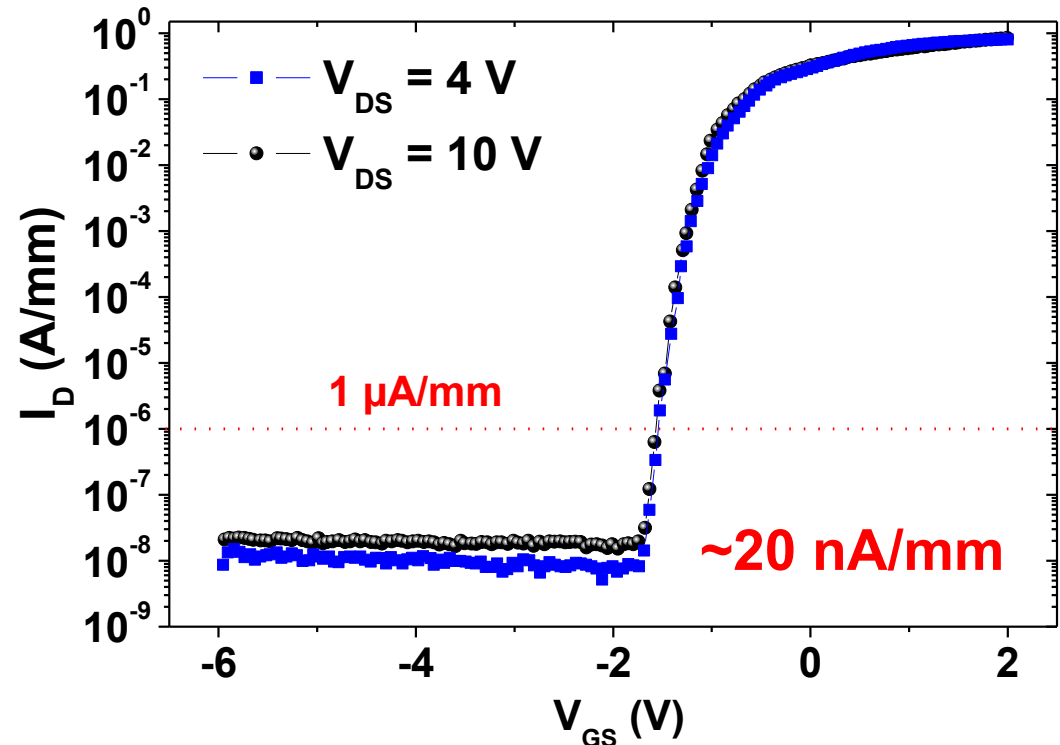


- Buffer layers have been specifically designed to enhance the electron confinement
- Ultrathin AlN barrier used for high aspect ratio with short  $L_G$  without degrading the 2DEG properties
- Thick SiN cap layer used to improve the device robustness, especially to avoid gate leakage current increase after full passivation

# Improvement of the electron confinement under high electric field to further push the GaN performance limits

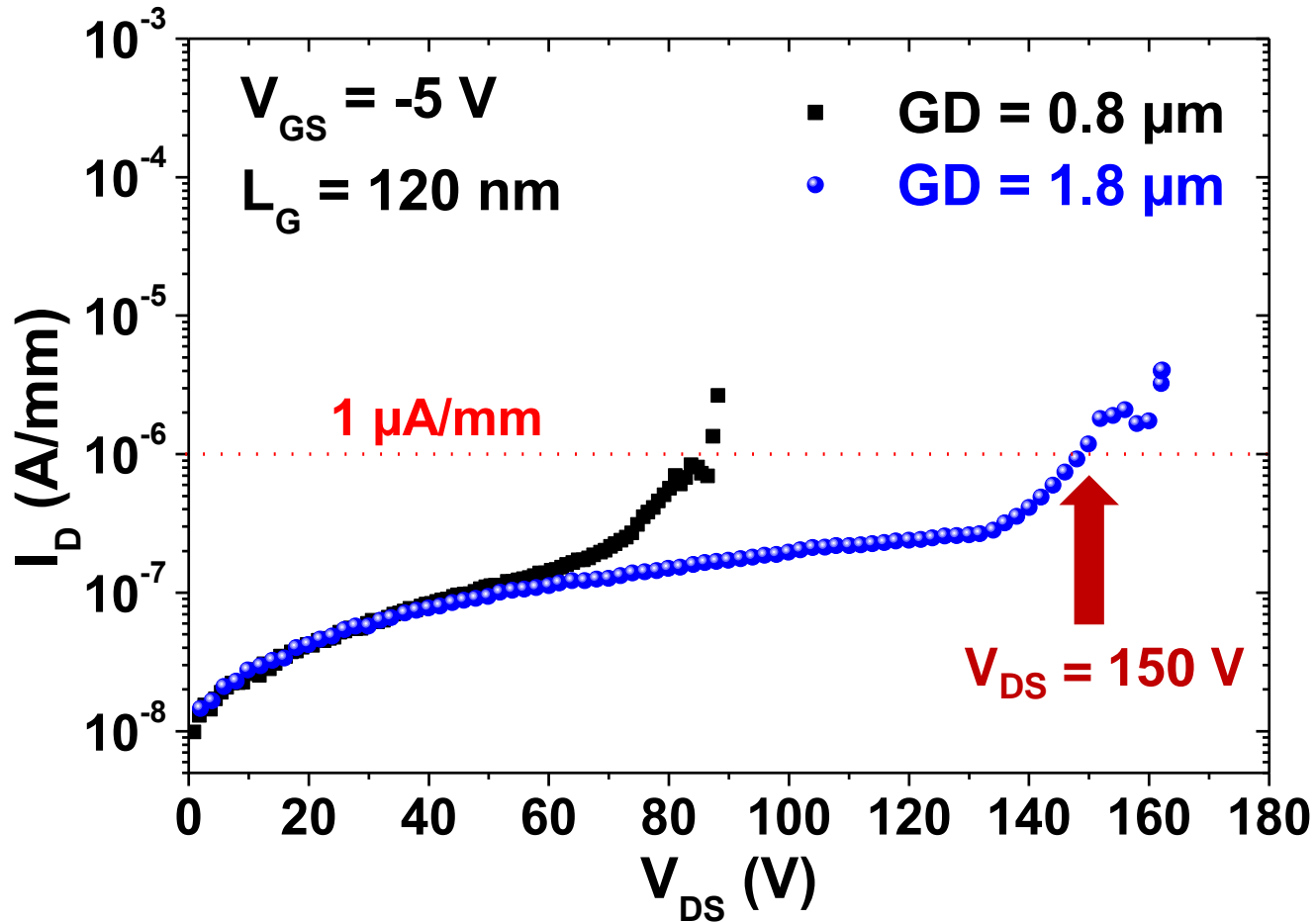


$L_g = 120 \text{ nm}$ ,  $GD < 2 \mu\text{m}$



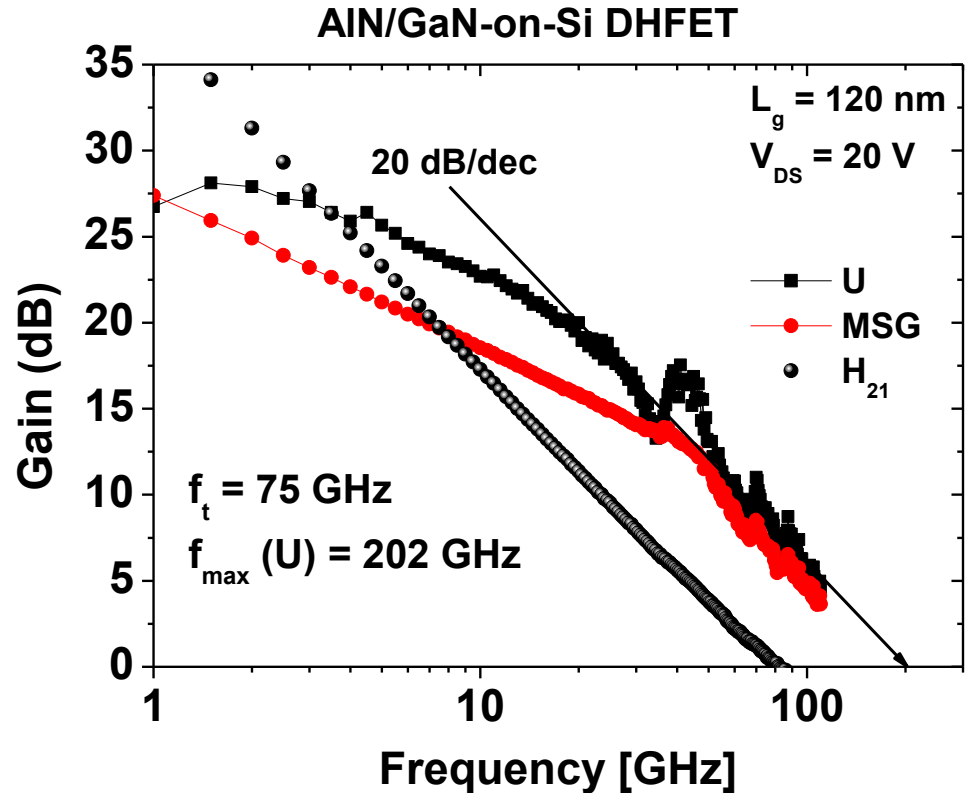
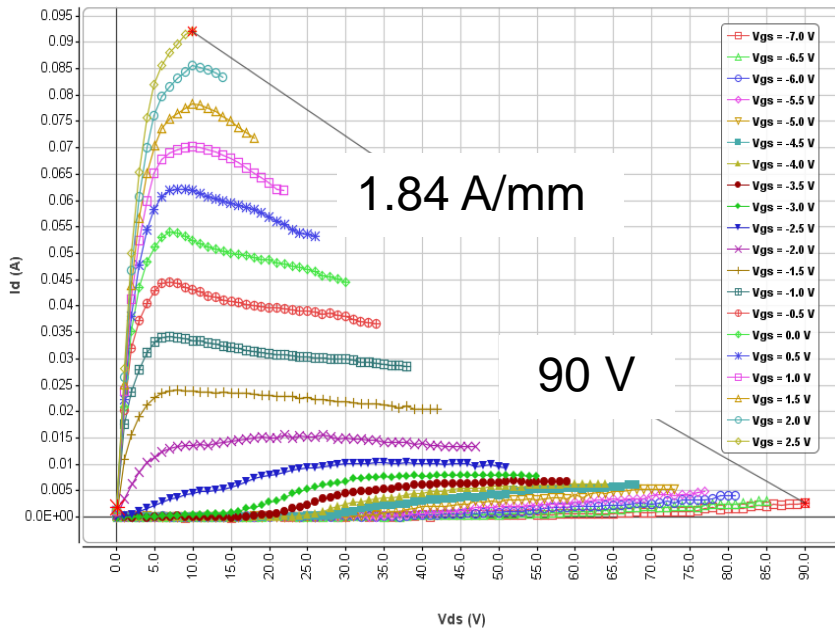
- Outstanding subthreshold leakage current  $< 1 \mu\text{A/mm}$  for sub-150 nm  $L_g$  while using a Schottky contact on  $< 5 \text{ nm}$  AlN barrier thickness showing an excellent electron confinement owing to an optimized buffer configuration

# Improvement of the electron confinement under high electric field to further push the GaN performance limits



BV about 100 V/ $\mu\text{m}$  for  $GD < 2 \mu\text{m}$  while using  $L_g$  sub-150 nm with extremely low leakage current  $< 1 \mu\text{A/mm}$  up to 150 V which is quite untypical

# High combination: $f_{\max} \times V_{\text{BK}}$

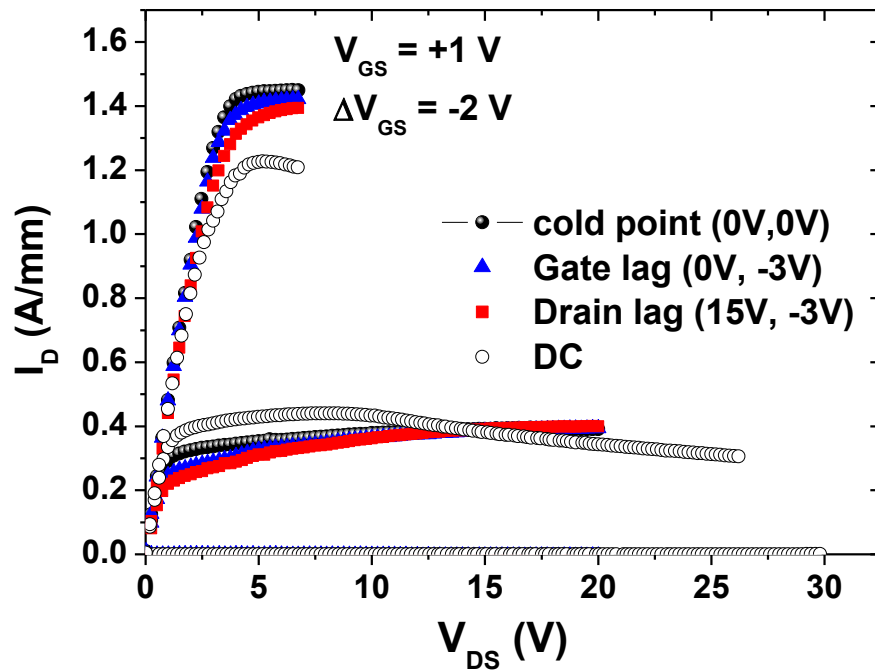


Fully reproducible devices delivering both high breakdown and high  $f_{\max}$

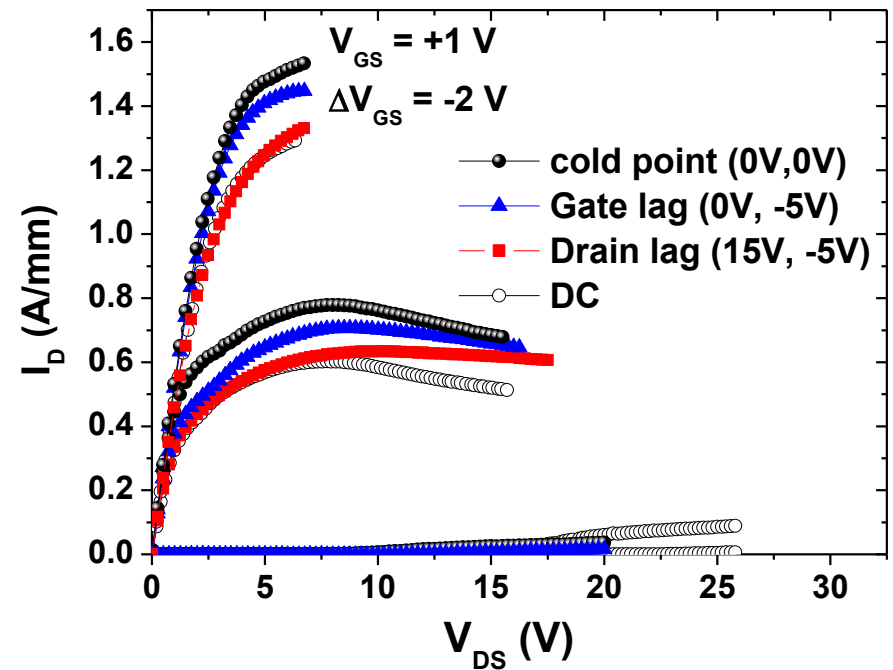
# Improved dynamic behavior in short GaN devices

AlN/GaN-on-Si devices using a critical SiN cap thickness  
( $L_G$  down to sub-100 nm)

DHFET:  $L_g = 200$  nm



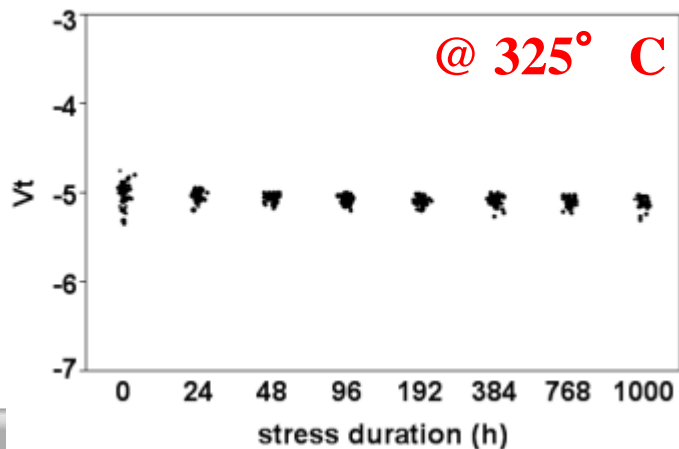
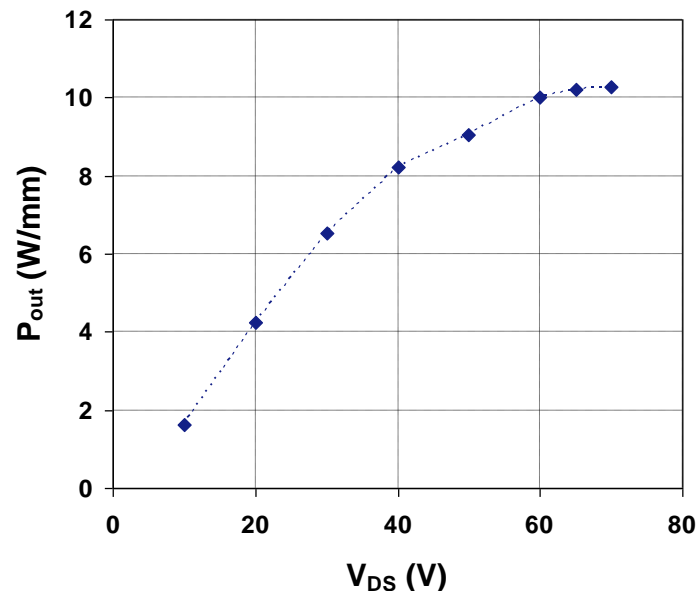
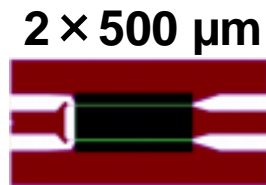
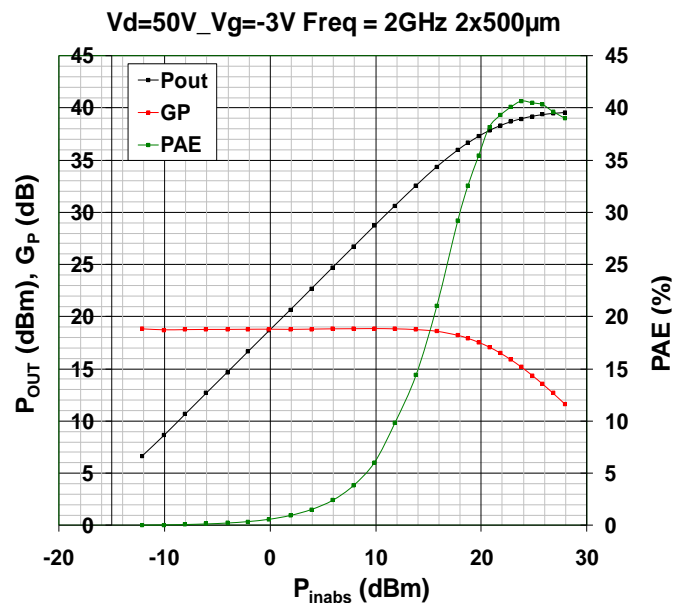
DHFET:  $L_g = 80$  nm



- Low trapping effects under 500 ns pulse width in highly scaled AlN/GaN devices

# High RF performance with high device robustness when using proper passivation design

## 50 nm SiN cap GaN-on-Si devices @ 2 GHz ( $L_G = 0.5 \mu\text{m}$ )

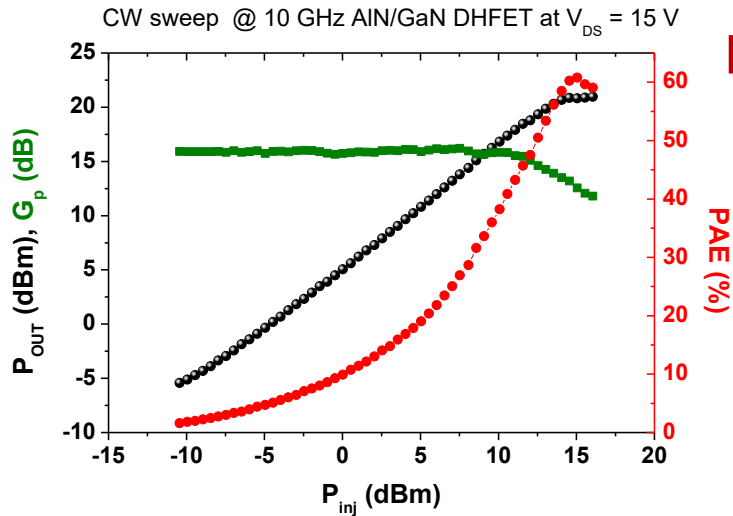


- Above 10 W/mm  $P_{OUT}$  at 2 GHz
- Unique thermal stability above 300° C (attributed to the thick in-situ SiN cap)

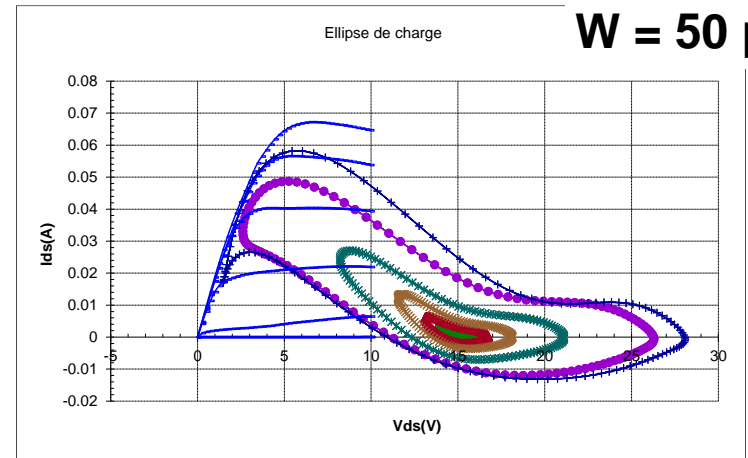
# 0.15 $\mu\text{m}$ AlN/GaN-on-SiC power measurement @ 10 and 18 GHz

## 4 nm barrier thickness

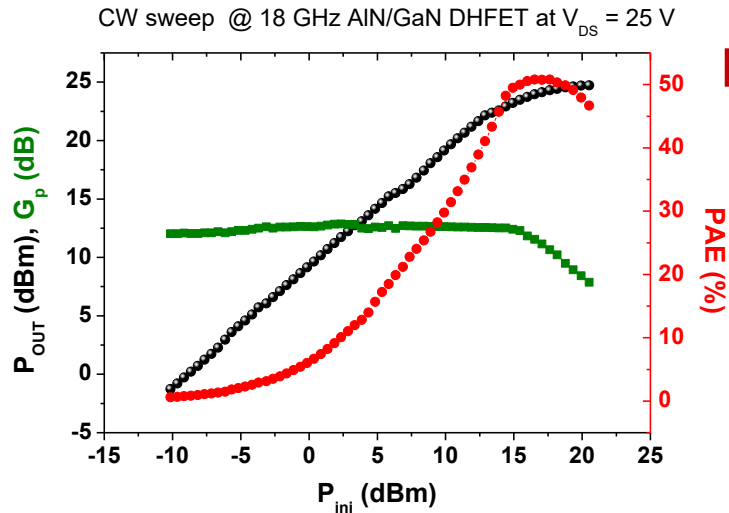
$W = 50 \mu\text{m}$



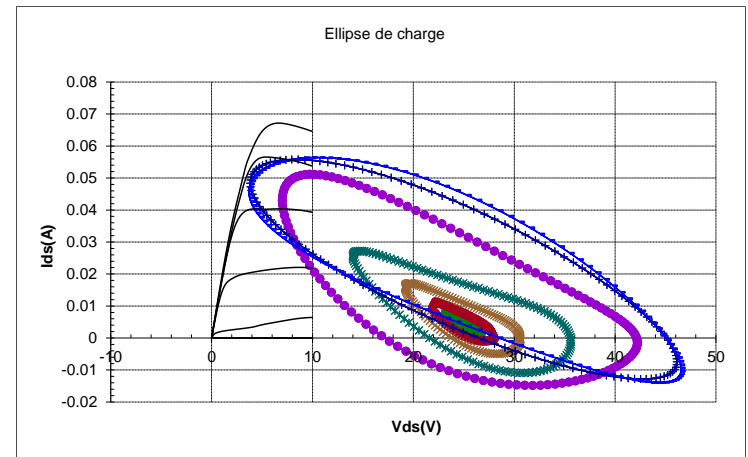
**PAE > 60%  
@ 10 GHz**



Load lines reflect the low RF dispersion  
The power gain confirms the high frequency performances



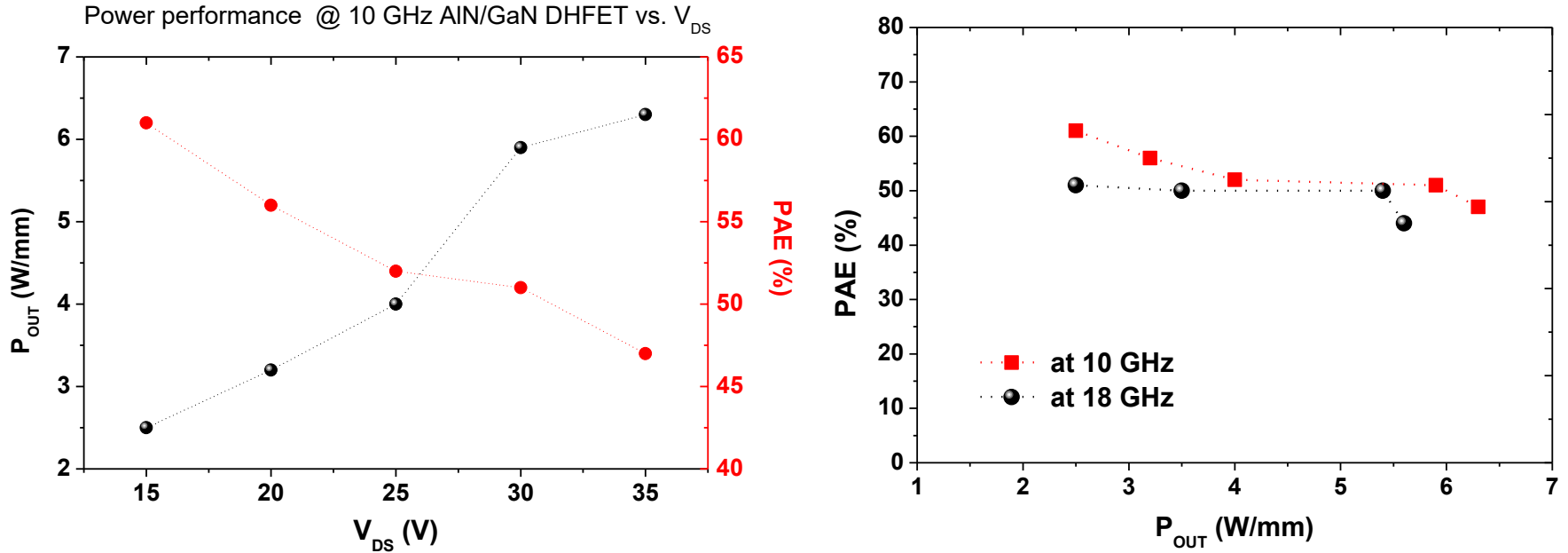
**PAE > 50%  
@ 18 GHz**



High PAE for the first time on sub-10 nm barrier GaN devices



# 0.15 $\mu\text{m}$ AlN/GaN-on-SiC power measurement @ 10 and 18 GHz

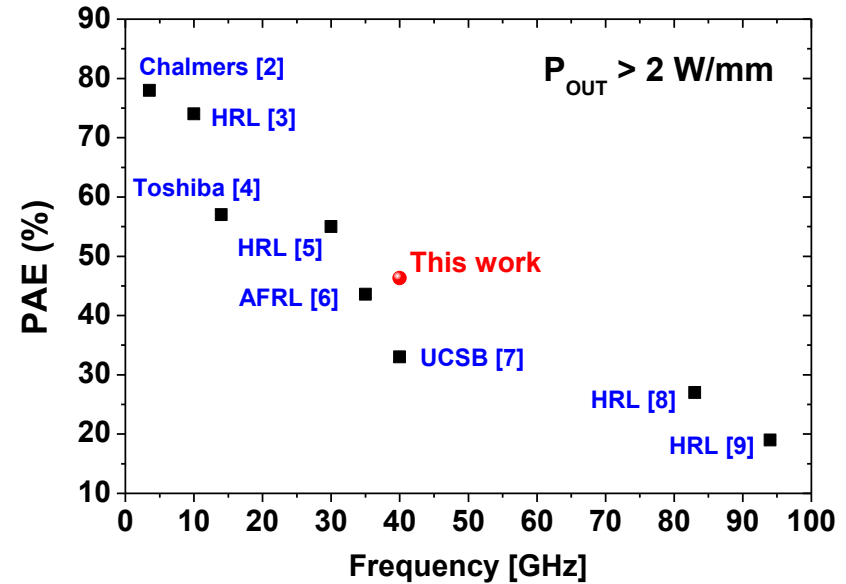
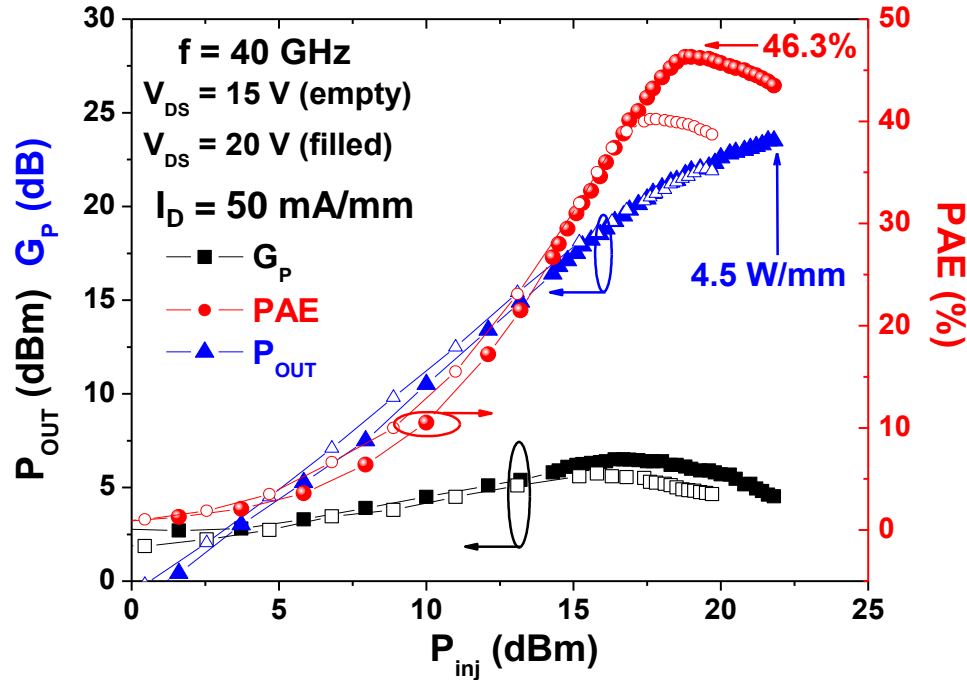


- High bias operation with ultrathin barrier GaN devices
- High PAE maintained up to high power densities

# 0.15 $\mu\text{m}$ AlN/GaN-on-SiC power measurements @ 40 GHz

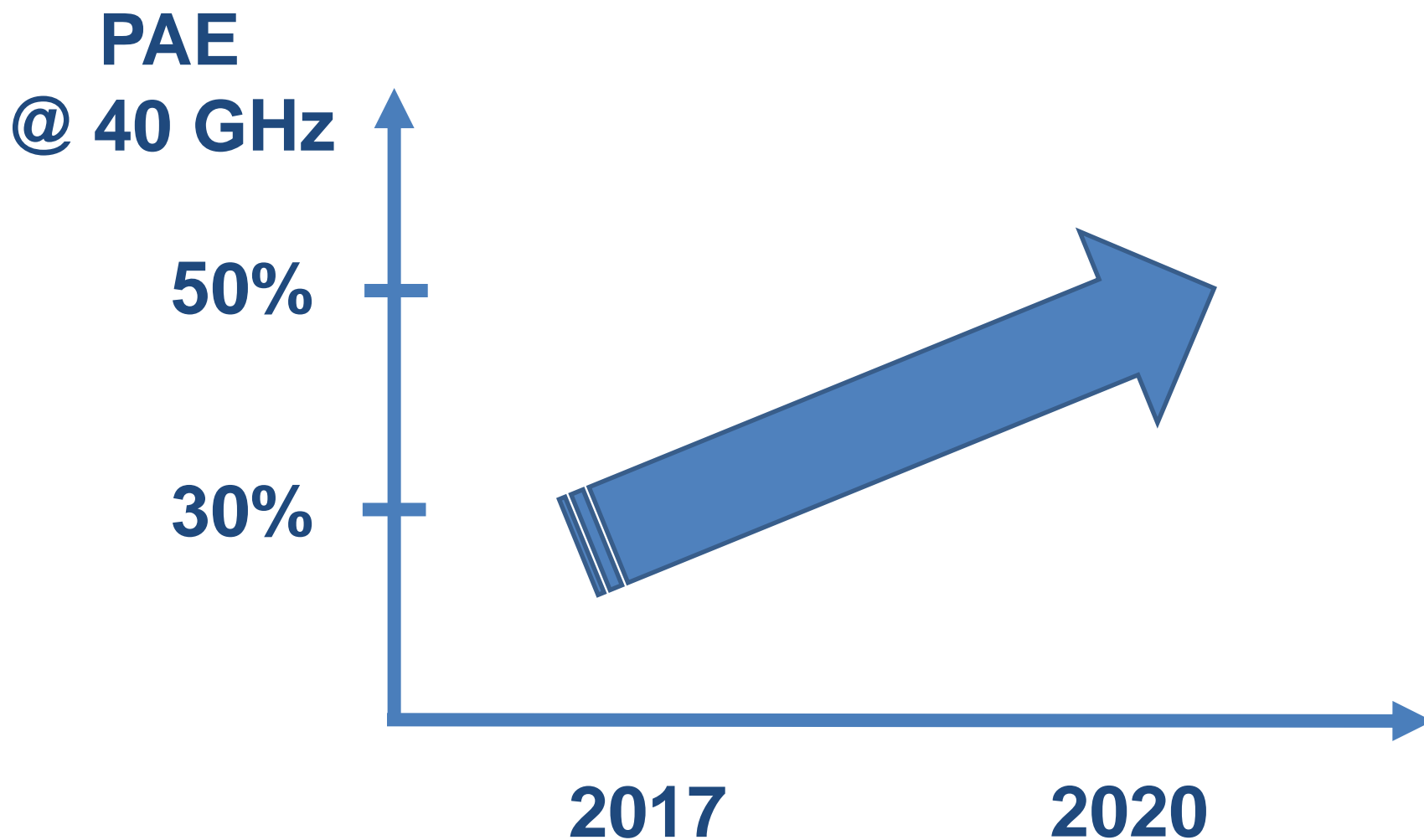
DHFET AlN/GaN-on-SiC. Barrier thickness of 4 nm

2x25  $\mu\text{m}$



State-of-the-art PAE @ 40 GHz for GaN devices

PAE > 50% @ 40 GHz will be possible soon with high power owing to innovative GaN devices

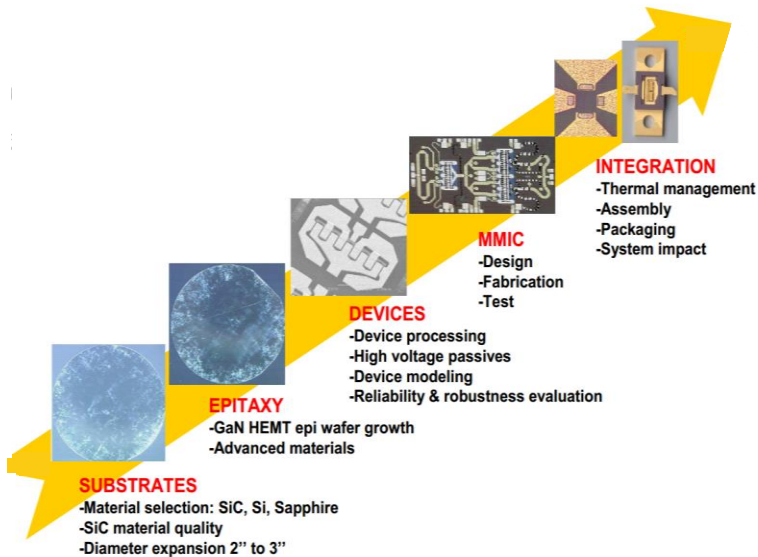


# Next generation of GaN RF devices in Europe

## EUGaNiC (2015-2019) :

Follow-up of EU programs (led by EDA)

KORRIGAN (2005-2009) et MANGA (2010-2014)



## Objectives :

- Qualification of GH25 generation fully European ( $L_G = 0.25 \mu\text{m}$ )
- Preparation and choice of industrial EU GH15 ( $L_G = 0.15 \mu\text{m}$ )
- IEMN contribution : Demonstrate the superiority of AlN/GaN for  $L_G = 150 \text{ nm}$  &  $100 \text{ nm}$  (performances + reliability !) compared to other types of heterostructures AlGaIn et InAlN

# Conclusion

- Possibility to achieve high breakdown (close to 100 V/ $\mu\text{m}$ ) under high electric field, with low leakage, and high PAE while using highly scaled sub-10 nm barrier GaN devices
- A critical in-situ SiN cap layer thickness is helpful to mitigate leakage current increase after full passivation resulting in superior device performance and robustness

Bright future for GaN !

Overcoming all challenges in highly scaled nitrides for breakthrough RF performances up to 100 GHz and above will definitely be achieved !