

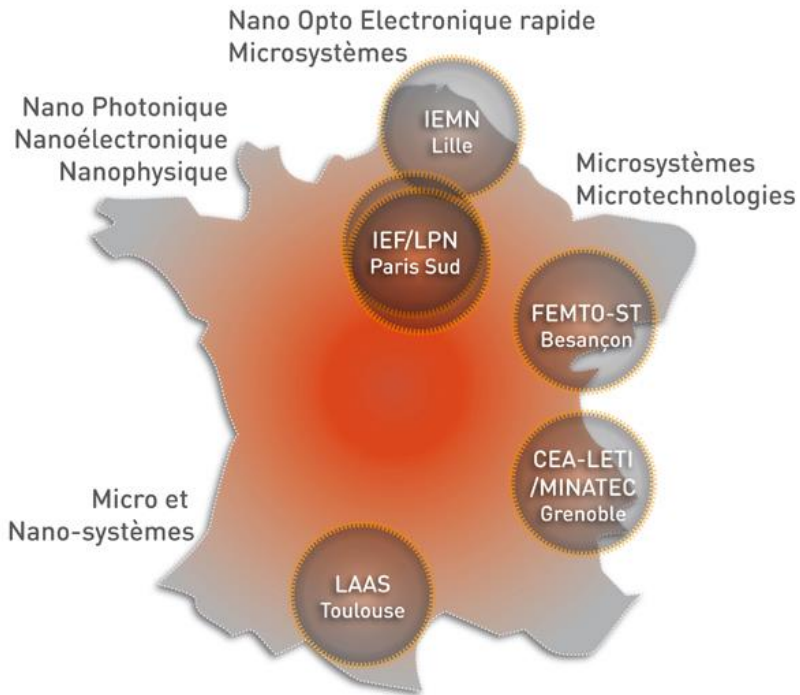
# Key features for high efficiency and highly robust mmW GaN HEMTs

R. Pecheux, R. Kabouche, T. Defais,  
E. Dogmus, M. Zegaoui

**F. Medjdoub**  
**CNRS - IEMN**



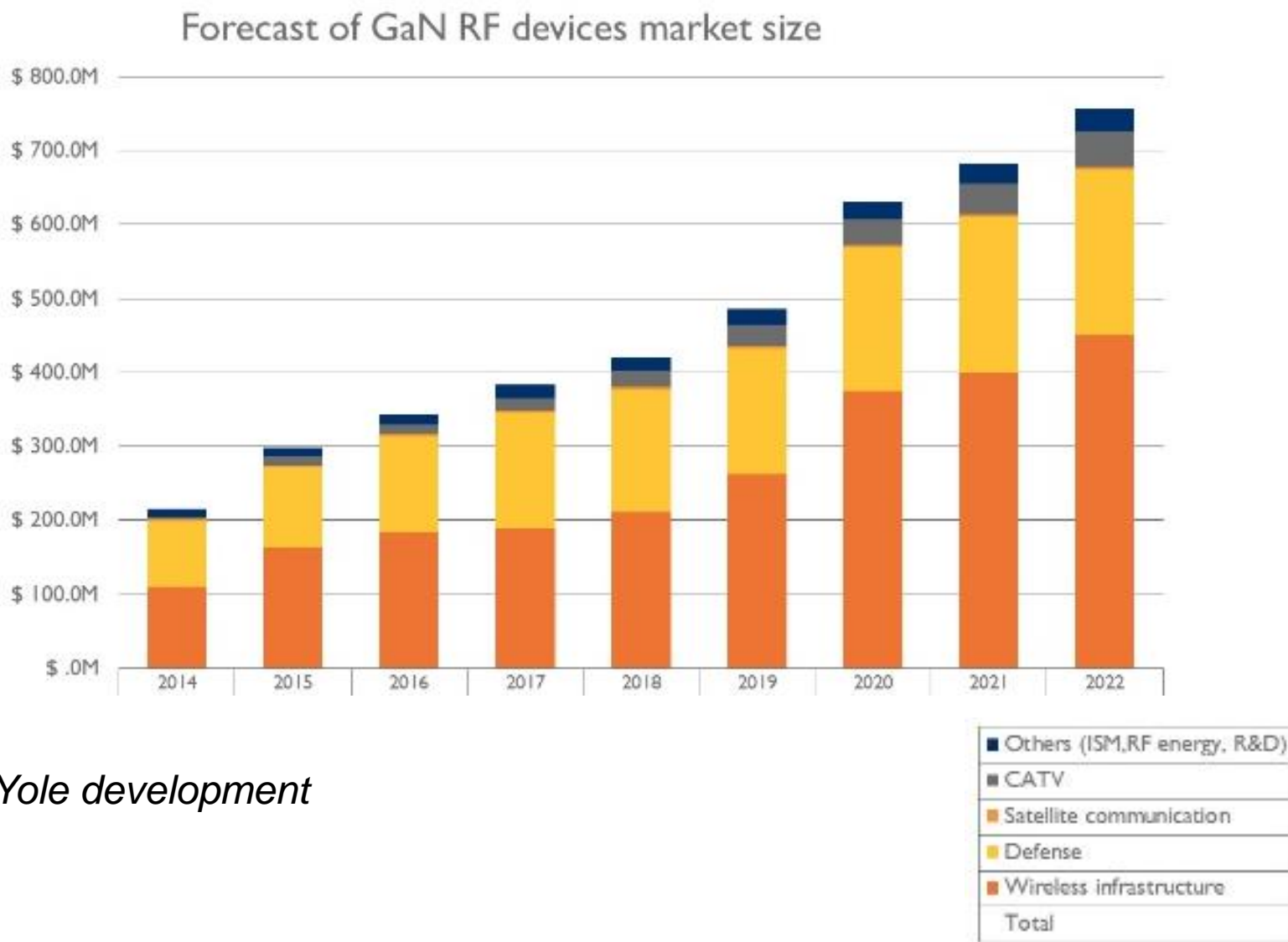
# National Network of Large Technological Facilities for Basic Research



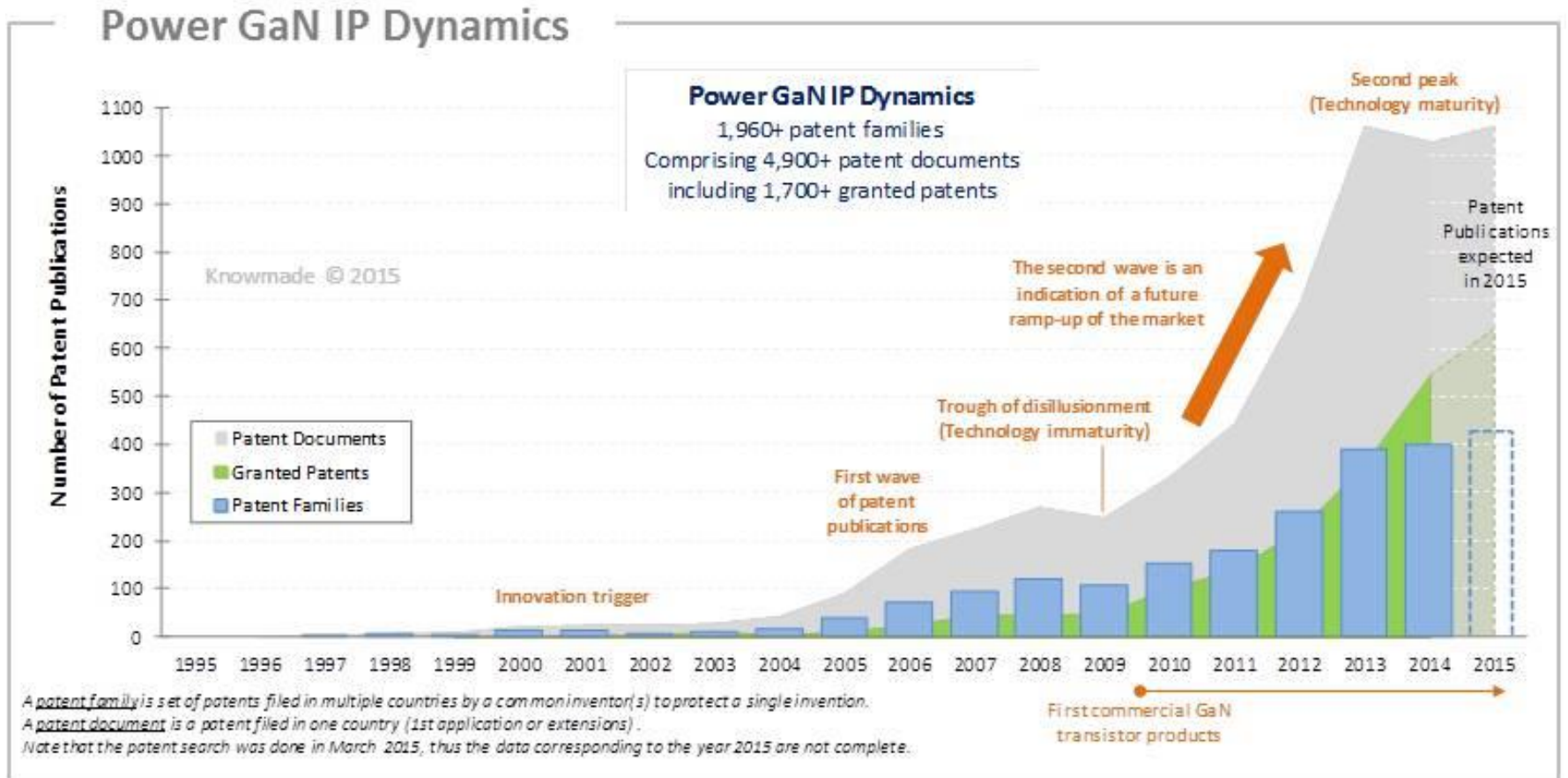
# OUTLINE

- Introduction
- Current status and challenges of mmW GaN devices
- Device design and characteristics for high PAE & robust Ka band + GaN devices
  - AlN/GaN DHFET vs. C-doped HEMT
- Conclusion

# RF power market predictions



# GaN is the semiconductor of the 21<sup>st</sup> century and should last for the next 30 years





# An example where GaN will bring a breakthrough: Space applications

TWT amplifier with necessary electronic power conditioner

*Courtesy NASA*



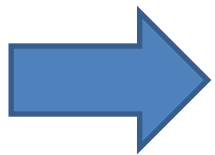
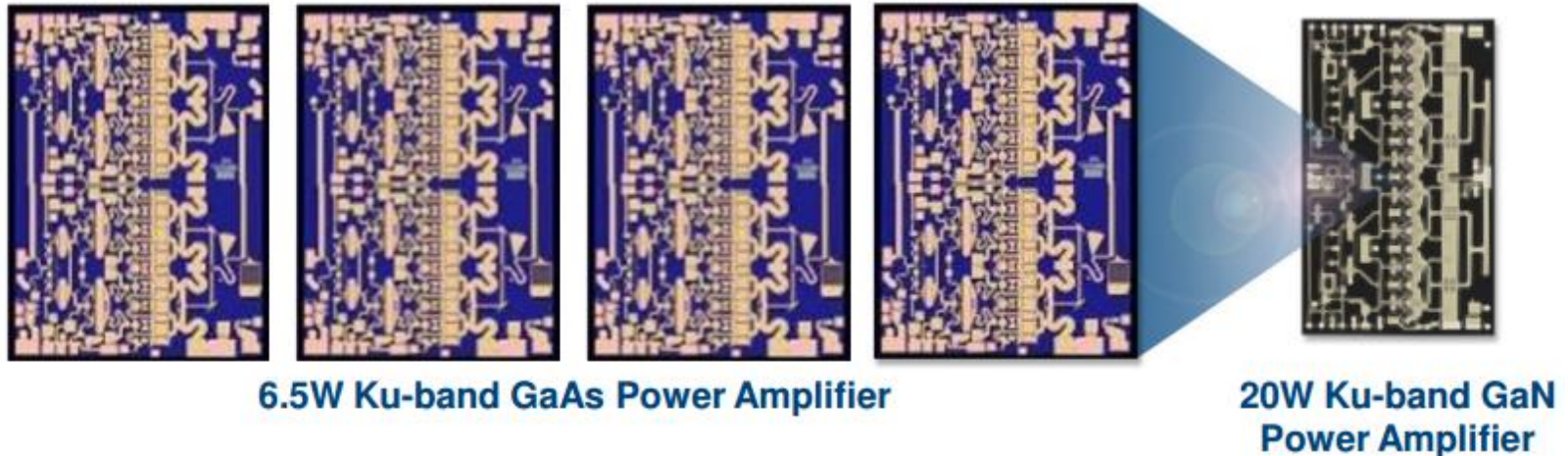
- Cover the majority of the amplifying stage on-board of satellites
- Operate in the mmW range with high power (> kW) & high PAE (about 50%)

BUT very large size !  
½ meter x 1 meter while many required in payload architectures

**Compact High power & efficiency SSPAs needed**

# GaN devices will be drastically smaller

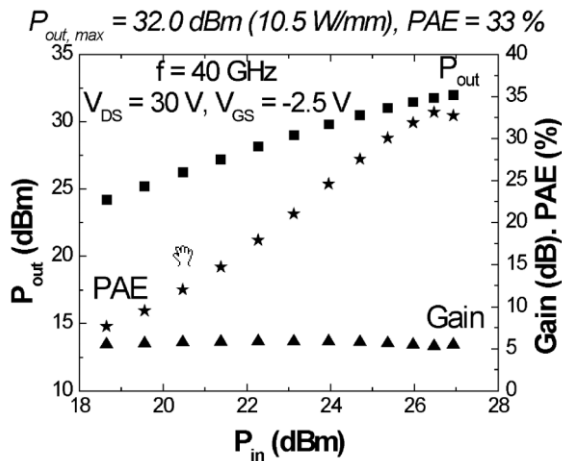
- Significant advantages over GaAs technology or TWT
  - Small size + high robustness ( $T^{\circ}C$ , damp conditions) make GaN transistors the preferred choice for next generation SSPA



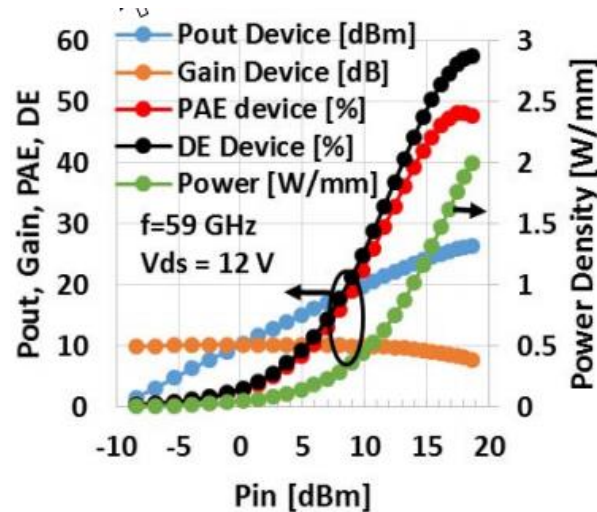
In order to be the TWT killer, GaN will have to show extremely high power **and efficiency** also at higher frequency.

# Current state-of-the-art: from the labs

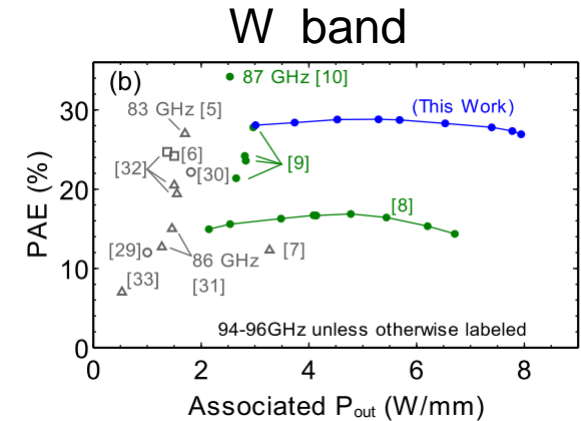
- Output power not the main issue as GaN material and technology are maturing



**UCSB:** T. Palacios et al, *IEEE EDL*, 26 (11), 2005



**HRL:** M. Micovic et al, *IEEE EDL*, 38 (12), 2017



**UCSB:** B. Romanczyk et al, *IEEE TED*, in Press, 2017

- ✓ PAE < 50% in the mmW range
- ✓ No device robustness/reliability demonstrated with sub-150 nm gate length (preventing market penetration)

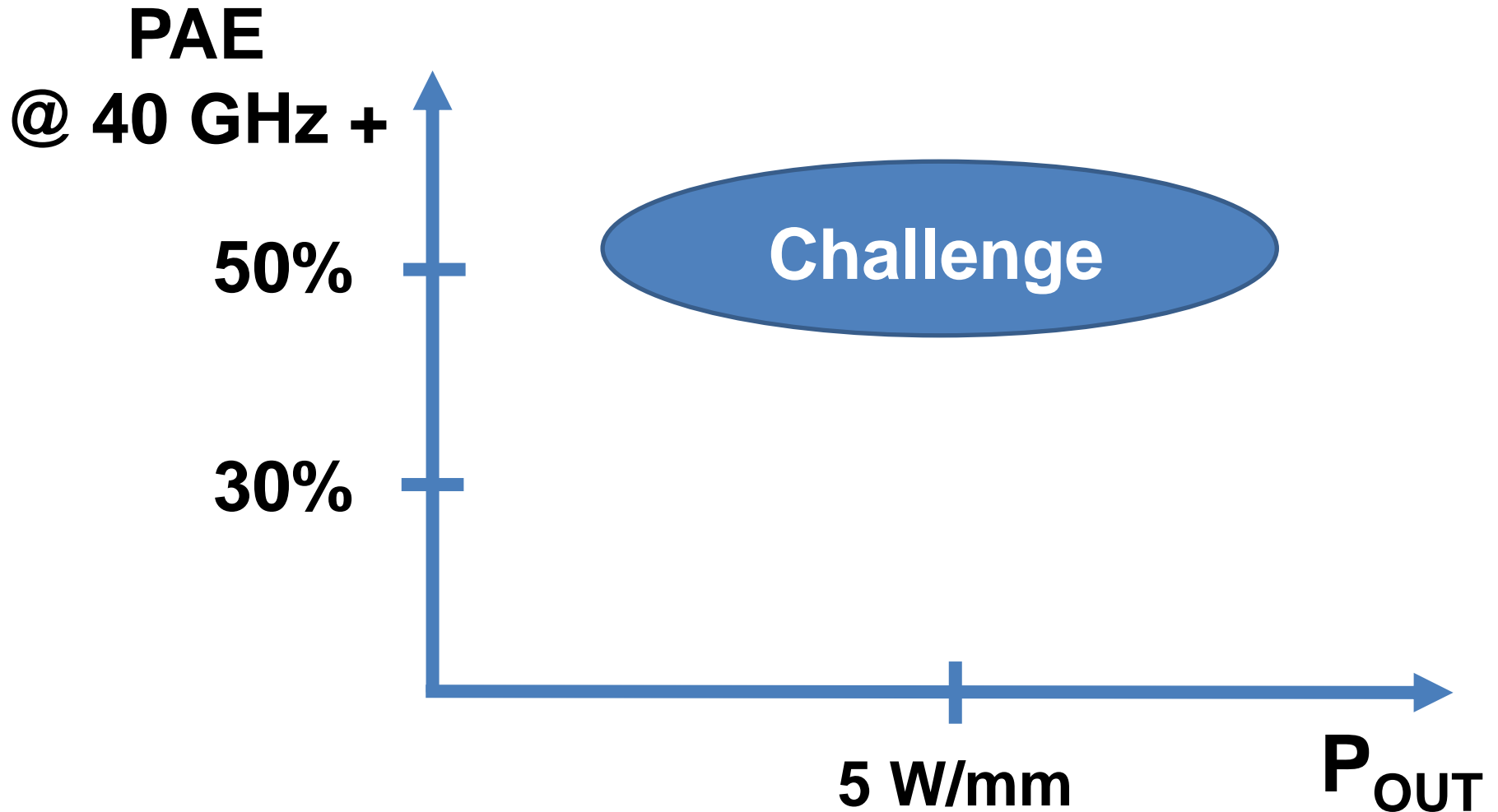


# State-of-the-art of K- and Ka-band MMICs from foundries

Vendor	Foundry	Frequency	Results	Periphery	Power density (W/mm)	$L_g$ (nm)	Year
Northrop Grumman	Available	18-23 GHz	6 W and PAE >30 % at $V_{DS}=28$ V, 20 dB gain	N/A	>3.4	200	2014
Northrop Grumman	Available	27-31 GHz	13 W and PAE = 25.5 % at $V_{DS}=28$ V, 19.5 dB gain	N/A	>3.4	200	2015
Toshiba	N/A	29-31 GHz	15 W, PAE=20%, 15 dB gain	N/A	N/A	N/A	2013
Qorvo	Available	29-31 GHz	8 W at 20 V, PAE=23-29%, gain=22-29 dB	14 cells (8x50 $\mu$ m)	>1.4	150	2015
Qorvo	Available	6-18 GHz	10 W at 20 V, PAE=20%, gain=25 dB	N/A	N/A	150	2016
IAF	Available	18-20 GHz	10 W, PAE = 30%, gain=20 dB	1 <sup>st</sup> stage 2x6x90 $\mu$ m 2 <sup>nd</sup> stage 4x8x100 $\mu$ m	>3	250	2016
OMMIC	Available	30 GHz	5.5 W, PAE = 32%, gain=20 dB	3 stage	3.3	100	2016
HRL	Available	40 GHz	0.5 W at 14 V, PAE = 10%, gain = 7dB	N/A	N/A	20	2016

**While achieving high Power density (> 3 W/mm), the PAE is still limited to about 30% in Ka band**

# Main challenges for mmW applications



✓ PAE > 50% in the Q band and above together with high device robustness under high electric field ( $V_{DS} \geq 15$  V)

# Limiting factors of mmW GaN device PAE

Gain



High frequency performances

Self-heating



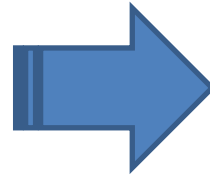
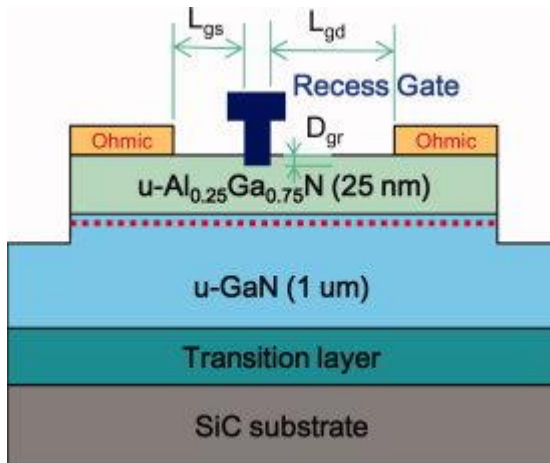
Thermal dissipation

Trapping effects



Control of surface and bulk traps

# Gate recess for mmW GaN devices: not an option !



under high electric field (defects induced by plasma are detrimental)

Because of the lack of efficient chemical (low damage) etching solution for GaN-based material

A solution is the use of an ultrathin barrier layer with wider bandgap

To both maintain a high carrier density and achieving a low gate to channel distance

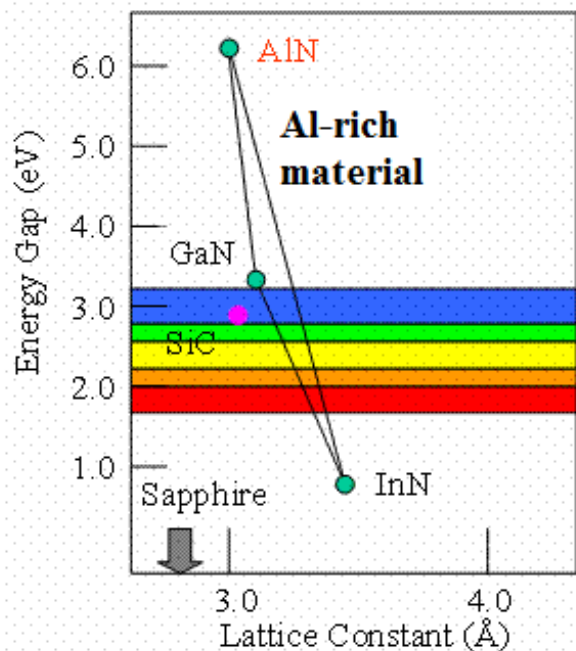
InAlN

Gate leakage issue not solved !

InAlGaN

AlN

# AlN/GaN heterostructure



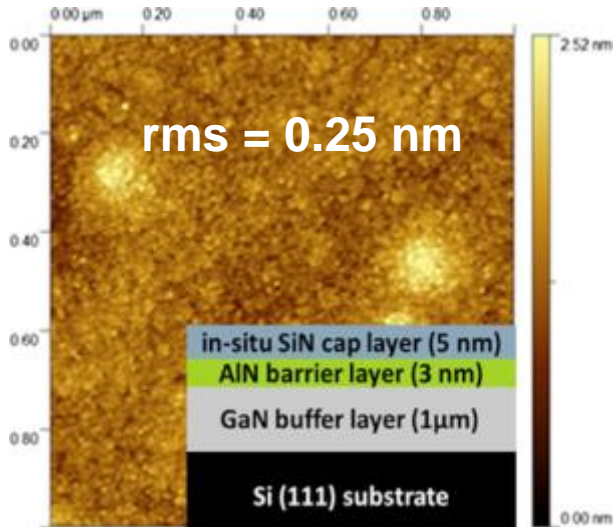
The idea is to use the widest III-N bandgap (AlN) as possible in order to maintain a high polarization while using ultrathin barrier

## Challenges:

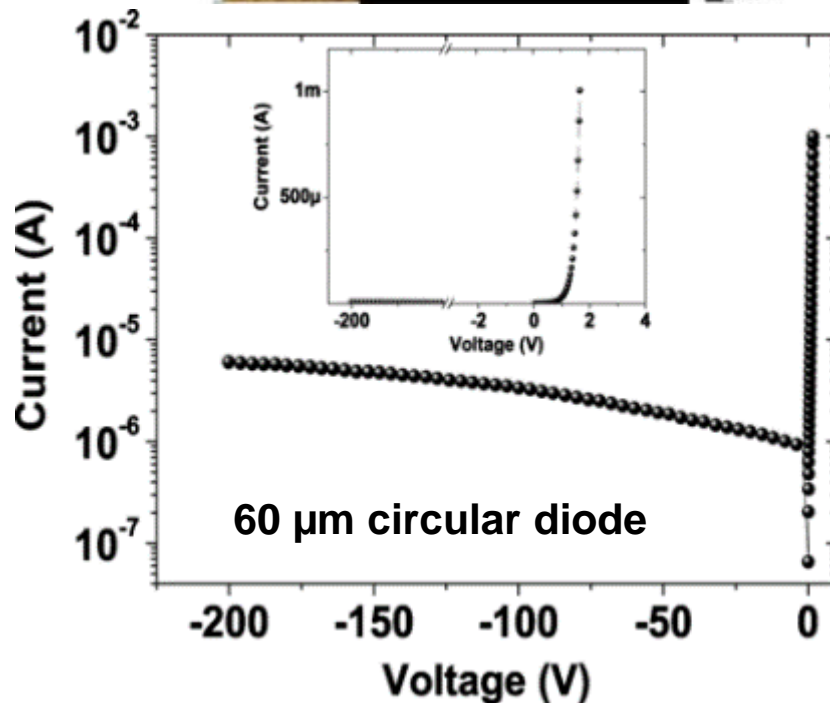
- Leakage through / on top of the ultrathin barrier
- Leakage following extra PECVD SiN passivation
- Leakage due to punch-through effects (electron injection into the buffer)
- Trapping effects: surface close to the 2DEG



# Low gate leakage through only 3 nm AlN barrier

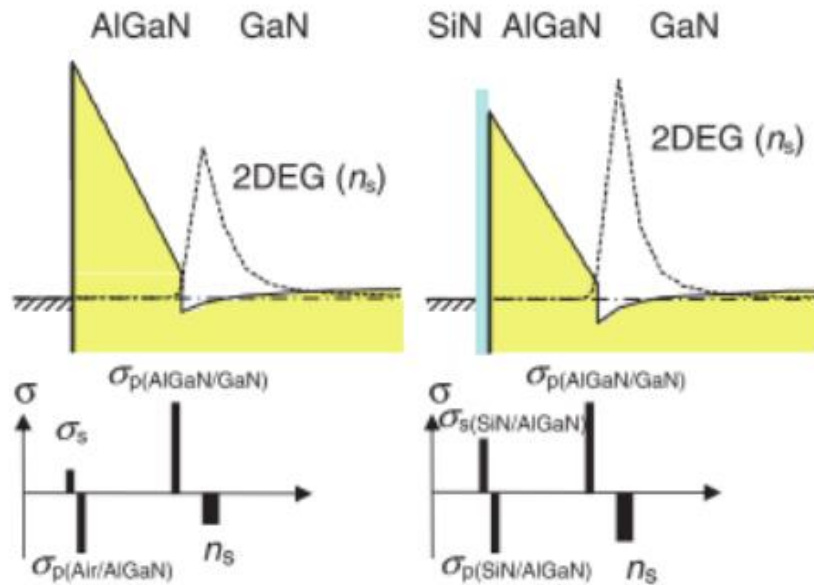


- High surface quality owing to the in-situ SiN preventing strain relaxation



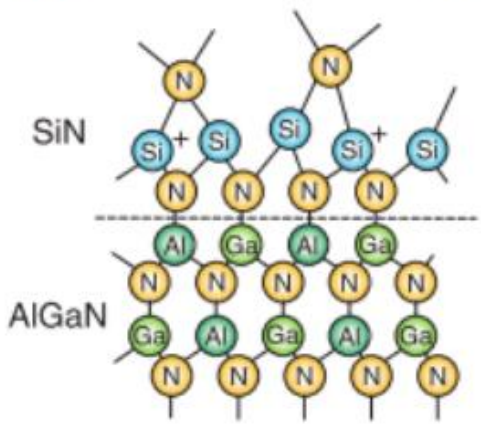
- Low Schottky gate leakage deposited directly on the AlN barrier layer (see forward diode)

# HEMT Surface Passivation with SiN



(a)

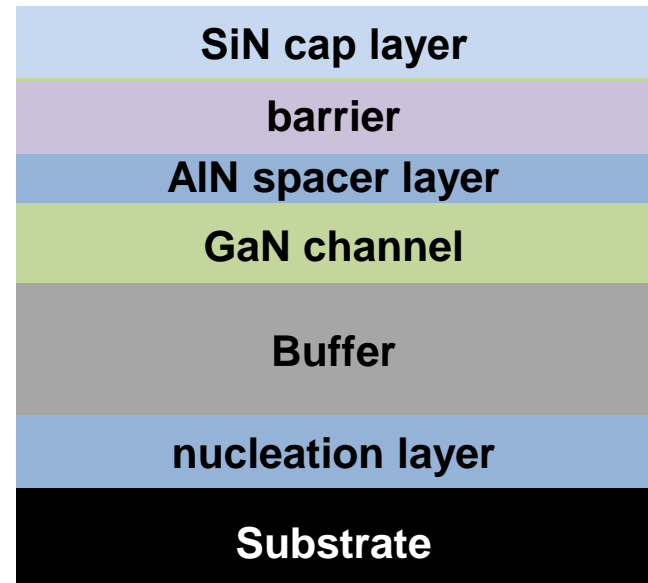
(b)



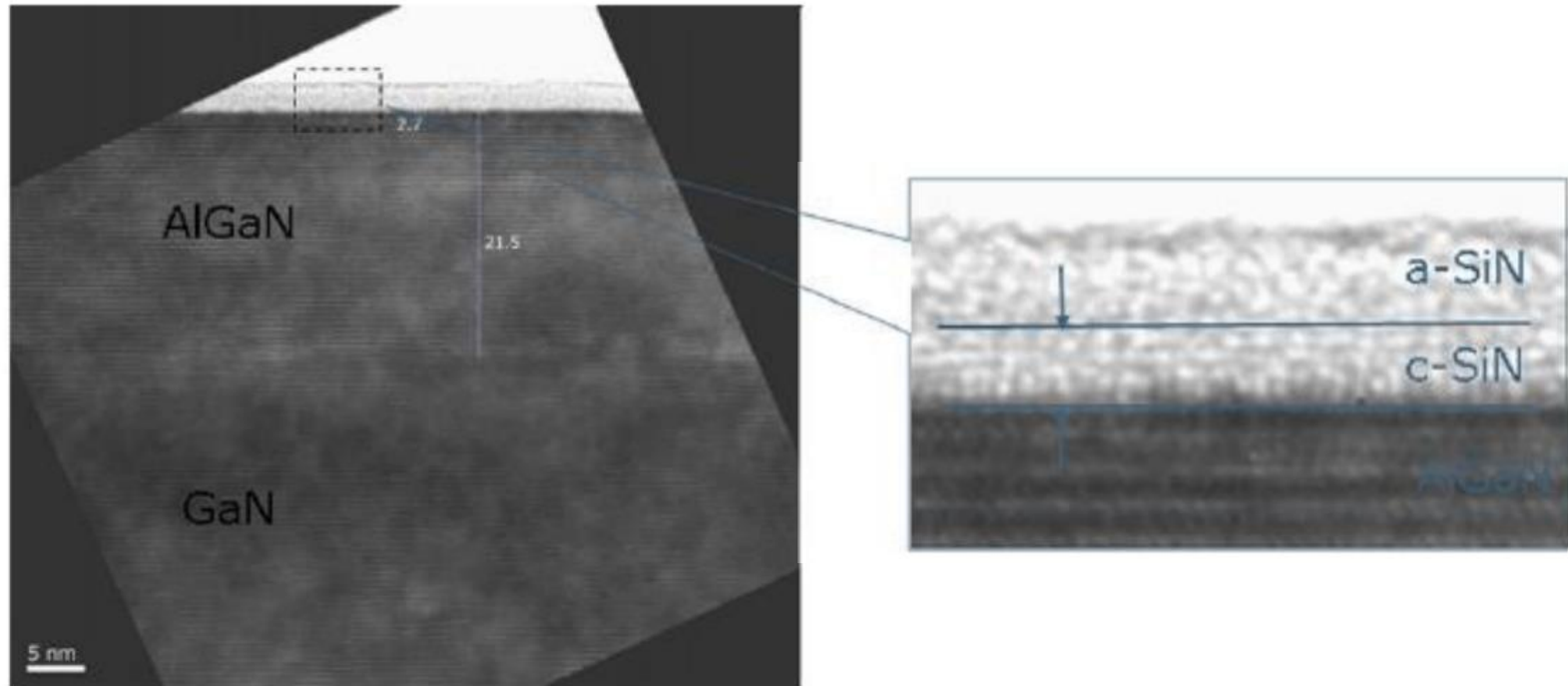
(c)

Atomic configuration matters !

Cleaning procedures for GaN are based on nitridation (N<sub>2</sub> plasmas, NH<sub>3</sub> plasmas, (NH<sub>4</sub>)<sub>2</sub>S, Thermal treatments in N<sub>2</sub> or NH<sub>3</sub>) + ex-situ SiN passivation



# HEMT Surface Passivation with in-situ SiN

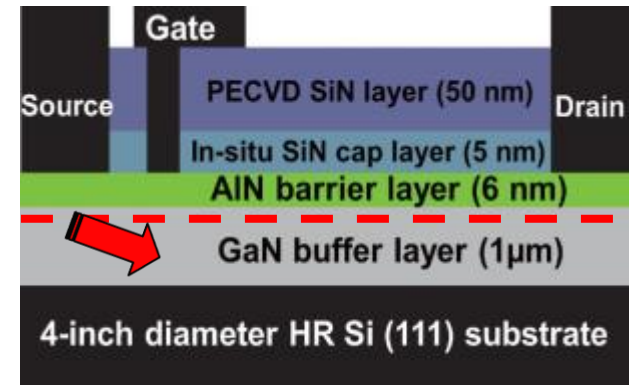
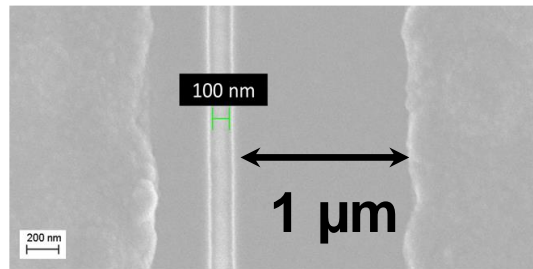
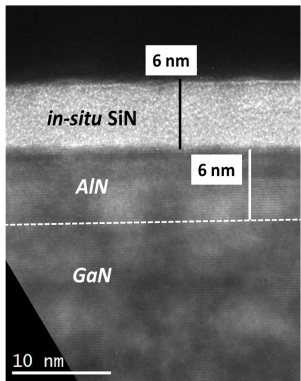


- SiN deposited in the MOCVD tool
- clean interface
  - crystalline interface
  - Relaxation prevention

# Buffer confinement for high voltage operation

What about high voltage operation when using ultrashort GaN devices?

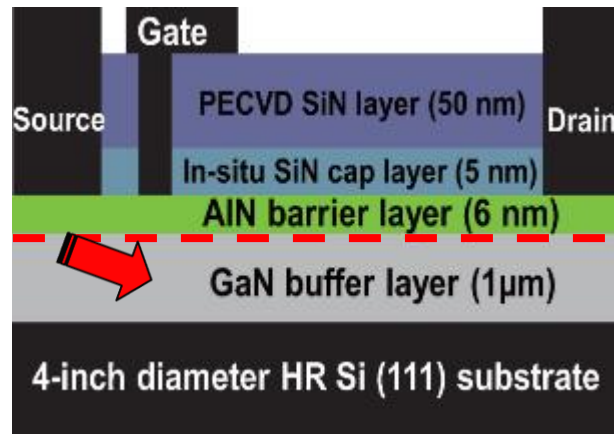
Ultrathin barrier + High  $N_s > 2 \times 10^{13} \text{ cm}^{-2}$  + Short  $L_{GD} \text{ \& } L_G$  +  $V_{DS} > 20 \text{ V}$  = Extremely high electric field



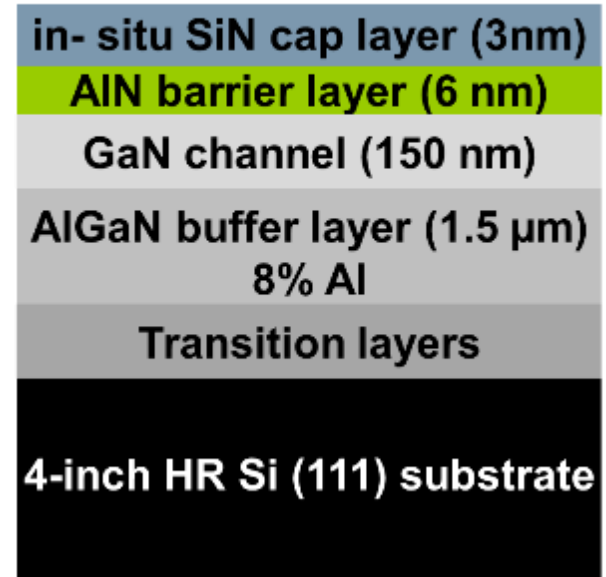
Poor electron confinement can be expected even if the material and processing are of high quality

# Back barrier needed

**Punch-through effect: Poor electron confinement even if the material and processing are of high quality**



## DHFET



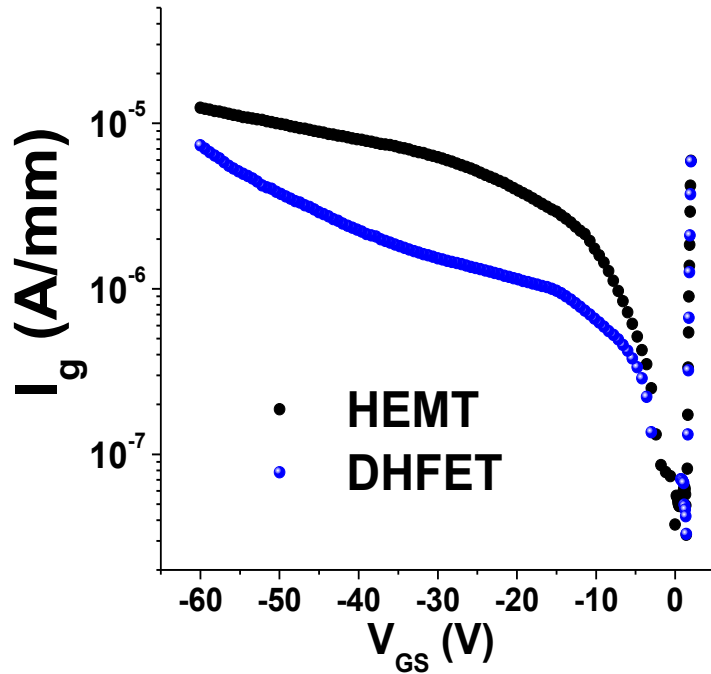
**Introduction of an AlGaN back barrier to prevent the electron injection under high bias (double heterostructure: DHFET)**



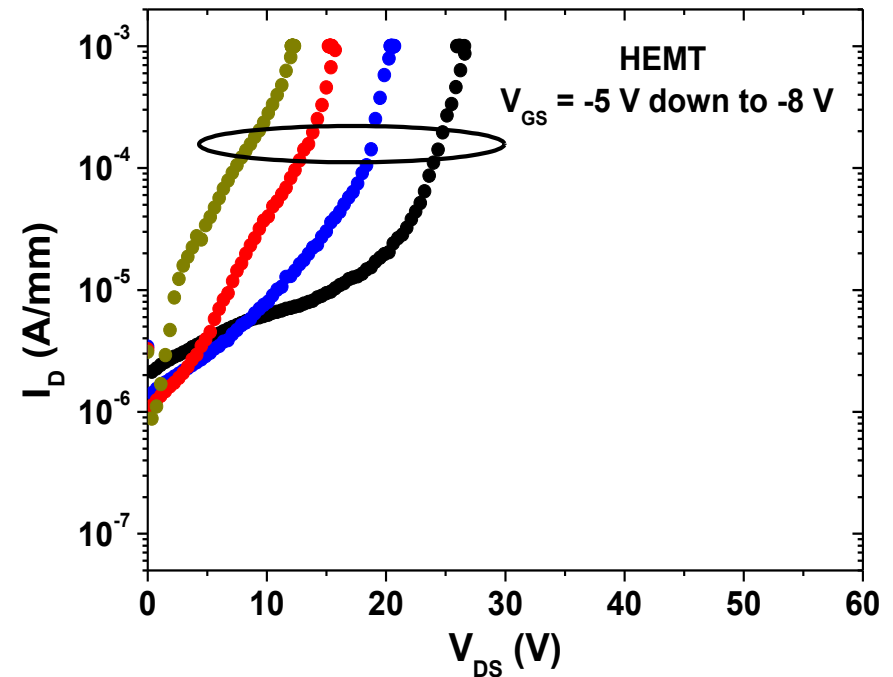
# AlN/GaN DHFET under high bias

$L_G = 200$  nm

Gate leakage current



3-terminal breakdown voltage

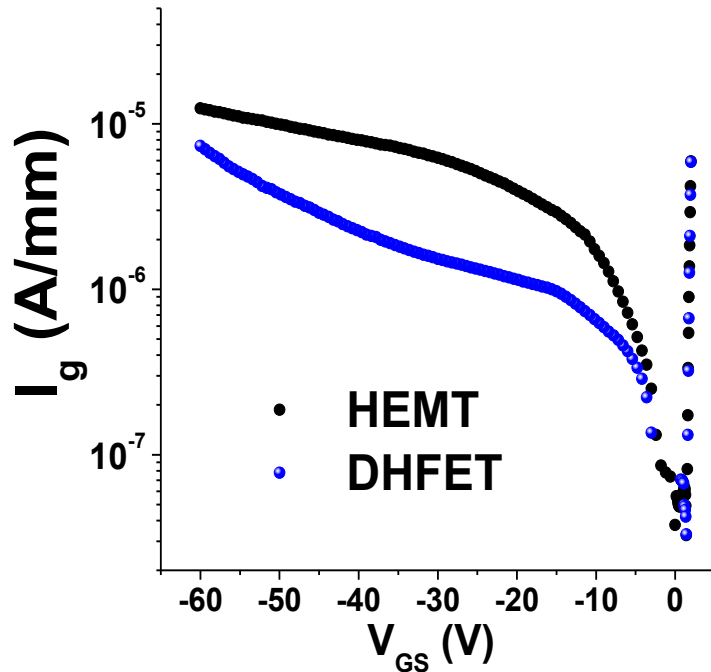


- Low Gate leakage current in both cases
- Huge drain leakage current: punch-through effect !

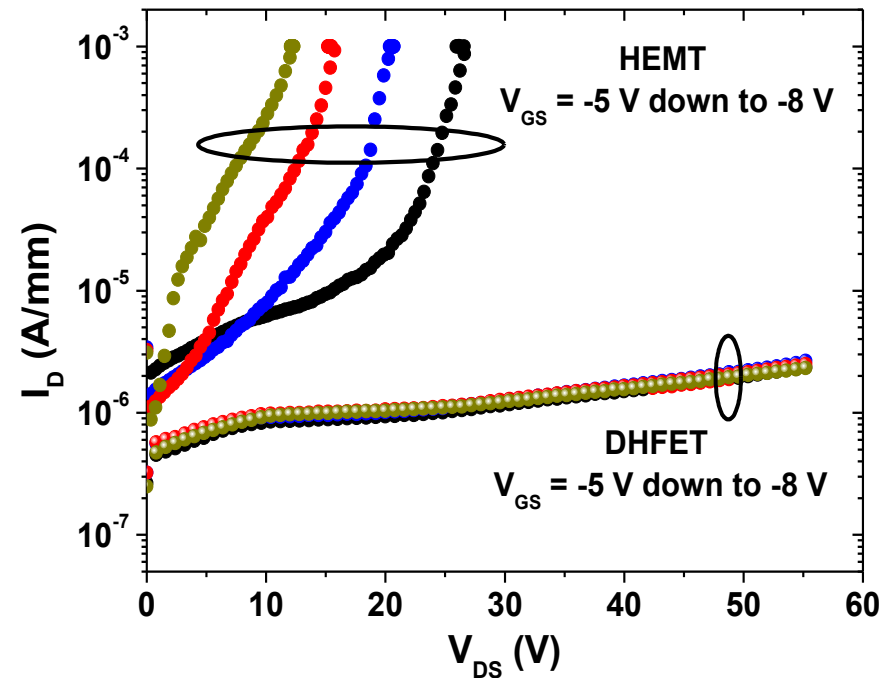
# AlN/GaN DHFET under high bias

$L_G = 200$  nm

Gate leakage current



3-terminal breakdown voltage

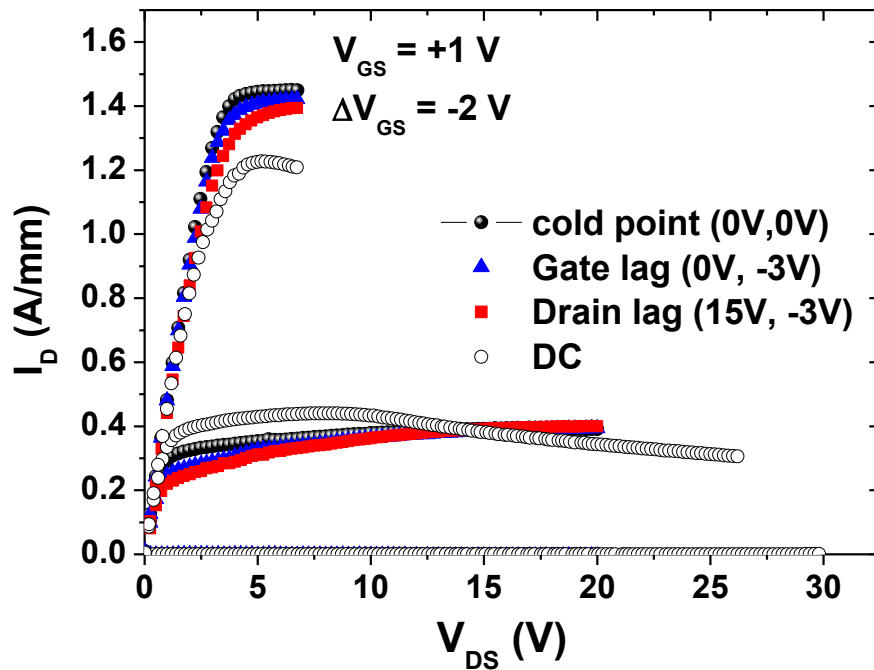


- Low Gate leakage current in both cases
- Low drain leakage: punch-through effect significantly reduced resulting in high  $V_{BK}$  ( $2 \mu\text{A/mm}$  @  $V_{DS} = 50$  V)

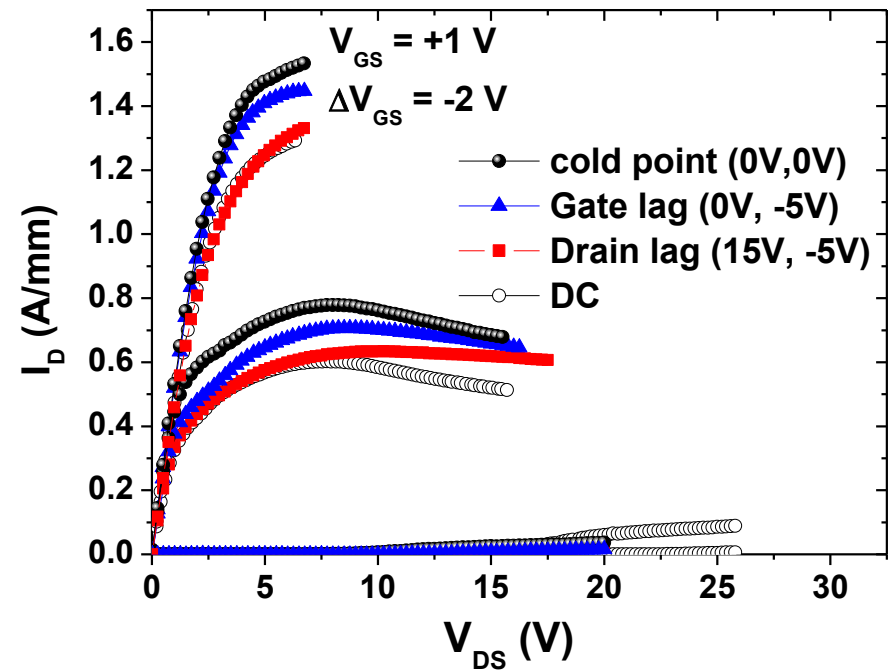
# Improved dynamic behavior in short GaN devices

AlN/GaN devices using a critical SiN cap thickness  
( $L_G$  down to sub-100 nm)

DHFET:  $L_g = 200$  nm

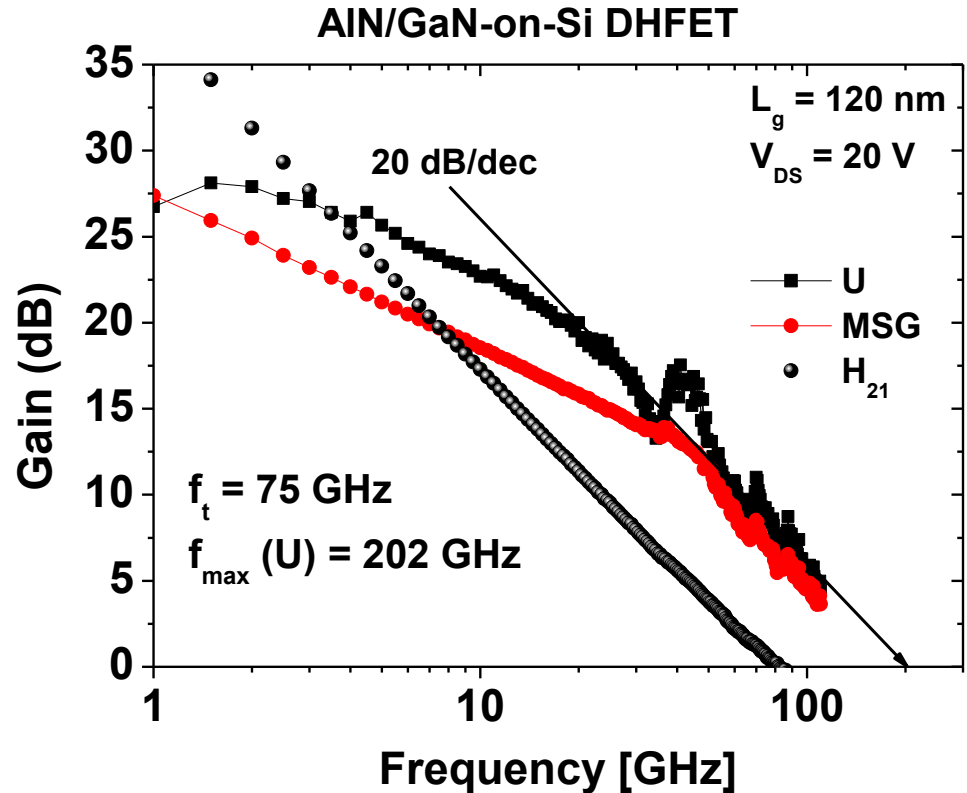
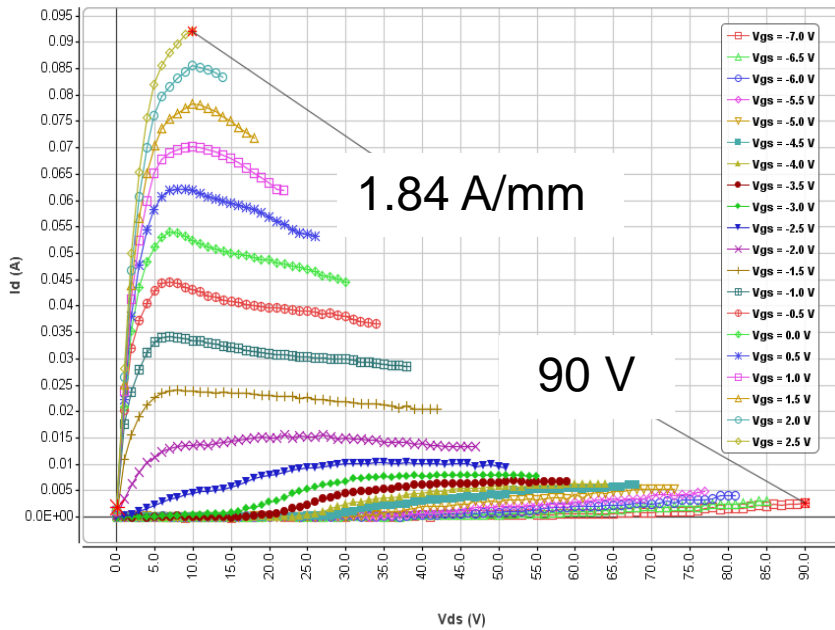


DHFET:  $L_g = 80$  nm



- Low trapping effects under 500 ns pulse width in highly scaled AlN/GaN devices

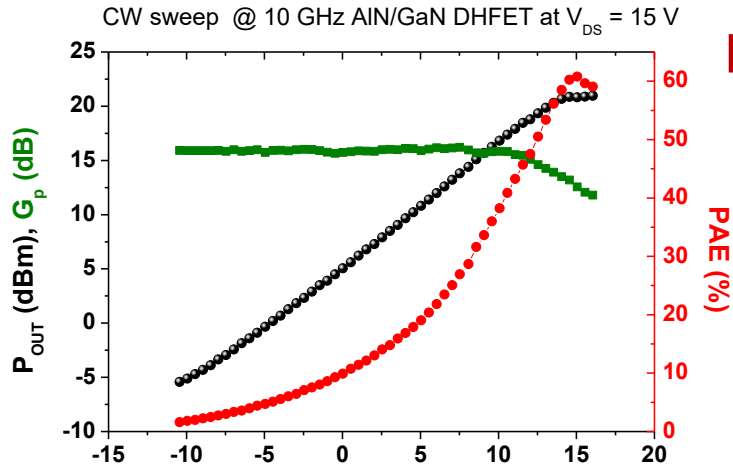
# High combination: $f_{\max} \times V_{\text{BK}}$



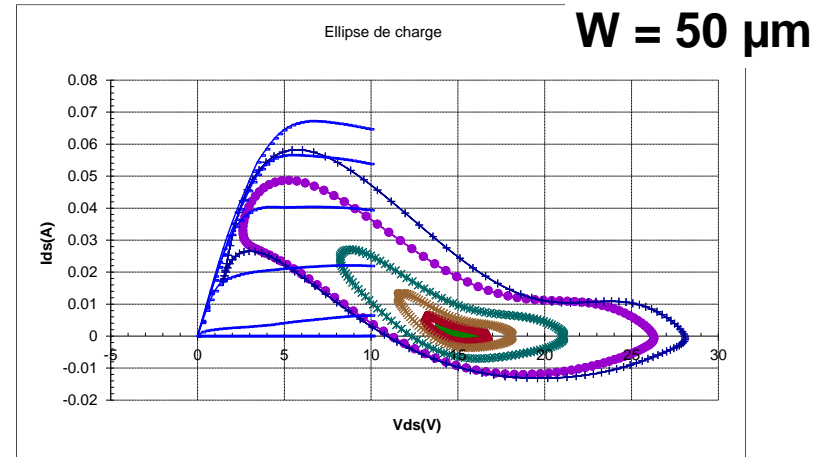
Fully reproducible devices delivering both high breakdown and high  $f_{\max}$

# 0.15 $\mu\text{m}$ AlN/GaN-on-SiC power measurement @ 10 and 18 GHz

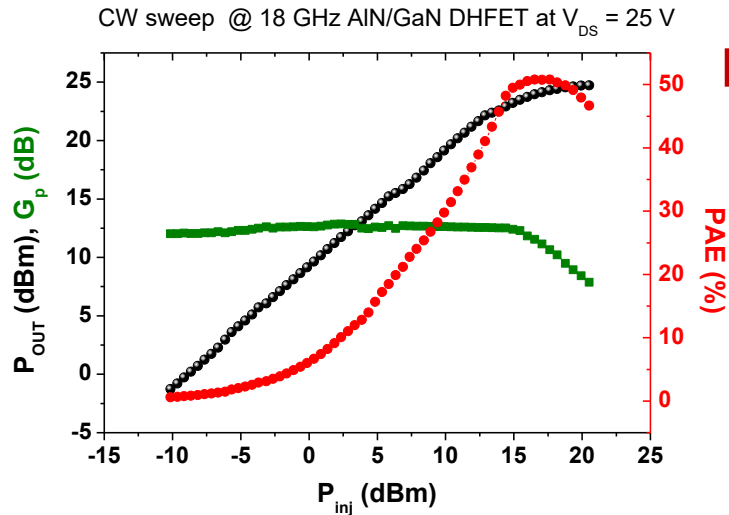
## 4 nm barrier thickness !



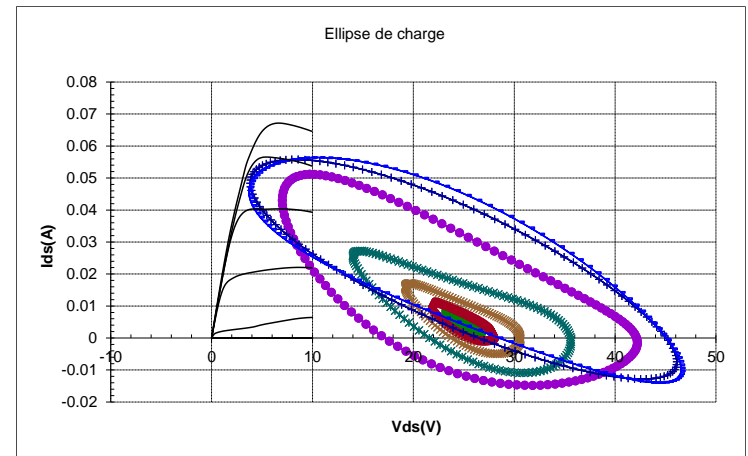
**PAE > 60%  
@ 10 GHz**



Load lines reflect the low RF dispersion  
The power gain confirms the high frequency performances



**PAE > 50%  
@ 18 GHz**



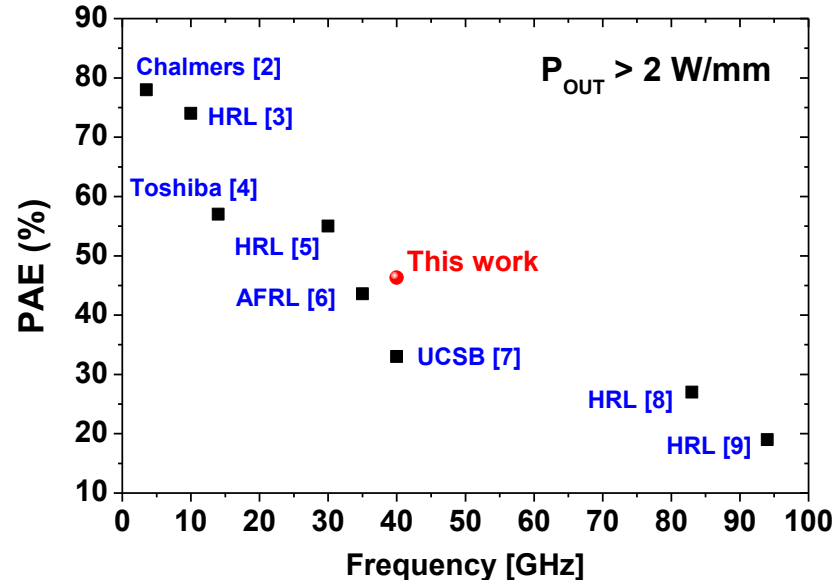
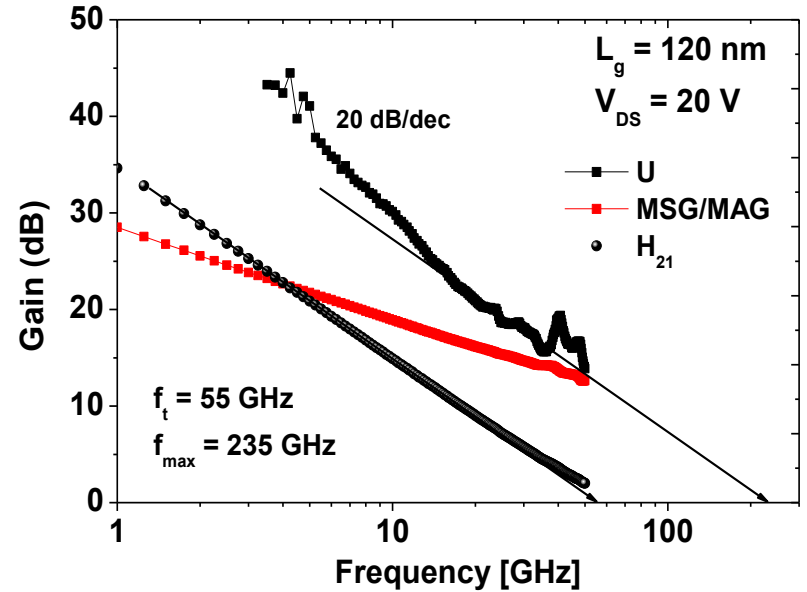
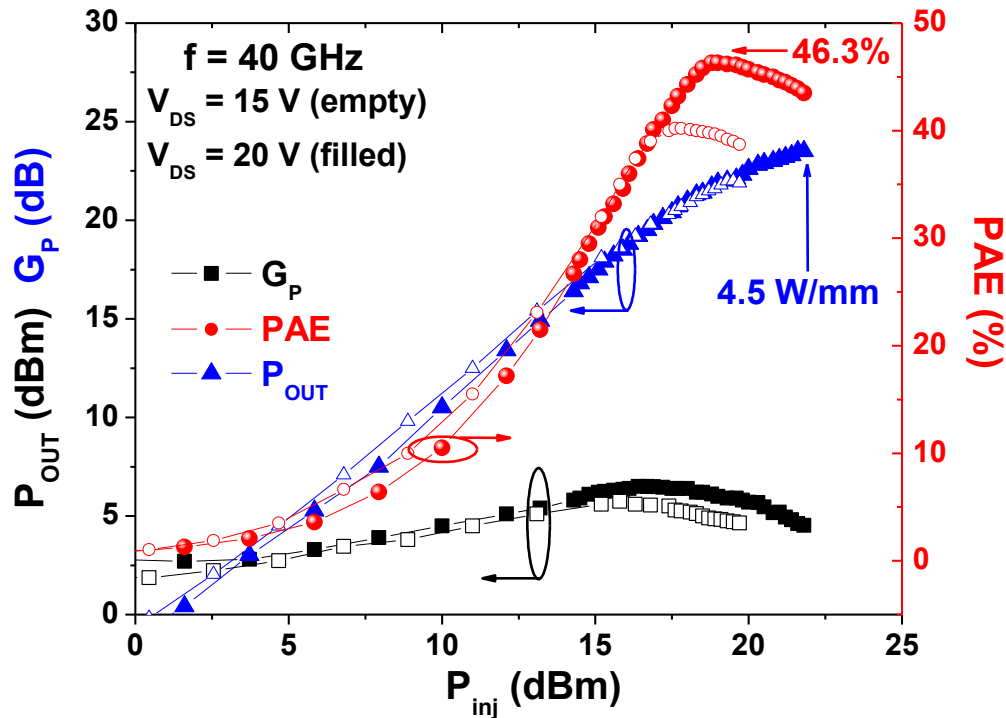
High PAE for the first time on sub-10 nm barrier GaN devices



# 0.12 $\mu\text{m}$ AlN/GaN-on-SiC DHFET @ 40 GHz

Barrier thickness of 4 nm

CW



State-of-the-art PAE @ 40 GHz  
for GaN devices

# 600 hours preliminary reliability assessment

Performed at the University of PADOVA

- ❖ AlN/GaN-on-Si DHFET capped with in-situ SiN ( $L_g = 100$  nm)
- ❖  $V_{DS} = 20$  V &  $V_{GS} = -7$  V (deep pinch-off) for 600 hours

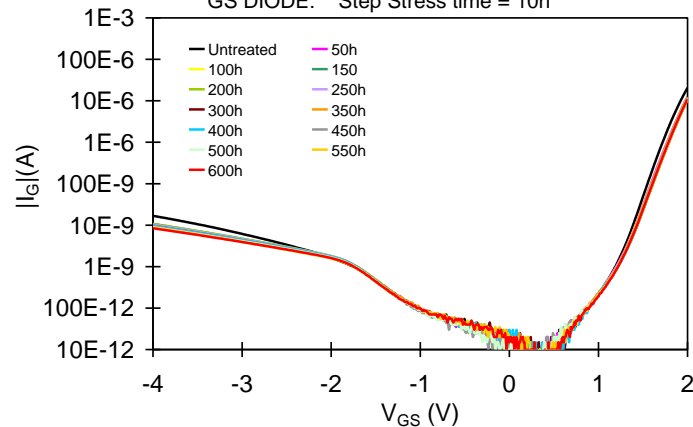


ME-LAB,  
DEPARTMENT OF  
INFORMATION  
ENGINEERING  
UNIVERSITY OF PADOVA

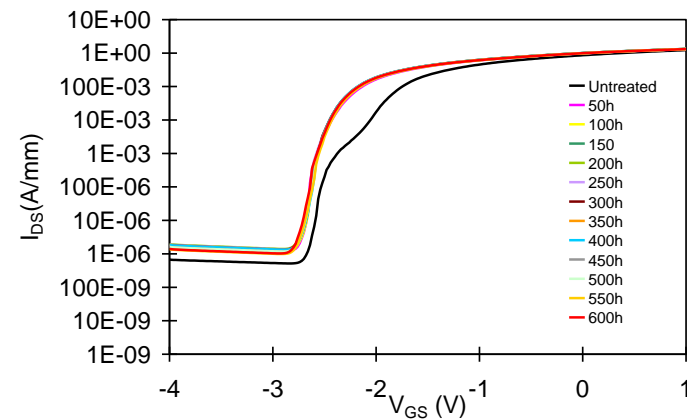


G. Meneghesso *et al*, TDMR, 13, 2013

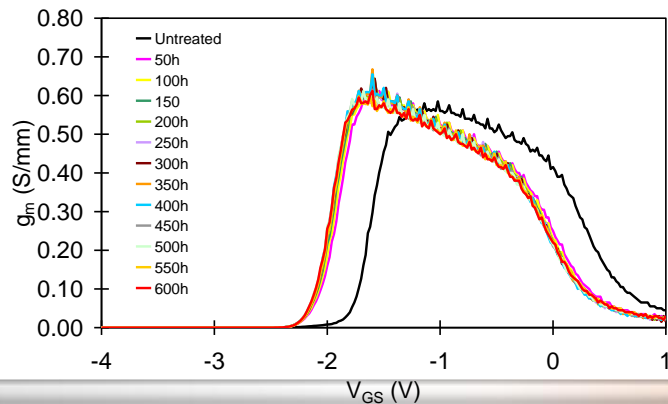
IEMN 1981 A1 2x25um\_0.1x3 DCstress @  $V_D=20$ V  $V_G=-7$ V  
GS DIODE: Step Stress time = 10h



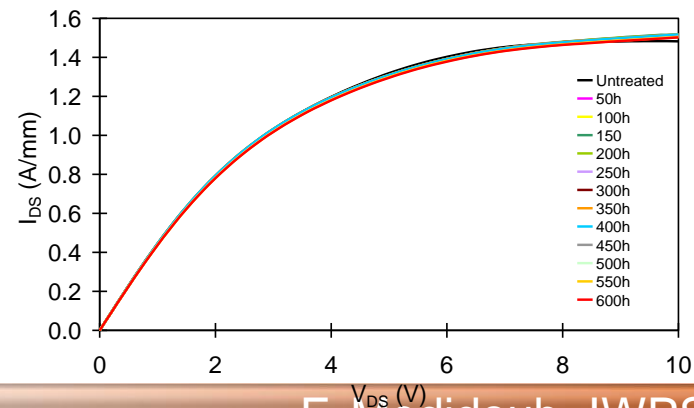
IEMN 1981 A1 2x25um\_0.1x3 DCstress @  $V_D=20$ V  $V_G=-7$ V  
 $I_D - V_G$ :  $V_{DS} = 20$ V Step Stress time = 10h



IEMN 1981 A1 2x25um\_0.1x3 DCstress @  $V_D=20$ V  $V_G=-7$ V  
 $g_m$ :  $V_{DS} = 3$ V Step Stress time = 10h



IEMN 1981 A1 2x25um\_0.1x3 DCstress @  $V_D=20$ V  $V_G=-7$ V  
OUT:  $V_{GS} = 2$ V Step Stress time = 10h



Off-state test: not an issue up to high bias

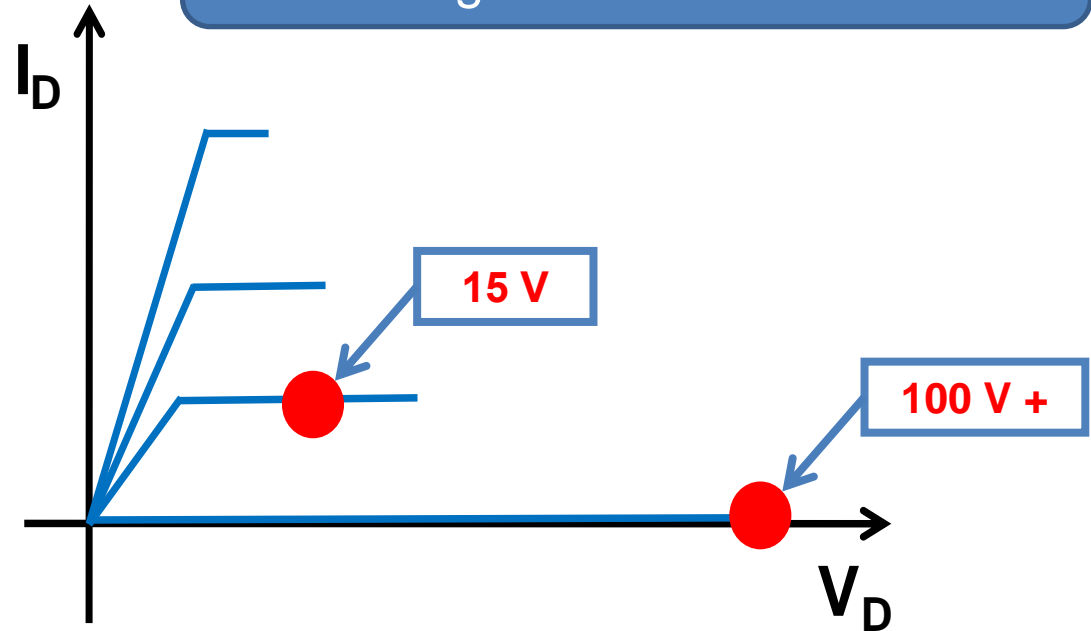
surface robustness enhancement owing to the in-situ SiN cap layer

Optimum electron confinement owing to the back barrier

$L_G = 150 \text{ nm}$

$GD = 2 \text{ }\mu\text{m}$

$f_{\text{max}} \geq 200 \text{ GHz}$



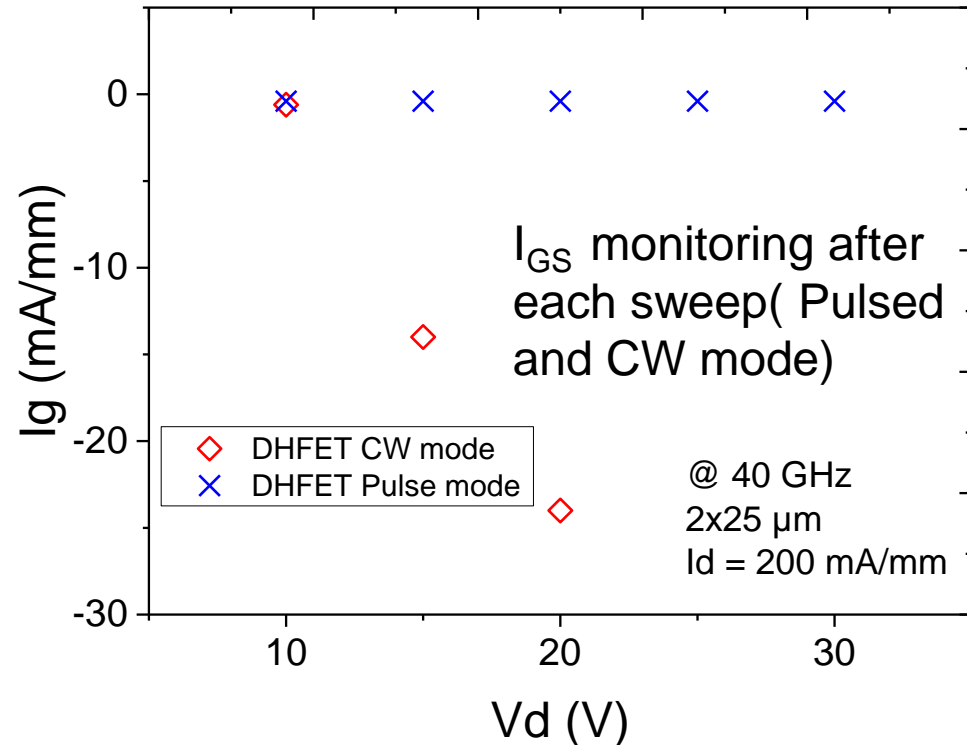
Thermally-limited in semi-on conditions for  $V_{DS} \approx 15$  to  $20 \text{ V}$

Poor thermal dissipation of the AlGaN back barrier

# Device robustness

- DHFET in CW mode
  - Strong degradation
- DHFET in Pulse mode
  - No degradation

***Pulsed mode reduces the self-heating effect in the transistor***

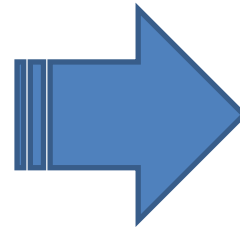
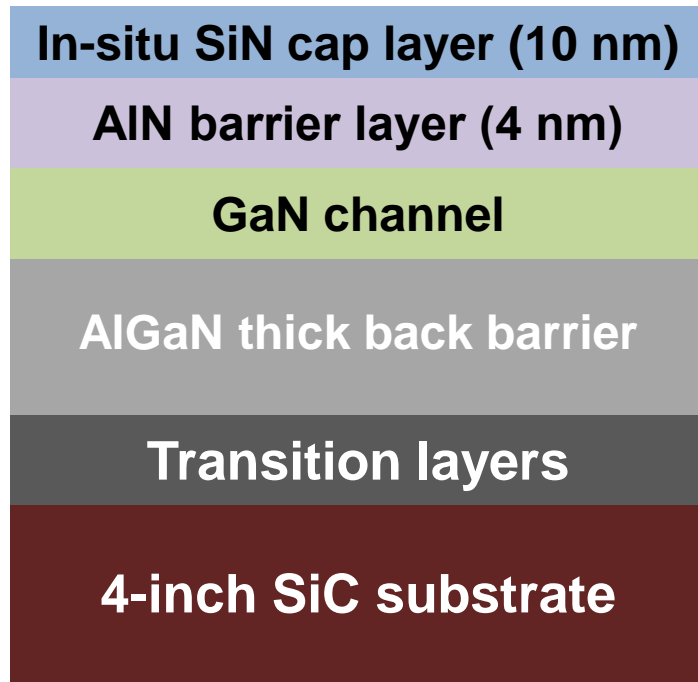


Degradation due to self heating resulting from the poor thermal dissipation of the thick AlGaN back barrier: DHFET not suitable for operation  $> 15 \text{ V}$

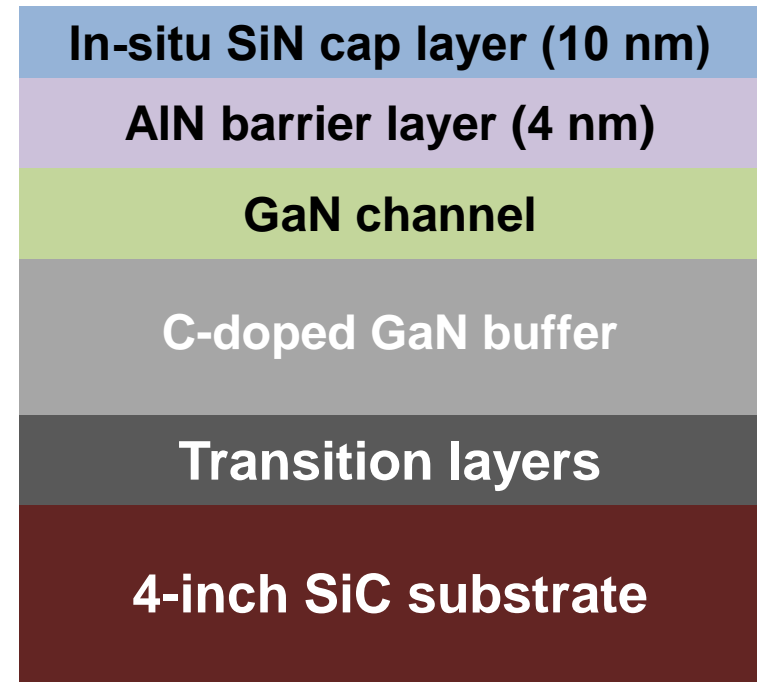
For short GaN devices, it seems that hot electron is one of the prime factor degrading the reliability.

# Change in the buffer layers: From AlN/GaN DHFET to C-doped HEMT

## DHFET



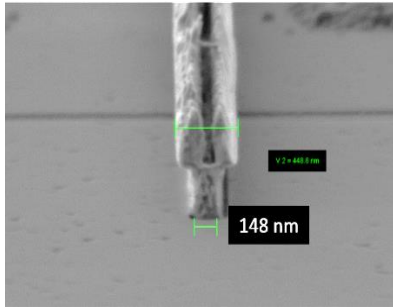
## HEMT



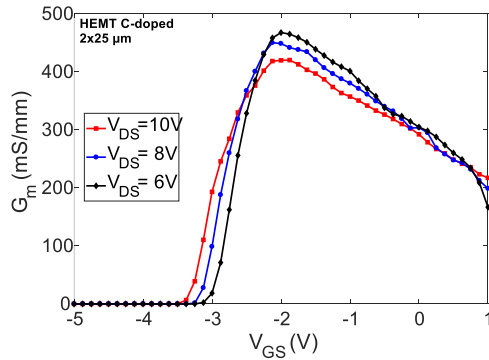
Much better thermal dissipation expected in HEMT configuration but what about electron confinement and RF power performances



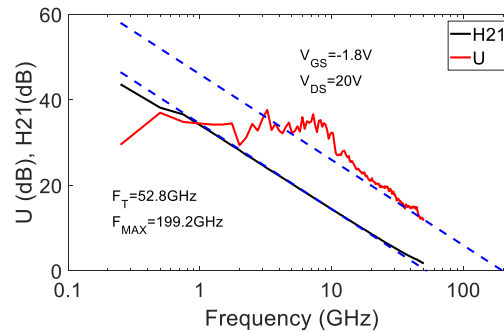
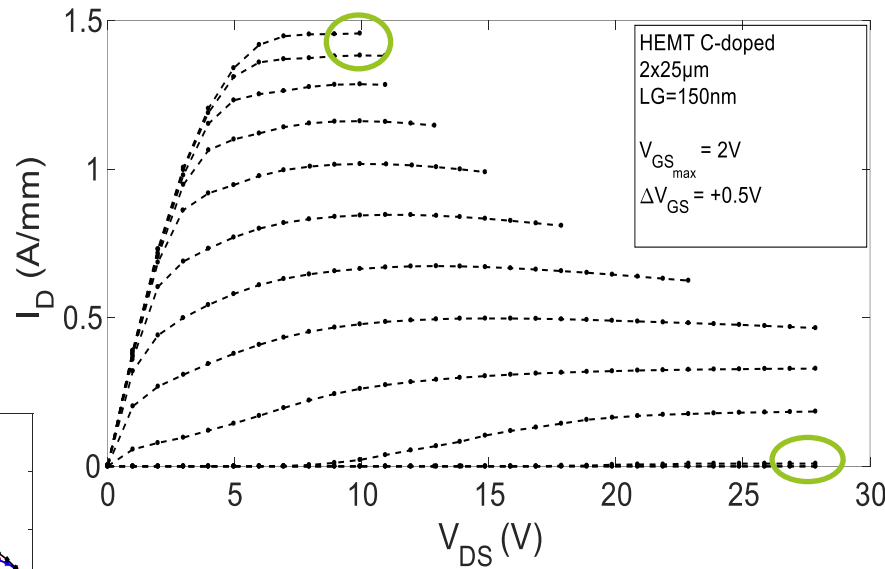
# DC Characteristics of AlN/GaN C-doped HEMT



$L_g = 150$

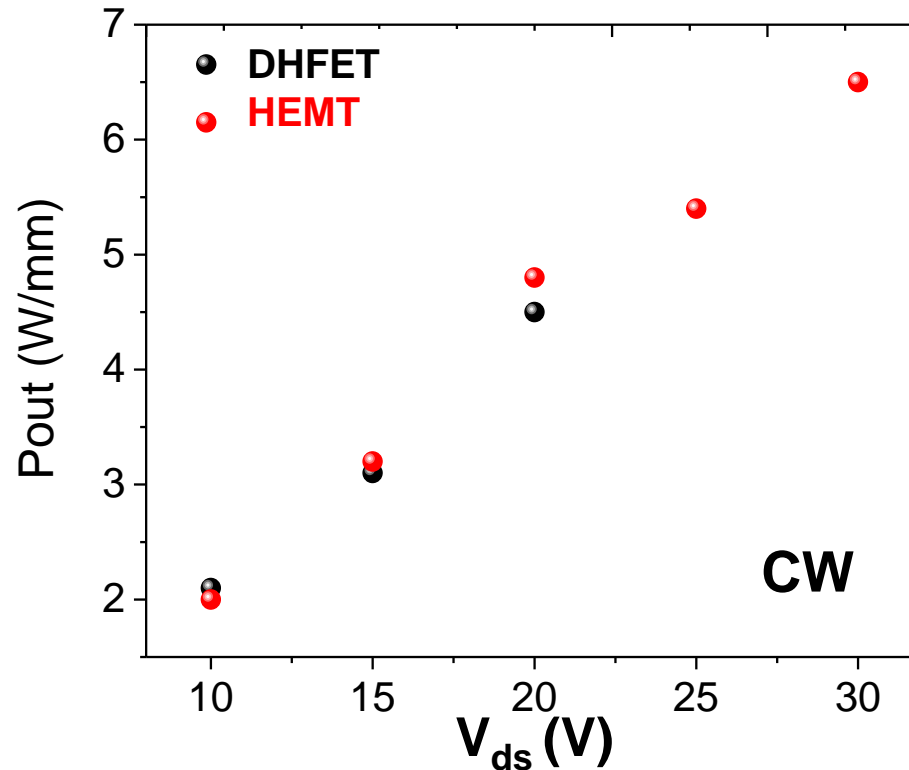


450 mS/mm @  $V_{DS} = 10V$   
High  $G_m$  due to the gate length + barrier thickness



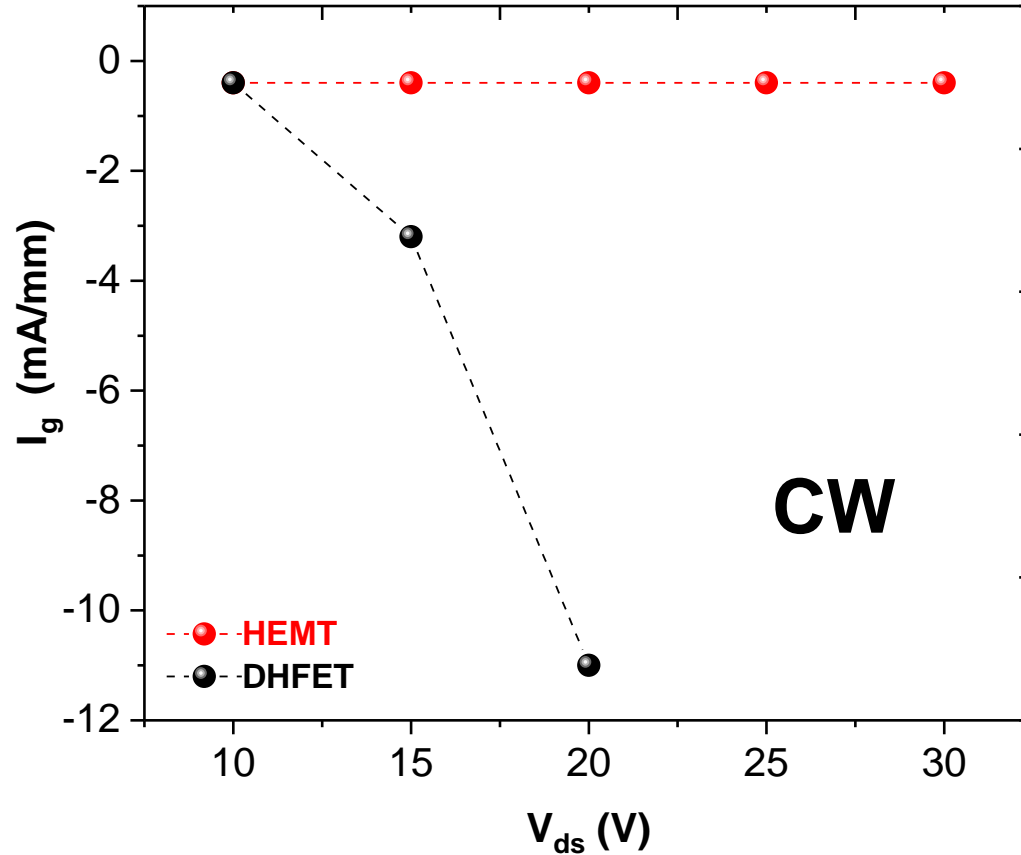
- **1.4 A/mm @  $V_{GS} = 2V$**   
**High current density**  
**owing to high  $N_s$**
- **Low leakage current**  
**(<1  $\mu A/mm$ )**
- **High electronic**  
**confinement**
- **High frequency**  
**performance**  
 $F_T = 60GHz / F_{MAX} = 200GHz$
- **Operation bias up to**  
**30V with high gain @**  
**40 GHz**

# AlN/GaN DHFET and HEMT Comparison



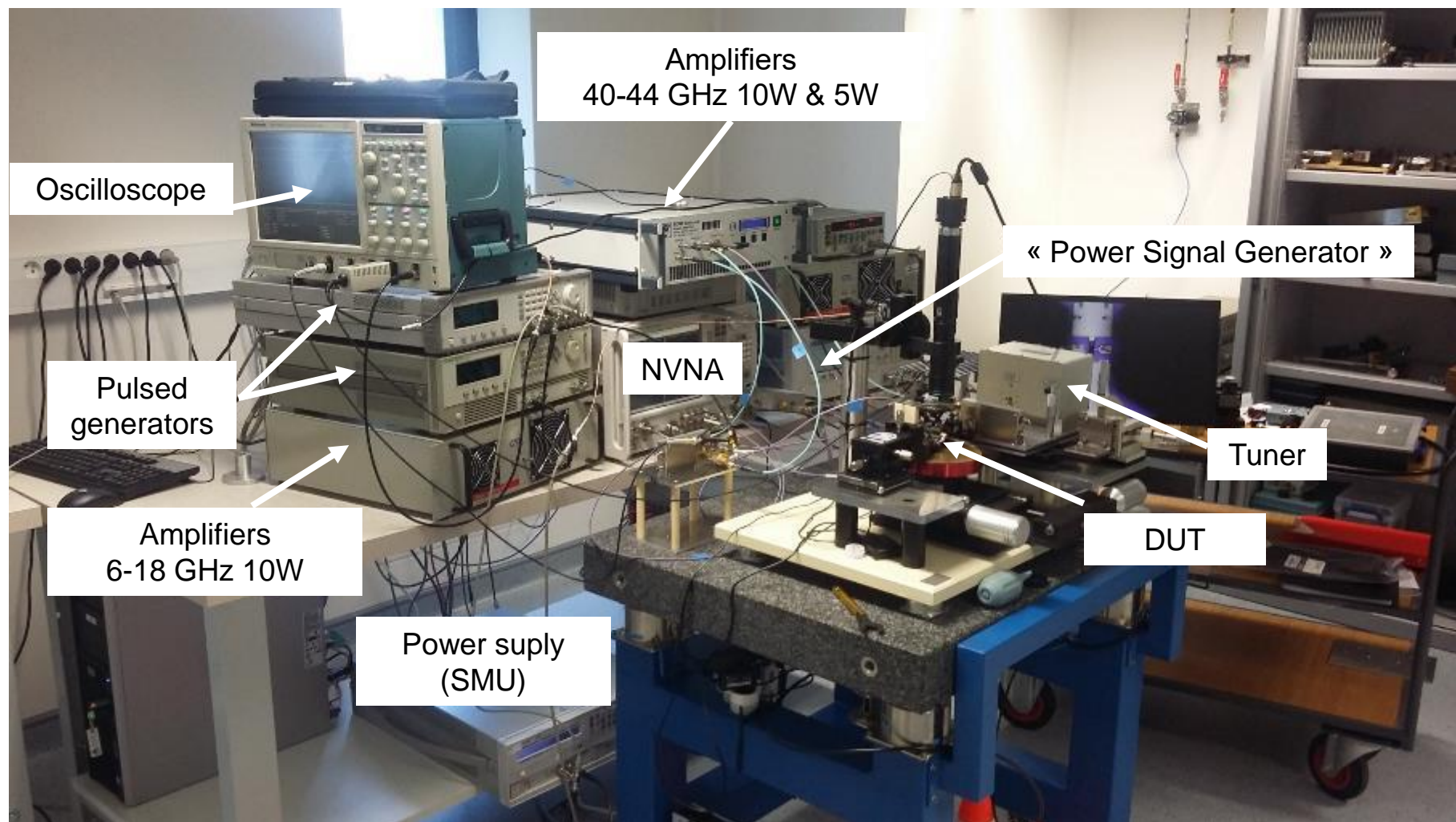
Linear evolution of  $P_{out}$  for both structures  
Possibility to drive the C-doped HEMTs at much higher bias

# Robustness : DHFET vs HEMT

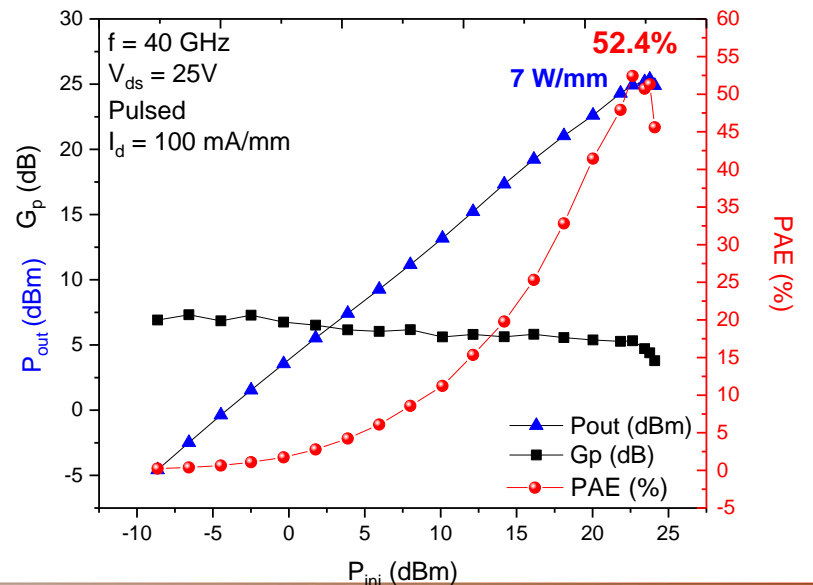
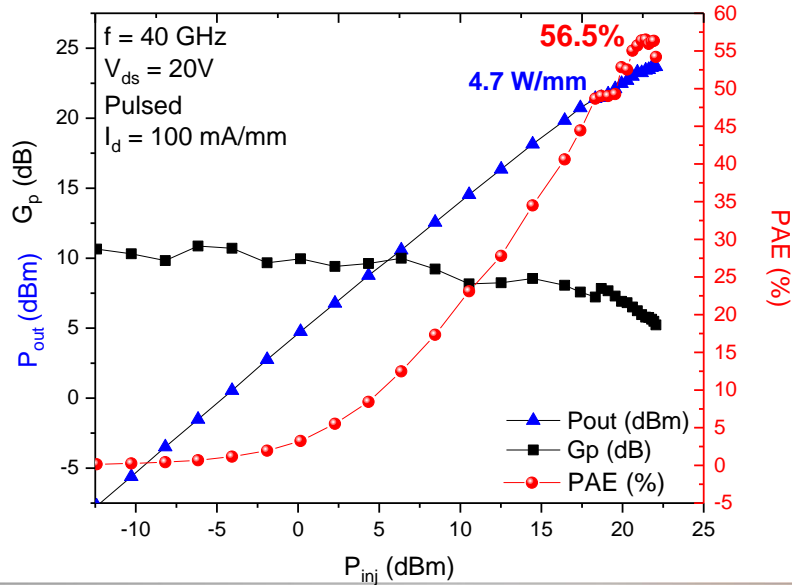
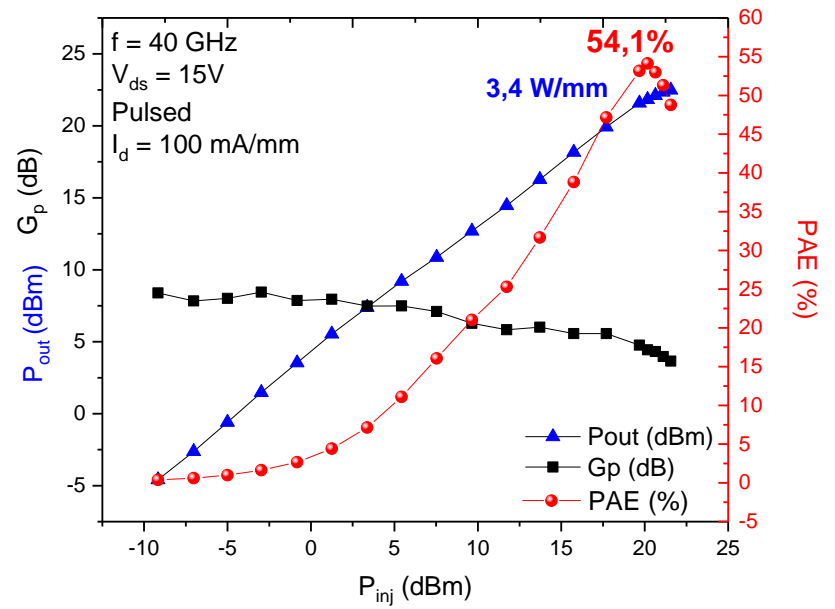
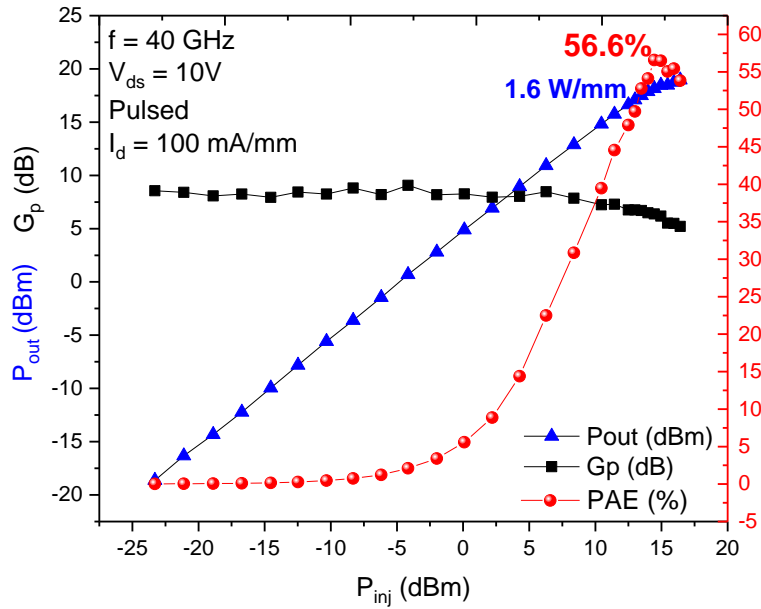


C-doped AlN/GaN HEMT promising for Q band + applications

# Specific bench for LoadPull high power measurements up to 40 GHz both CW and pulsed

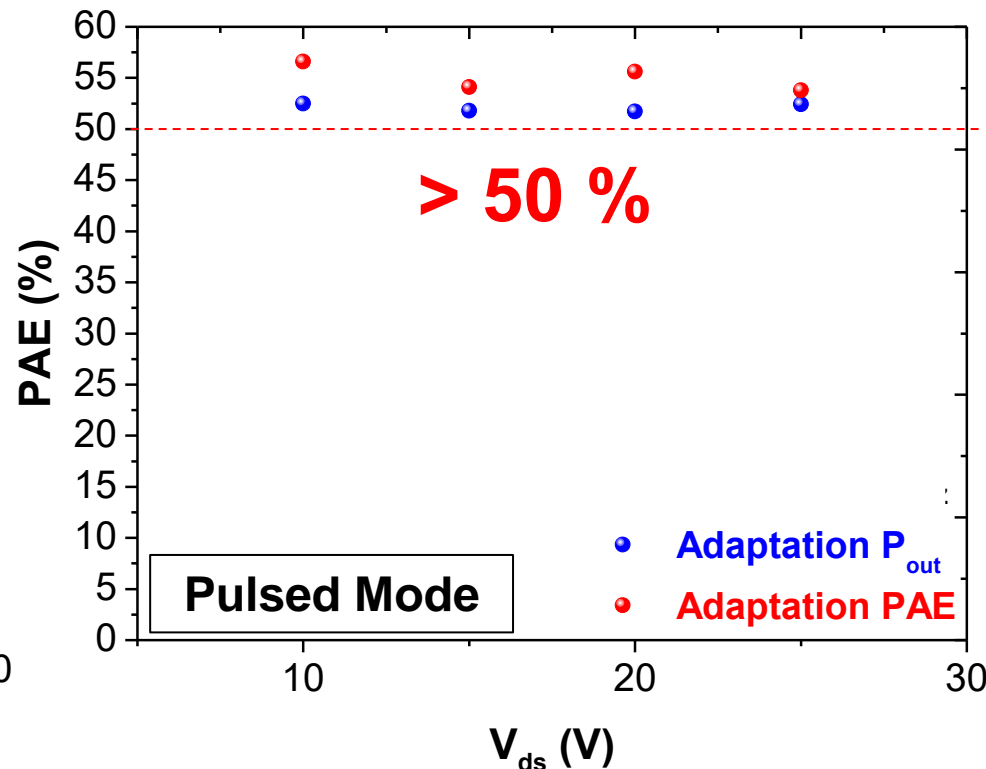
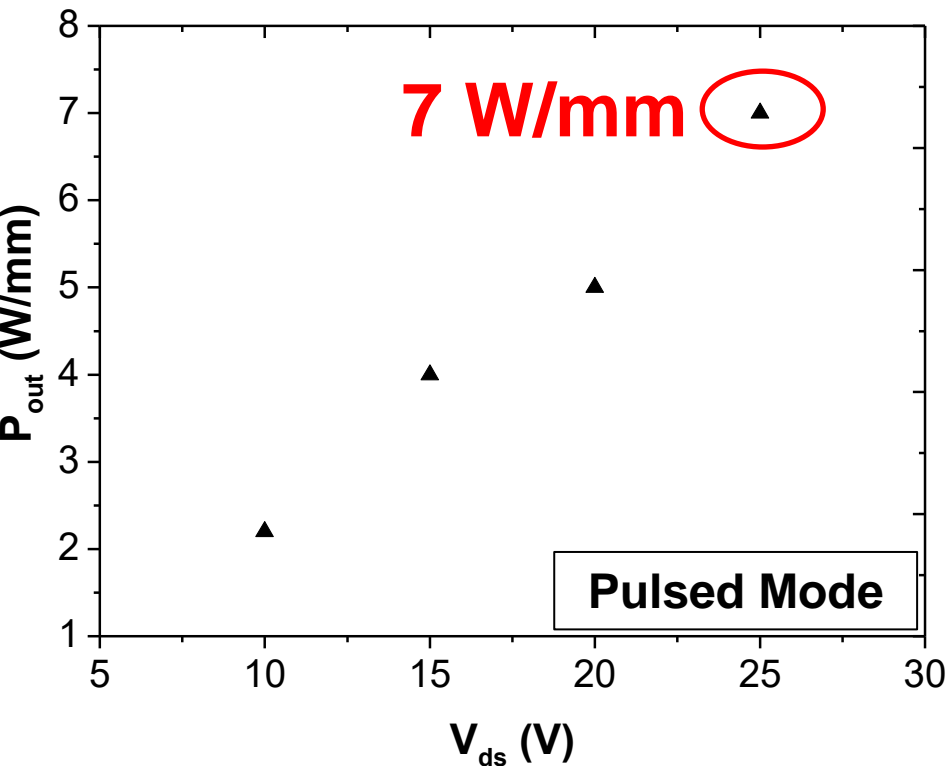


# Pulsed power of 0.12 $\mu\text{m}$ C-doped AlN/GaN HEMTs



# Pulsed power / PAE @ 40 GHz C-doped AlN/GaN HEMT

$L_G = 120$  nm



\*Record PAE (56%) et  $P_{out}$ /PAE combination 52% / 7W/mm @ 40 GHz confirming the potential of this structure.

*Unpublished results*



# Conclusion

- Possibility to achieve high breakdown (close to 100 V/ $\mu\text{m}$ ) under high electric field, with low leakage, and high PAE while using highly scaled sub-10 nm barrier GaN devices
- A critical in-situ SiN cap layer is helpful to mitigate leakage current and enhance the device performance and robustness
- Buffer configuration is a key to achieve GaN mmW device with both high efficiency and high robustness under high bias

**Initial results on AlN/GaN C-doped HEMTs show a record combination of  $P_{\text{OUT}} > 7 \text{ W/mm}$  together with PAE  $> 50\%$  in pulsed mode @ 40 GHz**

