Contribution to Health Monitoring of Silicon Carbide MOSFET

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Abstract. Power converters' usage is expanding ever in industrial ap- plications as they provide flexibility, high level of performances and new functionalities. However, with increased complexity come new constraints with respect to reliability. This chapter covers a study on reliability of a lab-scale power electronic module taken here as a vehicle. The downsizing of converters and new application-related operating constraints are accompanied by an increase in current density. The use of Silicon Car- bide wide-gap technology in power modules is therefore attracting but remains a challenge because this technology is not yet mature and does not benefit from the deep knowledge established about Silicon counter- part. Therefore, health monitoring has naturally emerged as an effective way to implement a reliability assessment. After a brief description of the expected failure modes, an experimental failure monitoring bench will be presented. The choice and implementation of failure indicators through a classification using a neural network will be discussed and presented.

Keywords: MOSFET SiC, health monitoring, classification, neural net- work

1 Introduction

In the context of more electric mobility, many projects have focused the more electric aircraft [1]. The aim is to gradually replace hydraulic transmission systems by equivalent electric actuators for environmental, maintainability and compactness constraints even if the reliability of power electronic systems under harsh operating conditions are far from the one of traditional power equipment [2]. The electrical actuators will be integrated into more powerful and flexible electrical networks. The advantages of the transition to more electric infrastructure are multiple. Electrical systems are supposedly more compact and lighter for a same level of power. They are also easily controllable and offer better immediate security. They are considered as more reliable for several reasons: their small size and properties allow for safer and simpler redundancy and their maintenance level is less restrictive than the one of hydraulic and pneumatic systems. There- fore, the reliability of a complete system is linked to its complexity. However, the electronic supply of electromagnetic actuators could bring some weaknesses to the whole system, especially in harsh environment (high temperature, vibration,...). Some applications such as avionic do require a high level of reliability and an assessment is mandatory.

Thus, monitoring of electric actuators is considered as essential in a large number of publications. Since power converters are directly connected to these actuators, their reliability is an important issue. Converters are key components in many applications but are also responsible for failures [3]. The power module is the core of a converter generally speaking. For the sake of power density, so-called planar power modules are preferred. The geometry of a planar module as well as the assembly of technologies render difficult the access to the temperature map or the power losses. It is the essential difference with an electro-mechanical sys- tem as an example, where successful monitoring approaches have been reported mainly because the observation of failure-related signals is possible. Practically a rainflow approach [4] is mostly considered when performing the

monitoring in an actual power electronic system. The rainflow is feeded by power losses computation and, thus, junction temperature estimations. Even if successfully demonstrated, the approach requires some calibration and many tests to obtain the evaluation of number of cycles before failure according to a targeted junction temperature, thermal excursion and cycle time or some ageing laws [5][6]. Other approaches are based on the extrapolation of time-series built from thermal sensitive parameters [7]. This kind of approach seems less expensive to implement and will be preferred here.

Most of the publications concerning the SiC [1] components focus on-chip performances and are made in laboratory conditions. The SiC technology behavior being quite different from the previous one (Si), the well-known results about Silicon MOSFET may not be translated. We propose, in this chapter, to study as many failure mechanisms as possible from the chip to the interconnections in- side a lab-scale module taken as a demonstrative vehicle. The module considered here is innovative in terms of technology. A special attention has been taken for its compactness and power density. Consequently, no model is available for this device. Therefore, the experimental approach through accelerated testing has been adopted in order to characterize its behaviour under different stresses. As a result, high stress cycles of operation are implemented to accelerate the ageing process [8]. Unfortunately, this approach generates a large amount of data because the ageing conditions must be various allowing an extrapolation of the consumed lifetime or the RUL[2] [9][10][11]. It must also be ensured that they do not address the same defects. The literature shows that the estimation of the junction temperature is recommended as it can be considered a relevant indicator [12][13][14][15][16]. But its evaluation must be done indirectly by monitoring sensitive electrical parameters (TSEP). Therefore, their analysis should be car- ried out and then failure modes should be identified against the selected TSEPs. In a first step, a database is created, producing about fifty potential indicators, representative of a fault or not.

A composite failure signature is built in order to follow the evolution of the defects in a classification space where the different areas will define some intervals of lifespan. The signature is naturally composed of failure indicators that will be selected through a systematic selection method to ensure the best sensitivity in terms of signature variation according to ageing while reducing the complexity and redundancy of the required information. A learning phase has been realized using 6 modules in order to create 4 classes as follow: healthy state, 30% of the lifespan (already over), 60% of the lifespan (already over) and end of the lifespan (nearby).

We first present below an overview of the expected failure modes and faults. Then, we discuss the accelerating process with the description of the test bench for the ageing process and the active power cycling test. Conclusively, knowing that signatures are generated, we suggest the monitoring of selected best sensitive signatures to establish the percentage of life elapsed using a neural network [17].

2 Overview of expected failure modes and faults

In the literature, [18] indicates that based on a study of 200 products 34% of failures come from semiconductor and soldering failures in device modules while [19] implies that 38% of faults in variable-speed AC drives are due to failures inside power devices.

Furthermore, [20][21] highlight the fault character in power electronic converters. These are distributed, in order of importance, as follow:

- 30% for capacitors;
- 26% for printed circuit-board (PCB);
- 21% for semiconductor devices;
- 13% for solders;
- 3% for connectors and
- 7% for the rest.

According to another survey, [22] and [3] have shown that sources of stress distribution come from several conditions as follow:

- 55% are related strongly to temperature;
- 20% are related strongly to vibrations;
- 19% are related to humidity and moisture, and
- 6% are due to contaminants.

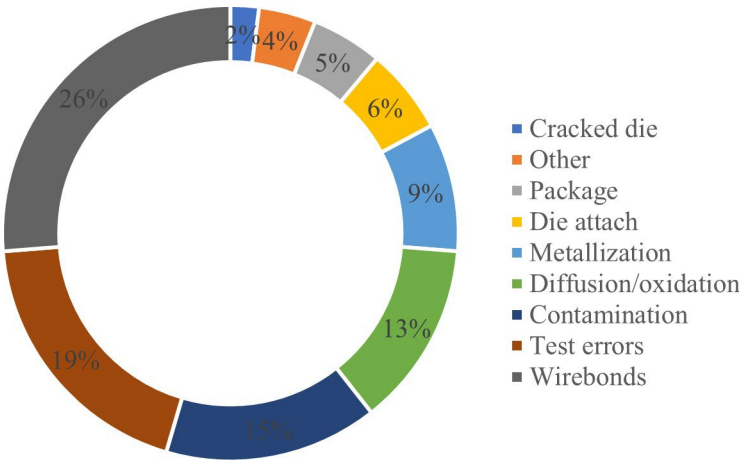

Fig. 1. Distribution of Failure modes [25]

Regardless of the technologies implemented in a power module (SiC, Si), the failure mechanisms are associated with the dices but not only. Indeed, the pack- aging takes a significant part. However, it depends on a multitude of parameters such as temperature, current level, voltage amplitude, switching frequency, etc., and the converter topology as mentioned in [23], [24]. [25] has shown that packaging induces failures during the module lifespan. The distribution of the different modes is shown in Fig. 1. For instance, wire bonds represent a significant part of failures (about 26%). They are followed by interconnection problems such as chip attachment and metallization (about 15%) and the package (about 5%). It should be noted that the contamination or diffusion aspects take a significant part in the failure modes (18%). However, the rate of test errors is unfortunately high (19%). The two main failure modes observed are:

- an open circuit: a conductive part is cracked or liftoff;
- a short circuit: an insulator is perforated or a conductive part has melted around an insulator to generate an electrical contact.

In any case, the most expected failure modes shown in Fig. 1 are:

- Bonding wires' liftoff or cracking [25], [26]
- Electromigration in connectors [25]
- Metalization reconstruction [27]
- Cracks in die attach [28], [29]
- Direct Bonded Copper cracking [26], [30]

Wire bond lift-off or cracking: Numerous studies have been conducted over the past decades on this type of fault because it was one of the most important. It is mainly due to the detachment of the bonding wire in a progressive mechanism.

Several phenomena can occur at the interface between the bond wire and the metalization of the upper pad. The first is observed when the metal of the bond wire and the metalization are dissimilar.

Electromigration in connectors*:* The power modules require metallic connection parts to connect the chips to the external connectors. These can undergo electromigration under high heat and high current conditions. Also this mechanism can lead to the creation of voids in the metallic conductors and consequently a local increase in resistivity. As a result, this will induce localized overheating and thus an increase in the failure rate.

Metalization reconstruction*:* Failure in a wire-bond-free module for the pad connection leads to another type of degradation [27]. Indeed, the Coefficients of Thermal Expansion (CTEs) are mismatched and effects can be observed during the PAC test. During a thermal cycle, the metalization layer undergoes compressive stresses between several relaxation phases that induce plastic deformation at the grain boundaries. The consequence is the creation of cracks between the semiconductor part and the metalization what corresponds to a reconstruction of the metallization. Also, the resistivity increases locally, leading undoubtedly to a localized increase in temperature and thus the appearance of a failure mode.

Cracks in die attach: Beyond its mechanical function to insure an electrical con- tact between connectors and the chip, the die attach is also the path to evacuate heat to the base-plate. This layer, very close to the chip, undergoes considerable thermo-mechanical constraints and it is, according to [28], the main failure mode in IGBT [3] power modules. A lifetime estimation in [29], has focused on solder failure modes. It is concluded that the major fault is a formation of cracks in the solder layer between the chip and the DBC[4]. Indeed, this failure mechanism lays on progressive and successive degradation which leads to a general crack and an increase in resistivity and overheating as previously stated.

[26] studied solder technologies with respect to reliability. With silicon car- bide, lead solutions are not competitive any more. Silicon carbide dices will present reduced contact surface and higher operating temperature. Thus, some other technical solutions must been studied. Four solutions are described below:

- A solution with a lead, silver and tin alloy does not present any deterioration after 1000 cycles;
- A solution with silver nanoparticles presents cracks after 100-300 cycles;
- A solution with a silver sintering presents delamination phenomena after 1000 cycles;
- A solution with a gold alloy does not present any deterioration through 1000 cycles.

The first and fourth solutions seem to be equivalent in terms of reliability. For economical reason, the first proposal is considered to improve the die attach reliability in module with SiC chips.

DBC cracking: [26] and [30] present studies on DBC issues. The choice of a substrate is essential because it must satisfy strong constraints. Indeed, it must ensure an efficient heat transfer. The DBC will have to ensure electrical continu- ity knowing that it will be subject to mechanical stresses generated by thermal effects. The CTE of the DBC must be similar to that of the substrate (silicon and silicon carbide). Among the most common flavors are Al_2O_3[5] and AlN[6]. However, preference will be given to AlN because its CTE is close to that of Si as well as SiC. Moreover, it is well suited for high-temperature applications. The weakness is mainly located at the edge of the interface between copper and sub- strate. Indeed, due to the various mechanical constraints, cracks appear at these parts. With the technological developments of components, the power density is constantly increasing (this is the case of SiC) the thermo-mechanical constraints are increasingly important. Moreover, SiC presents another weakness which is located at the gate level. Studies [31] show that under the same level of stress, SiC technologies are more fragile compared to Si. The weakness is due to the use of SiO_2[7]. This study is consistent with the failures observed throughout our experiments.

3 Accelerated ageing process

In the literature, many accelerated life tests have been performed either on single chips, packaged or unpackaged, or on single modules. Few studies deal with a complete system. Few studies are dedicated to the failure mechanisms of SiC MOSFET-based power module as summarized in [32]. As mentioned before, the factors accelerating the degradation of the MOSFET gate are the high temperature, a high drain current (short circuit) or the application of a high voltage on the gate continuously. The DC gate voltage method will be considered to obtain an acceleration factor for the failure mode of the gate and not of the other parts of the chip and module. Concerning the failure modes of the module, the literature shows that thermal cycling seems to accelerate most of the expected failures. To impose thermal cycling, two approaches are possible. The first one is a passive cycling, the second one is an active cycling.

- Passive cycling [33], [34] consists in getting the module in a controlled climatic enclosure with a temperature varying from -55 C to 180 C. This method imposes thermo-mechanical constraints on the components and causes the failure modes expected in a power module;
- Active cycling [10], [35] is more representative of the operating constraints because the temperature distribution in the module is created by the heating of the chip. This study shows that the upper and lower temperature limits as well as the duration of the cycles allow exciting some failure modes more than others.

3.1 Description of the test bench for the ageing process

Reliability testing is performed on a module consisting of a single converter leg with one MOSFET per switch. To stress SiC power MOSFETs, there are two tests which are mainly used in literature: HTGB8 and HTRB9. These tests have been created to stimulate the MOSFET gate oxide degradation. So, to initiate the failure modes specific to the MOSFET gate, the HTGB test was chosen. Two types of HTGB tests will be performed: the first with a positive bus voltage higher than the nominal voltage and the second one with a negative bus voltage lower than the nominal voltage. Each HTGB tests will be carried out on 4 identical modules in order to check the repeatability of the behavior of the indicators. The indicators observed during these tests will be the gate threshold voltage, the drain leakage current, the drain-to-source on-state resistance and the gate leakage current. The HTGB test consists in applying a constant gate bias under a high ambient temperature. During this test, no current flows through the MOSFET. Temperature and electrical stresses have to be chosen according to several parameters: the nominal operating values for the gate bias and the maximum temperature allowed.

3.2.1 Power Active Cycling tests

The Power Active Cycling (PAC) tests using the HTGB test is realized to learn about the SiC MOSFET behavior suffering from a Gate oxide ageing under thermal cycling. So, PAC tests have been designed to stimulate different failure modes and try to de-correlate gate failure modes, metalization failure modes and transfer element failure modes. The first test consists in long thermal cycles created by the self-heating of the MOSFET under a nominal drain current. The aim is to trigger a heat diffusion through all the layers of the module during each cycle. This heat diffusion should trigger the failure modes concerning the metal- ization, solder transfer and the substrate. The second test is composed of short thermal cycles created by self-heating of the MOSFET whose drain current value will be much higher than its nominal value. This test will allow the triggering of charge traps in the gate oxide as well as the metallic reconstruction of the upper metalization. During both types of PAC tests, the gate leakage current, the saturation current, the gate threshold voltage, the on-state resistance, the reverse voltage and the thermal resistance are recorded. The saturation current will be used as a TSEP[10] to estimate the temperature in the conduction channel. A calibration phase has been carried out and already shows that a rigorous protocol is necessary to obtain an accurate correlation between the saturation current and temperature. Indeed, the state of charge of the gate creates a bias in the value of the saturation current, so the calibration comes after an OFF state with a gate voltage of -5 V between each measurement in order to reset the state of charge of the gate. The global consideration of all these indicators in both types of test should make it possible to dissociate the different failure modes. For the sake of repeatability, the PAC tests will also be carried out on 10 sample modules. Only the lower-side MOSFET in the converter is tested and

monitored. A last test will be performed in a specific test protocol monitoring the junction temperature, the drain leakage current and the reverse voltage to track the internal diode reliability.

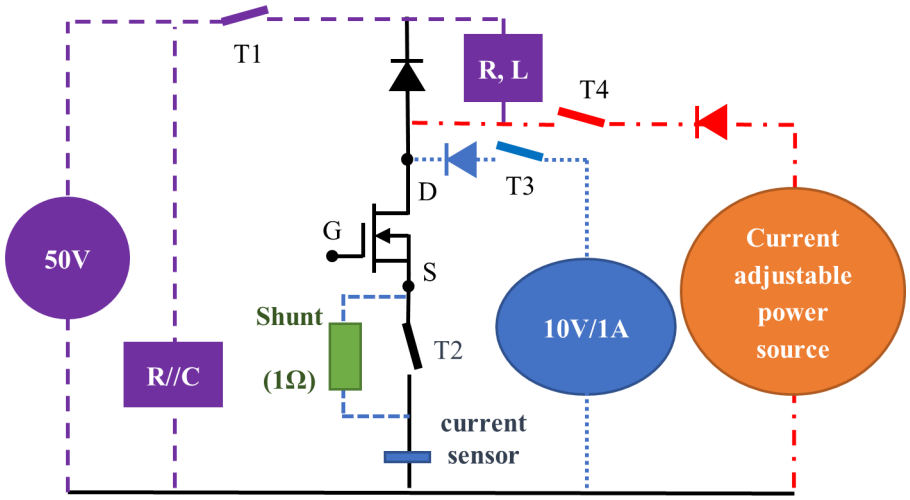

Fig. 2. Synoptic of the Power Active Cycling test bench

As shown in Fig. 2 the PAC test bench is composed of a power circuit to trigger the self-heating of the MOSFET under study. Another circuit allows to measure the value of the saturation current. A last circuit allows to realize a double-pulse. This step will be used to obtain an evaluation of the threshold voltage via the Miller plateau and to measure the on-state resistance. Figure 3 shows the logical sequences of driver signals. The self-heating pulses take some seconds and the double-pulse needs few microseconds. During the test duration, the power module undergoes a long heating phase (+1000s) followed by a short cooling phase (4s). The die self-heating during DC current conduction produces the heating phase. The die turn-off and a cooling system ensure the cooling phase. The temperature swing is imposed between 40 C and a maximum limit which is between 110 C to 150 C. This is an ageing accelerated test thanks to an electrical stress what creates successively self-heating and cooling phase in the SiC MOSFET. The temperature and the electrical parameters are evaluated during this cooling phase. Many dynamic parameters (Rise time of Gate voltage, Gate current peak . . .) but also static parameters (On-state voltage, On-state resistance . . .) are recorded during the double-pulse phase. A total of 50 potential ageing-related parameters are collected over the lifespan of the module (see Table 3 in Annex).

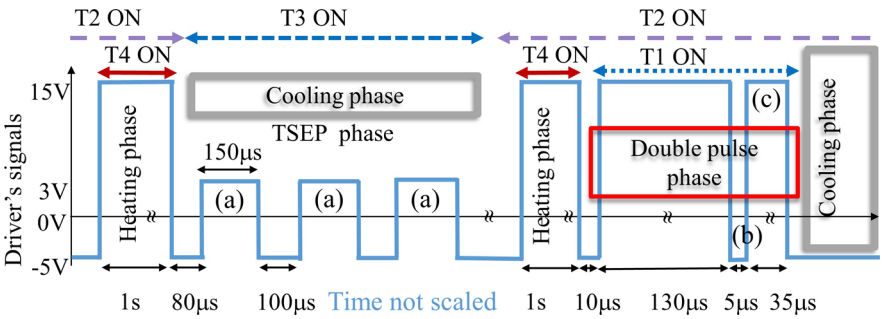

Fig. 3. Typical waveforms during the TSEP phase and the double-pulse measurement: (a) Measurement of *IDS* and *VGS* to obtain a temperature evaluation, (b) Measurement of *IDS* and *VDS* to extract a on-state resistance *RDS ON* evaluation, (c) Measurement of the Miller effect to extract the threshold voltage *VTH* .

The following figures show the configurations when the transistors are ON:

- Fig. 4: typical circuit when T2 is ON;
- Fig. 5: typical circuit when T4 and T2 are ON, the SiC MOSFET is OFF;
- Fig. 6: typical circuit when T3 is ON;
- Fig. 7: typical circuit when T1 and T2 are ON.

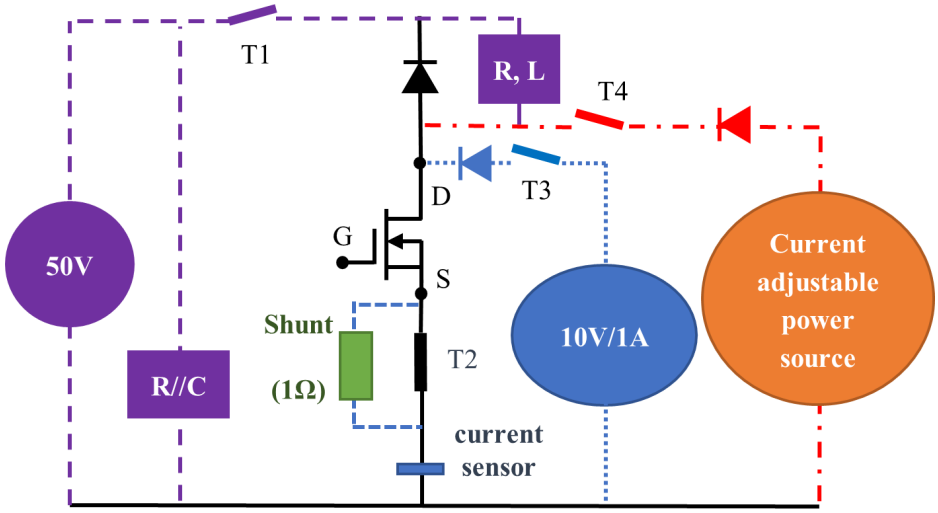

Fig. 4. Typical circuit when T2 is ON

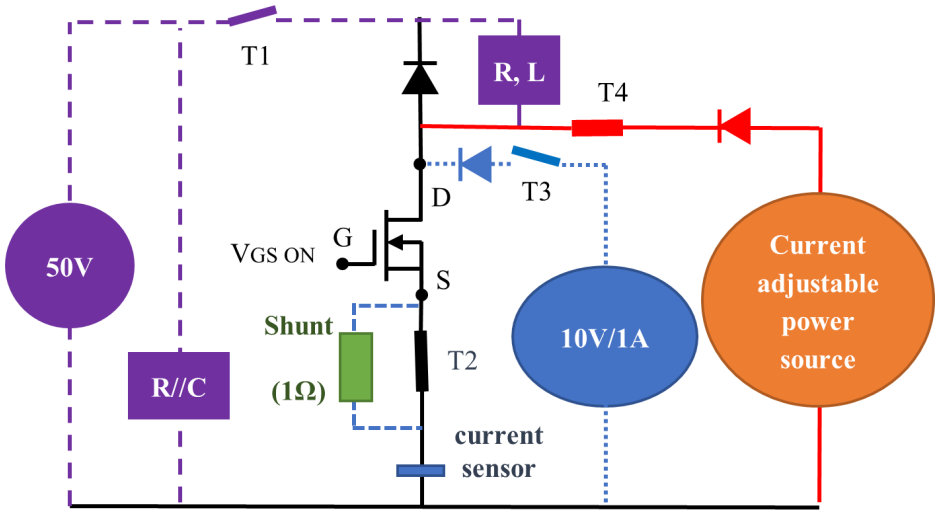

Fig. 5. Typical circuit when T4 and T2 are ON

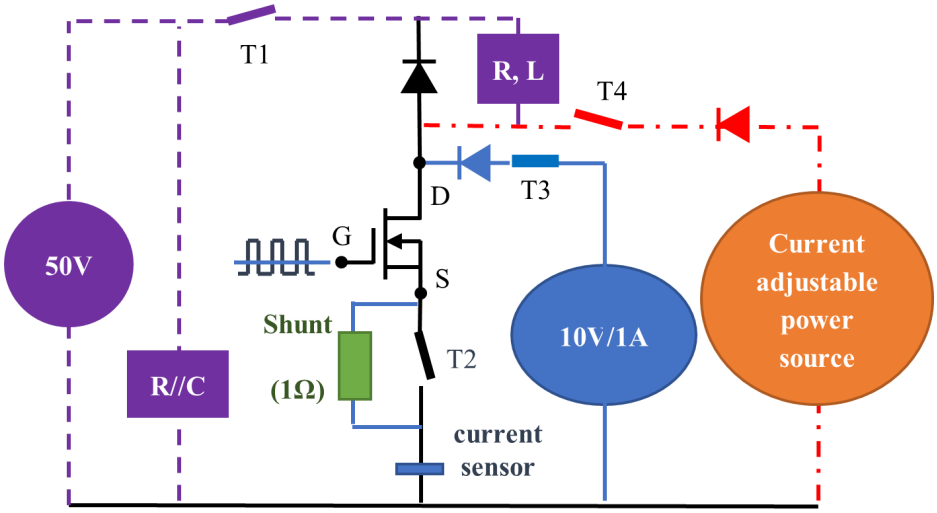

Fig. 6. Typical circuit when T3 is ON

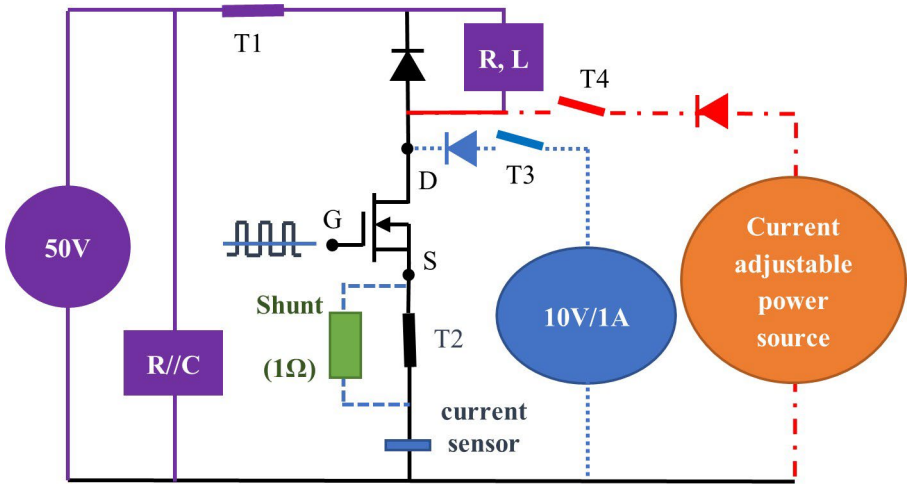

Fig. 7. Typical circuit when T1 and T2 are ON

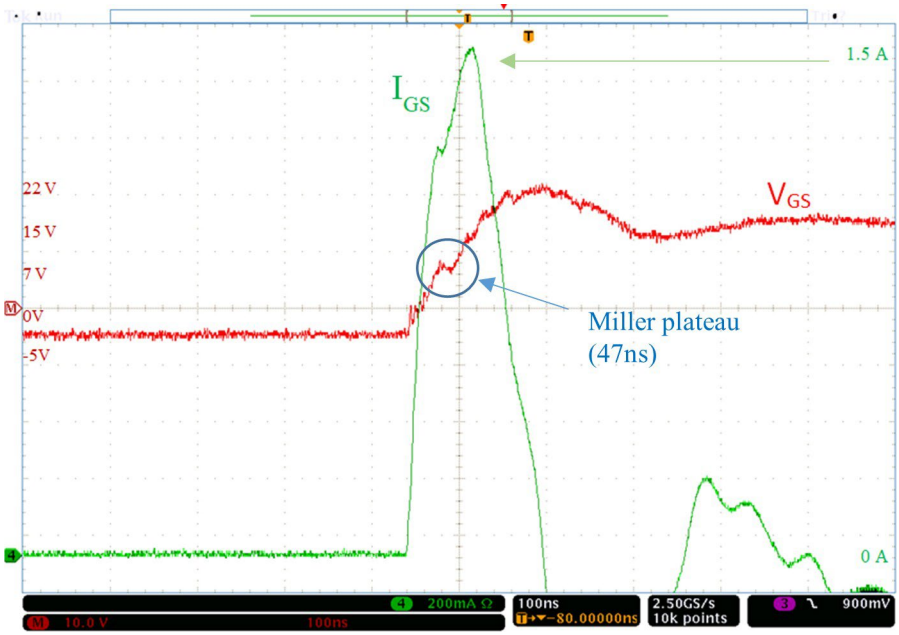

Fig. 8. Typical electrical signals during a SiC power MOSFET turn-On

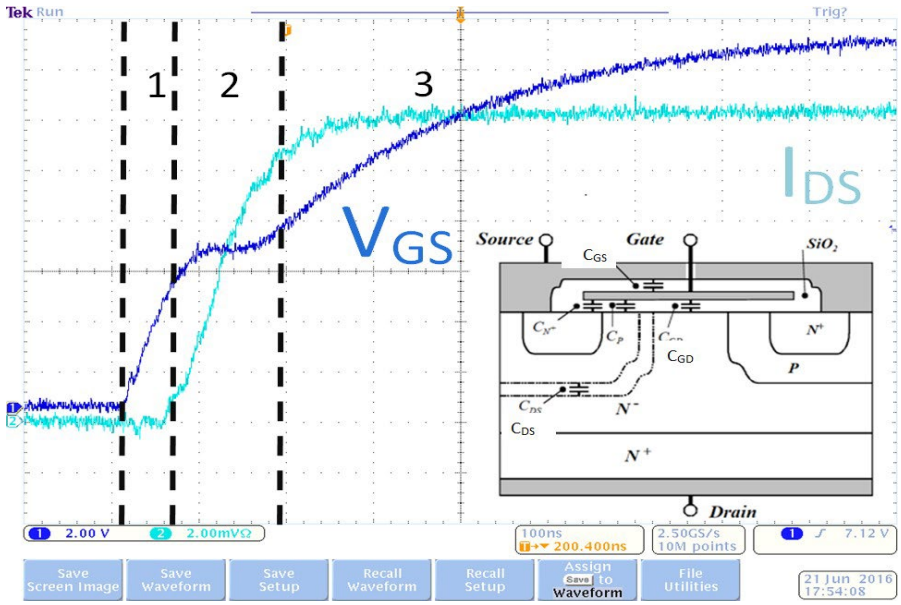

Fig. 9. Typical electrical signals during a SiC power MOSFET turn-on: stage 1 to 3.

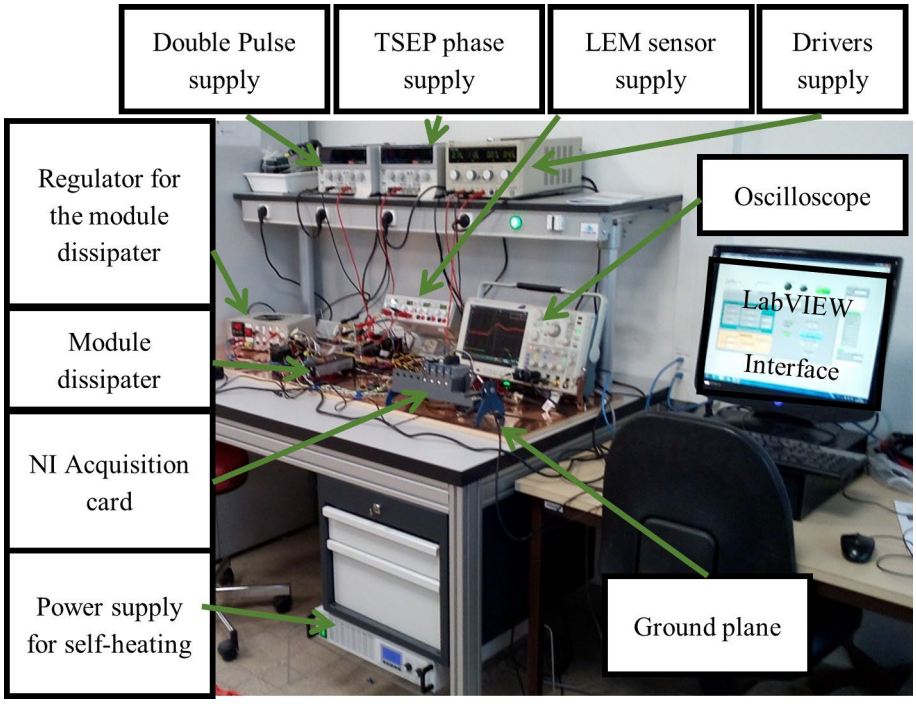

Fig. 10. Test bench: global view

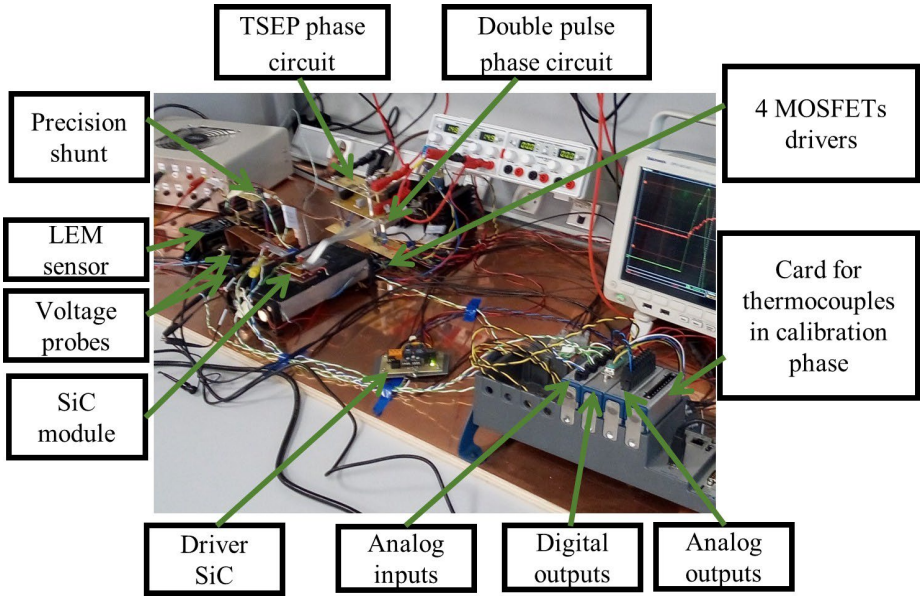

Fig. 11. Test bench: close-up view

During a switching transient, the following process is observed. Signals V_{GS} and I_{GS} are shown in Fig. 8 and signals V_{GS} and I_{DS} are shown in Fig. 9. The waveform in Fig. 8 is particularly interesting because of the pseudo Miller effect which is linked to the threshold voltage. This one is a good indicator of gate state-of-health.

One can decompose the transient response during a commutation from off- to on-state as shown in Fig. 9.

- During stage 1, V_{GS} increases and I_{GS} decreases regularly: it is the Gate- to-Source capacitance charging. The MOSFET is off and the drain current is nearly zero. The drain voltage remains mostly constant.
- During stage 2, a drain current appears and the drain voltage decreases, because of the drain-to-gate capacitance end of charge. The drain-to-gate capacitance is charged with the current flowing in the gate-to-source capacitance. This negative feedback creates a pseudo-plateau which occurs during 47*ns*. Features of this pseudo-plateau will constitute a reference in this study because they are linked to the health of the gate oxide.
- During stage 3, the gate-to-source voltage increases until the driver operating point. The drain current reaches its nominal value and the drain-to-source voltage reaches its lowest value.

Figures 10 and 11 show the test bench. It allows accelerating the ageing process of SiC MOSFETs [36].

The feature selection is based on the following steps:

1. Collect parameters issued from 10 cycling tests,
2. Feature selection based on monotonous behavior of the parameters with ageing and sufficient information level,
3. Selection of 10 best significant parameters for classification purpose,
4. Signature extraction at determined percentage of lifespan,
5. Classification into 4 classes thanks to a supervised signature approach,
6. Monitoring and percentage of life elapsed estimation.

Test campaigns have produced a database constituted of 50 parameters recorded every 3 minutes during the lifespan of 10 modules knowing that each modules present a lifespan between 20,000 and 176,000 cycles of stress (see Table 3 in Annex). All these parameters have shown a monotonous evolution according to ageing over the lifespan. Parameter values have been normalized in time and in amplitude. As the on-state resistance had drifted over 10% for the MOSFET of the modules during lifespan, it has been decided that the degradation was sufficient to select ageing parameters, i.e. to reduce this set neglecting the parameters of least pertinence [37].

4 Failure mode signature

The conduction path degradation and a partial perforation of the gate oxide lead to the drift of several parameters. In each test, the duration of ageing has been different and the definitive failure mode has been either a deterioration of the gate or a deterioration of the drain-to-source path. According to this variability, the chosen parameters must be sensitive to the related failure modes. To judge the sensitivity of parameters, two mathematical tools are used:

- Spearman correlation coefficient calculation in order to check the monotonous behavior of the signal with aging [38];
- Shannon entropy calculation in order to check the sensitivity [39].

Once the monotonous parameters are isolated, their sensitivities are com- pared. As the ageing has led to different failure modes with different lifespans, the Shannon entropy coefficient varies for each tested device. The aim is to gather a batch of parameters sufficiently sensitive to both possible failure modes.

The selection of parameters is based on two steps. The first step consists in evaluating the Spearman correlation which allows detecting parameters linked to ageing [40]. The Spearman approach lays on a research of a monotonous behavior at each rank iteration. The calculation of the coefficient is given by:

Eq.(1)

where $rg(X_i)$ $rg(y_i)$ is the difference between the two ranks (two recordings) of each point and n is the number of points. As a consequence, the Spearman approach helps reducing the number of candidates from 50 down to 20.

The second step is based on a Shannon entropy calculation which highlights the most informative parameters [41]. It constitutes a good tool to find out the best information carried out by the correlated failure precursors. The Shannon entropy, H, evaluates the level of information contained in a signal as [41]:

Eq. (2)

where X is the studied signal and P_i is the probability to meet the i^{th} class of the signal. In our application, the Shannon entropy calculated for 20 pre-selected parameters gives:

- the maximum entropy value is 3.2 (100%)
- the minimum entropy value is 0.5 (0%).

Table 1 shows the entropy coefficient of the 10 selected parameters. We are not able to classify them by order of importance, that is why we keep all these 10-parameter batch and then proceed to a PCA [11] to reduce the problem order of the neuronal network used afterwards.

Table 1. Entropy calculation for correlated parameters of each tested module

Parameters	Modules									
	TM1	TM2	TM3	TM4	TM5	TM6	TM7	TM8	TM9	TM10
Temperature	2.5	2.8	2.3	3.2	3.1	2.6	2.6	2.2	2.4	3.1
IdVg	2	X	2.25	3	2.9	2.6	X	2.3	2.8	2.9
IdP	2	X	2.25	3	2.95	2.5	X	2.3	2.8	2.6
RiseTime	1.1	2	X	2.7	X	2.3	X	X	X	3.2
Tmeanplateau	0.5	1.6	X	2.3	X	2.	X	X	X	3
RDSON	X	3	2.5	2.8	3	2.5	2.9	2.5	2.6	3
VDSON	X	3	2.4	2.9	3	2.5	2.5	2.3	2.5	3.1
PMiller	X	2.7	2.3	2.5	3	2.3	2.5	2.3	2.3	3
Meanplateau	X	2.7	X	2.9	X	X	X	X	X	X
Coeflinear	X	3	X	2.7	X	X	X	X	X	X

The 10 parameters are selected thanks to a satisfying correlation level (65%) with ageing and cover more than one failure mode: T_J , $I_{DS} * V_{GS}$, I_{DS} , $V_{DS\ ON}$, *PMiller* , *TMean Plateau*, *VGS Slope*, *Rise Time*, *Pinst* and *RDS ON* (see Table 2). Consequently, a 10-dimension signature is composed of parameters whose drift is linked to the gate oxide failure mechanisms and some other parameters whose drift is linked to interconnection issues.

Table 2. Ten parameter candidates composing the failure signatures

Abreviation	Description
TJ	Estimated temperature at the third pulse
*IDS * VGS*	instantaneous power during the second pulse
IDS	Current during the second pulse
VDS ON	Voltage during the second pulse
P_{Miller}	Mean voltage of Miller plateau
$T_{Mean\ P\ lateau}$	Mean time of Miller plateau
$V_{GS\ Slope}$	Slope of the Miller plateau
Rise T ime	Gate voltage rise-time
Pinst	Instantaneous power
RDS ON	On-state resistance

4.1 Failure Signature classification

Once the signature is constituted, a classification helps matching the power module ageing and the signature value. Six modules have been chosen to constitute a learning database [37]. For each module, we have extracted the value of the signature from different lifespan of the power module (0%, 30%, 60% and 100%), as pictured in Fig. 12. The modules have shown various failures under different stress levels so they constitute a base to construct a model of classification.

- Class 1: 5 signature values are extracted from healthy samples;
- Class 2: 5 signature values are extracted around 30% of the lifespan;
- Class 3: 5 signature values are extracted around 60% of the lifespan;
- Class 4: 5 signature values are extracted before the end of the lifespan.

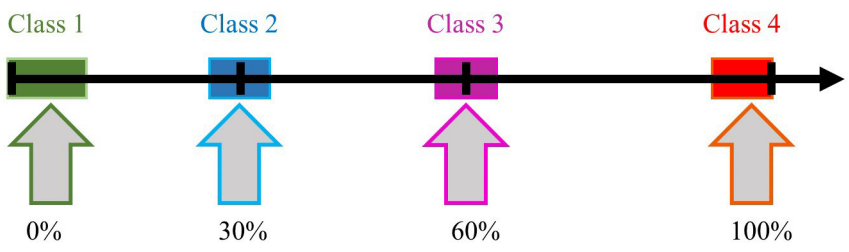

Fig. 12. Signature Classes' construction

Four learning classes have been constructed upon the values of the signatures for various module lifespans. For each module a range of 5% of the lifespan has

been defined around the reference values by extracting 5 values of the signature for each class. The learning phase is realized with 5 points extracted for 4 classes during the lifespan of 6 modules to constitute the learning database. A total of 120 signatures are available in the database. The learning phase has been realized with 84 signatures among the 120 constituting the learning data. The validation test has been realized with 18 signatures and finally an attribution test has been made with 18 signatures. The results are presented in Fig. 14.

4.2 Neural Network

Many schemes or types of Neural Networks exist [42], [43], [44], [45], [46]. The simplest one is a neural network based on three layers. This one is widely used and covers a large number of applications. Each layer is composed of neurons which are connected to the previous layer via weights. The first layer is connected to the input variables. The output layer is composed of one neuron per output. In our application, we have 10 input variables and 4 output variables as shown in Fig. 13. A bias is connected to all layers via weights. The relationship between inputs and outputs in a multilayer NN[12] is generally based on nonlinear functions. The activation function used in the hidden layer is a *sigmoid* Symmetric Transfer Function described as follows:

Eq. (3)

Eq. (4)

with x_i the input, $w_{i,j}$ is the weight between the input x_i and the neural j, b_i is the weight between the bias and the neural j and n the number of inputs. This type of function is interesting for the training process because its derivative is a continuous function ($f'(x) = 1 \quad f(x)^2$). For the output layer, the choice is a *softmax* function. So, we introduce an intermediary variable based on this equation:

Eq. (5)

Finally, the output layer is described as follows:

Eq. (6)

The learning algorithm is based on scaled conjugate gradient back propagation knowing that our NN design is composed of one input layer with 10 nodes, one hidden layer with 10 nodes and one output layer with 4 nodes. The goal of the training process is to define all weights of the NN. The learning phase was tested on 70% of the database, i.e. using 84 signatures among the total of 120 signatures. 15% of signatures are dedicated to the validation phase and 15% for the test. The results are shown in Fig. 14.

The detection of the condition monitoring system is effective. The detailed rates of classification are also presented: healthy state (1), 30% of the lifespan (2), 60% of the lifespan (3), and close to the end of the lifespan (4). In conclusion, results show an efficiency of 100% in class attribution.

In order to validate this classification using a NN, a test on a separate sample module has been performed. The result is promising as 96% of good attribution to classes are observed. Classes 1, 3 and 4 are well discriminated with this model. Only Class 2 is not determined for the last signature. One can suppose that this class is certainly not discriminating enough for the module under test (i.e. the lab-scale technology selected to provide ageing data). In conclusion, the neural network shows promising results. Signatures are well discriminated. The proposed approach to estimate the remaining useful lifetime is a rough draft and can constitute a great track to explore. The results obtained with few samples are promising. The next step would be to consider a realistic mission profile to estimate the remaining lifetime in a given environment and not only the estimated percentage of elapsed lifespan. Rainflow-type approaches could be used in this perspective.

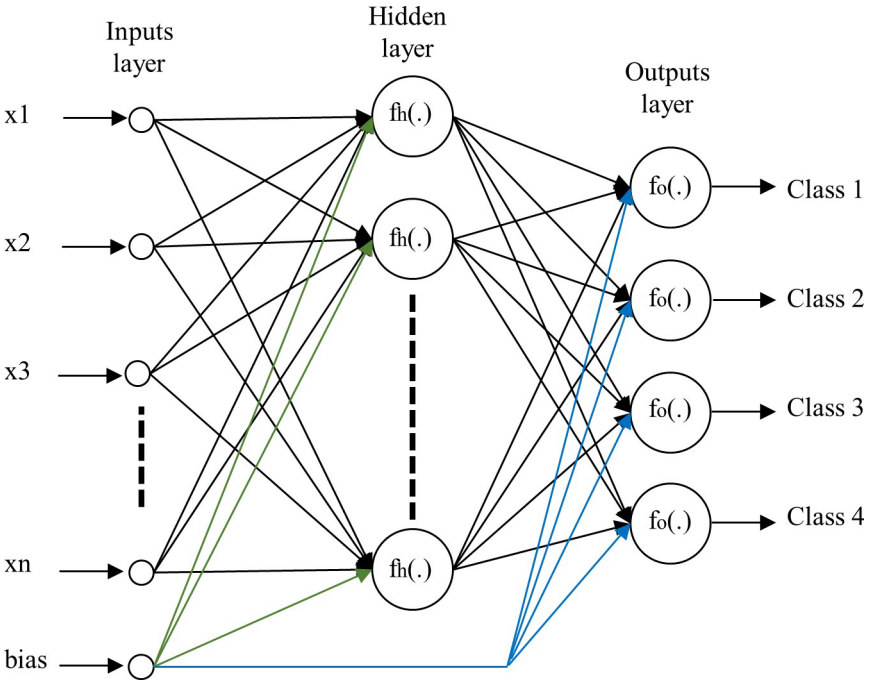

Fig. 13. Structure of a neural network

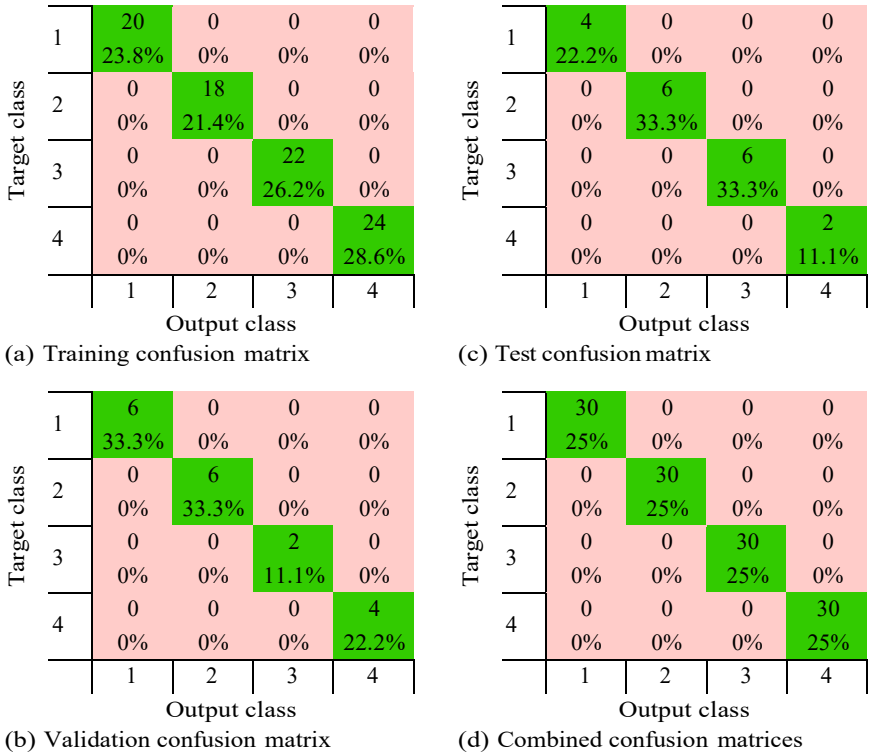

Fig. 14. Neural Network confusion matrices issued from the learning phase (84 signatures), from the validation phase (18 signatures) and from the test phase (18 signatures) gathered in the combined confusion matrix view.

5 Conclusion

This chapter wishes to offer a synopsis of a larger work on the estimation of the percentage of life consumed in the operation of a power module with SiC power MOSFETs. Results are based on a lab-scale power planar module of non-mature technology. One interest was to give rise to failure modes of a large variety. It is then a complete example of the necessary steps involved in selecting a monitoring strategy. Failure modes have to be identified as well as the parameters to sense them. The most informative precursors are selected among a large number of recorded ones during the test, thanks to the Spearman correlation and the

Shannon entropy calculation. These mathematical tools have allowed to systematically extract the precursors that have a monotonous evolution against ageing. Then, the reduction in the number of contenders was made based on the 10 best candidates which better represent variations according to ageing whatever the failure mechanism in progress. According to this signature evolution, 4 classes have been created thanks to a learning process based on 6 modules. The first class represents a healthy signature, the second one a signature around 30% of the lifespan, the third one a signature around 60% of the lifespan and finally a fourth class which represents a signature at the end of the lifespan. One efficient model to discriminate these classes is a neural network. The model was tested on a separate module and has attributed the signature in the true class with a probability of 96%. Finally, an estimation method has been proposed for the percentage of consumed life. The method has been implemented. The important conclusion is the applicability of the strategy detailed in the chapter: it is repeatable with quite any technology of planar module based on SiC MOSFETs.

Acknowledgment Authors acknowledge the financial support of EU H2020 project *I²MPECT* , grant n 636170.

Annex

Table 3. 50 ageing parameters extracted or calculated from the online measurement files

Parameters	Description	Number of parameters obtained
TP(i)	Estimated temperature at pulse 1, 2 and 3	3
IdVg(i)	*IDS.VGS* at pulse 1, 2 and 3	3
IdP(i)	*IDS* at pulse 1, 2 and 3	3
MId	*IDS* at pulse 1, 2 and 3	1
RDSON	On state resistance	1
PMiller	Current power during the second pulse	1
VDSON	Voltage during the second pulse	1
IDSON	Current during the second pulse	1
EON	Injected energy in the gate	1
EONN	Injected energy in the gate normed by *ID*	1
EONN 2	Injected energy in the gate normed by *ID* 2	1
IGmax	maximum gate current	1
VGmax	maximum gate voltage	1
AreaIG	Area under *IG* during turn ON	1
FIG	Pseudo-frequency of *IG* during turn ON	1
RiseTimei	Rise time to reach i V with *i* from 1 to 15	15
AreaVGS	Area under *VGS* during turn ON	1
Areaplateau	Area under *VGS* plateau during turn ON	1
Maxplateau	Maximum point of *VGS* plateau	1
Minplateau	Minimum point of *VGS* plateau	1

Meanplateau	Mean level of *VGS* plateau	1
Lengthplateau	Length of *VGS* plateau	1
Tmeanplateau	Mean time of *VGS* plateau	1
SlopeVGS	Slope of *VGS* curve to reach the plateau	1
SDplateau	Standard deviation of *VGS* plateau points	1
Coeflinear	linear function fitting on *VGS* plateau	1
$Coef_{poly}$	3th order function fitting on *VGS* plateau	4

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