

High voltage GaN-on-silicon with low-trapping up to 1200 V

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Carbon doped buffer within GaN heterostructures is widely used to increase the buffer resistivity and improve the electron confinement. However, it has been shown that carbon doping can also induce electron trapping under high electric field. This paper presents an assessment of a GaN-on-silicon buffer structure from the epi-wafer provider ALLOS Semiconductors GmbH targeting 1200 V power applications. This structure do not include intentional carbon doping showing a residual carbon below $5 \times 10^{16} \text{ cm}^{-3}$ as measured by SIMS. The AlGaIn/GaN heterostructure has been grown on 150 mm silicon (111) substrates by MOCVD. The total buffer thickness is as high as 7.1 μm with several interlayers for strain management. High crystal quality of GaN is observed, with XRD FWHM of (002) and (102) being 395 and 423 arcsec, respectively. The thickness uniformity is below 2% and the bow is less than 25 μm over the 6-inch wafer.

DC characteristics carried out on 2 μm gate length transistors (using a 30 nm thick LPCVD SiN as gate dielectric) indicate low leakage and excellent pinch-off. These data confirm the absence of punch-through effects despite the fact that a carbon-free buffer has been used. Because of the thick and excellent crystal quality of the GaN buffer, low leakage current and state-of-the-art vertical breakdown voltage above 1400 V were achieved at room temperature. The vertical breakdown is above most of the commercially available GaN-based epi-structures (using typical thickness between 5 and 6 μm) while delivering comparable floating lateral breakdown around 2 kV.

The effects of buffer traps have been studied by means of substrate bias ramp measurements. This approach is surface insensitive and applies a 1-D vertical field. Various sweep rates have been used because with slower sweep rates, the thermal generation rate of traps is expected to be enhanced. This is generally observed on 650V-rated commercial devices with trapping activation occurring below 1 kV with an enhancement of the charge storage when using slower sweep rates. In the case of the carbon-free thick buffer, low trapping effects are observed for the first time up to 1200 V. It can be pointed out that a low dependence of the substrate bias on the current density is also observed. This demonstrates the potential advantage of using carbon-free buffers, paving the way to GaN-on-silicon for 1200 V applications with a much lower on-resistance as compared to other existing technologies operating above 1 kV.

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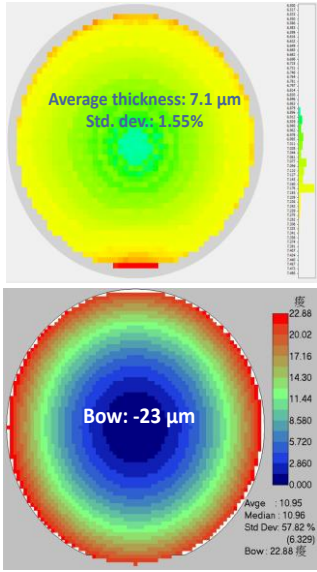


Fig. 1: PL mapping and bow data of ALLOS wafer

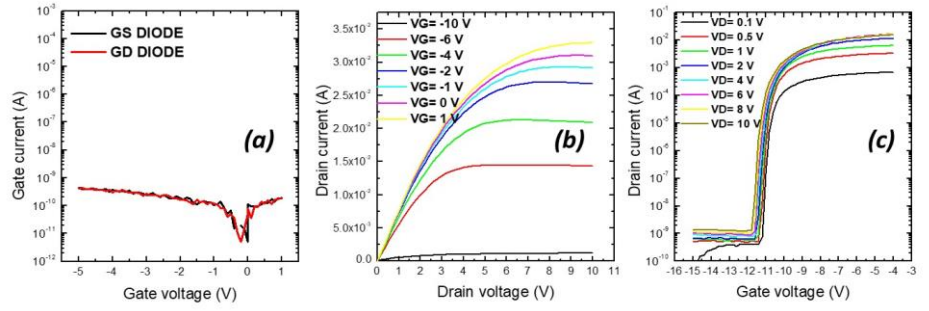


Fig. 2: DC characterizations on devices fabricated on ALLOS structure

(a) diode I_G - V_G (b) I_D - V_D (c) I_D - V_G .

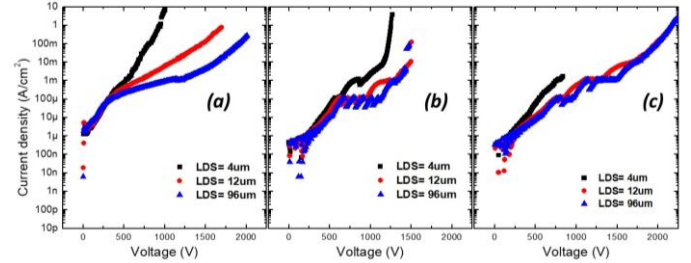
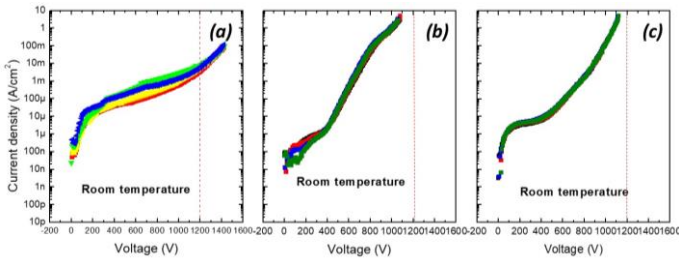


Fig. 3: Vertical (left) and Lateral (right) breakdown voltage of (a) ALLOS structure (b), (c) commercial devices

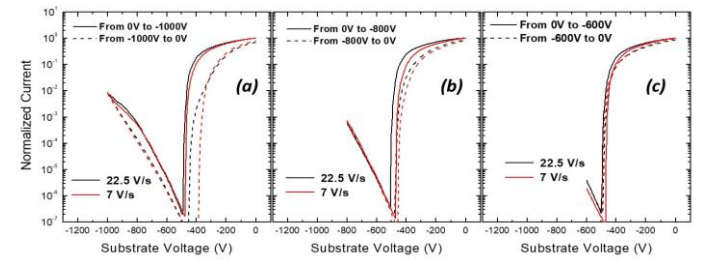
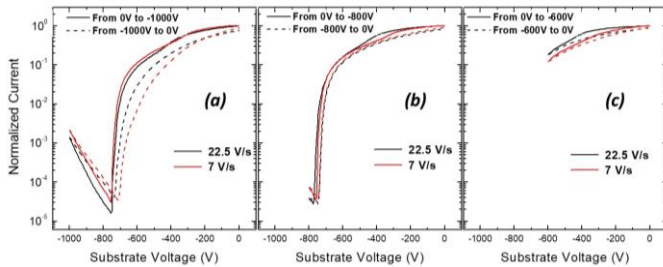


Fig. 4: Substrate ramp down to (a) -1kV (b) -800V (c) -600V on commercial device 1 (left) and commercial device 2 (right)

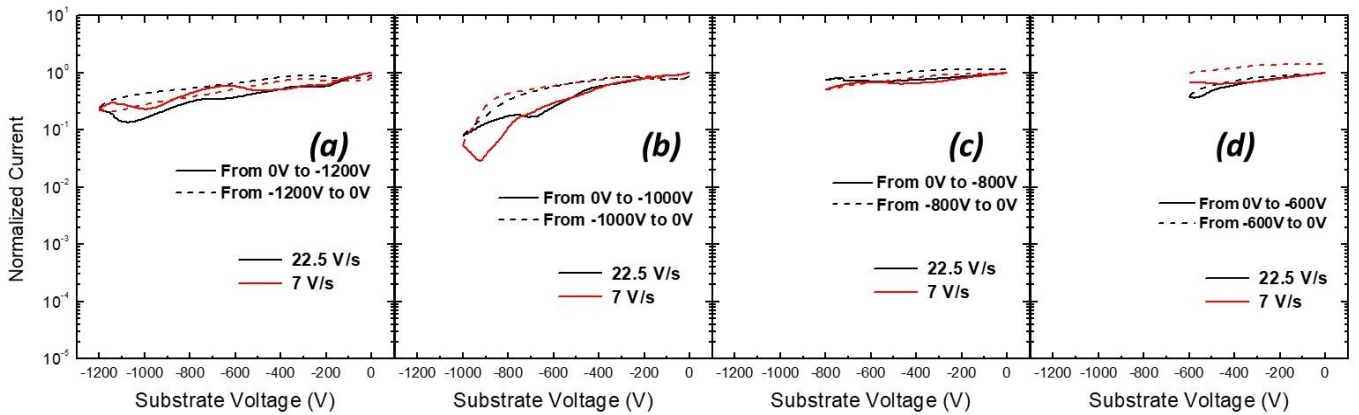


Fig. 5: Substrate ramp at two different rates on the ALLOS structure, down to (a) -1.2kV. (b) -1kV. (c) -800V. (d) -600V.