

GaN HEMTs for millimeter-wave applications: Status and Challenges

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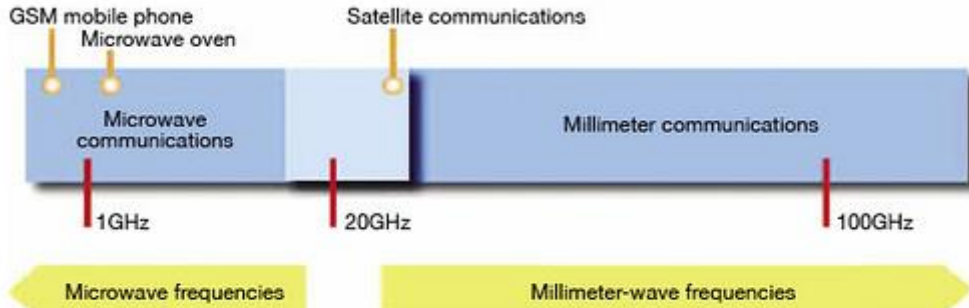
Research and Innovation
InRel-NPower
NMBP-02-2016
EU proposal 720527



OUTLINE

- Introduction
- Challenges and issues for mmW GaN devices
- Development of AlN/GaN heterostructure at IEMN
- Conclusion

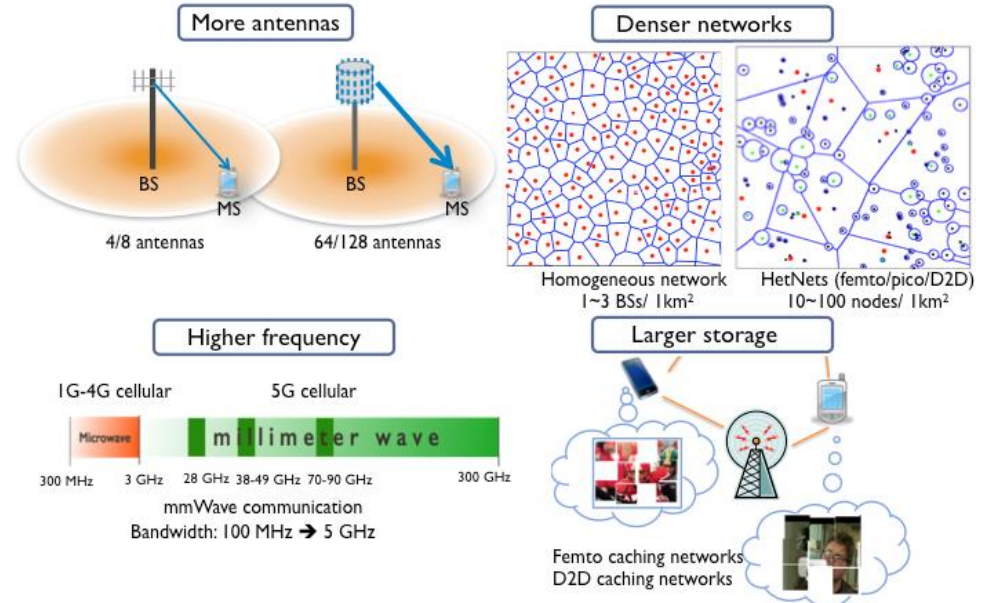
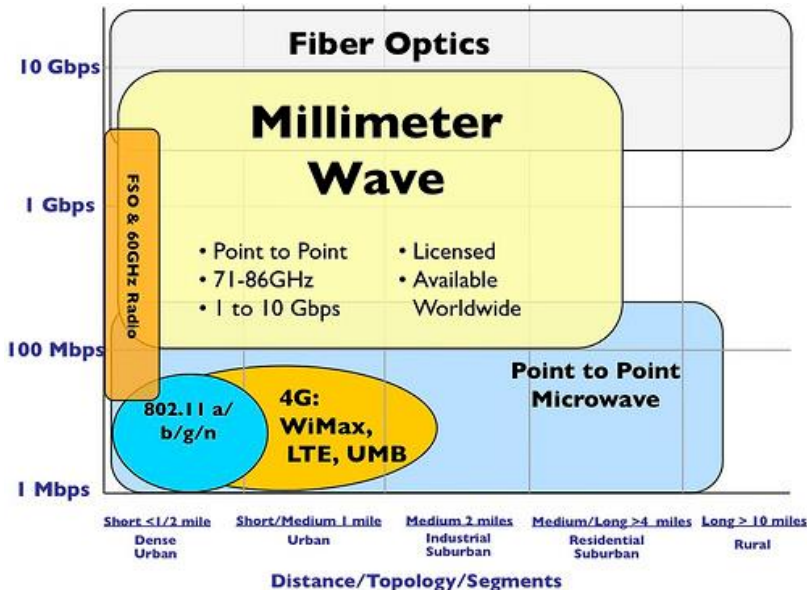
Future communication in mmW frequency range



Communication in Millimeter-Wave Frequencies

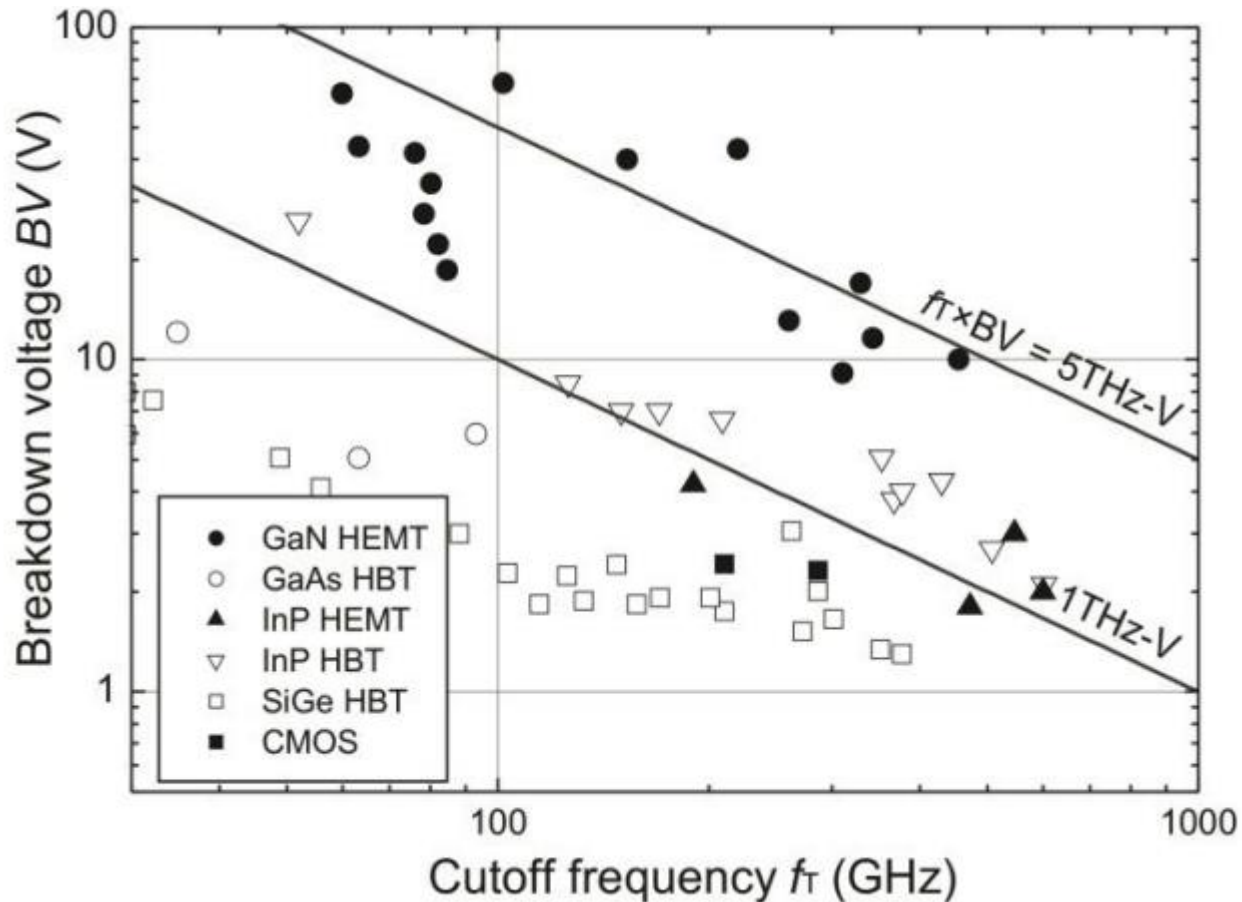
Towards significantly increased bandwidth

Towards 5G Networks



Millimeter Waves Will Expand The Wireless Future with larger bandwidth and smaller device size: more antennas, denser networks, faster communications, larger storage...

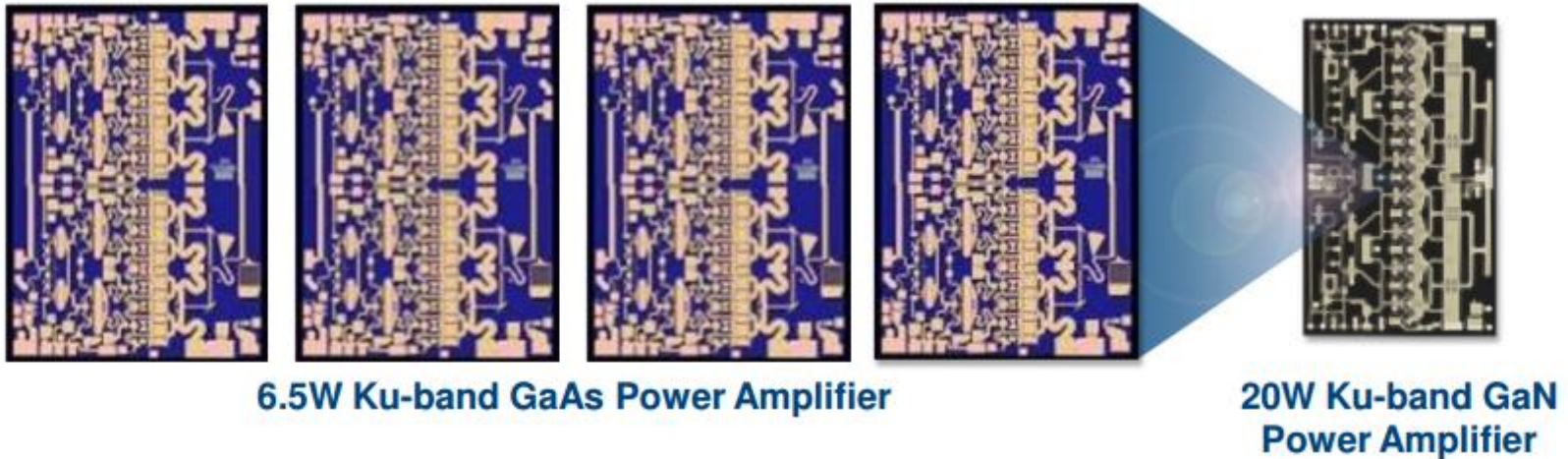
Comparison of Johnson's figure-of-merit (JFoM) among various high-speed device technologies



$f_T \times V_{BK}$ five times better for GaN
(theoretically this is true up to THz range)

GaN devices delivered on their promises

- Significant advantages over GaAs technology or TWT
 - Small size + high robustness ($T^{\circ}C$, damp conditions) make GaN transistors the preferred choice for next generation SSPA

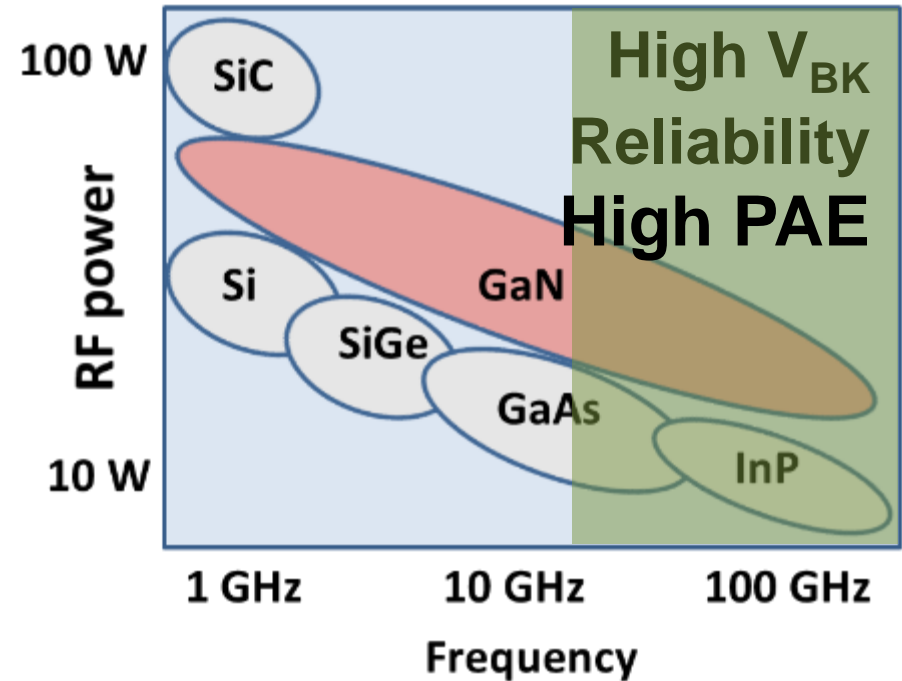
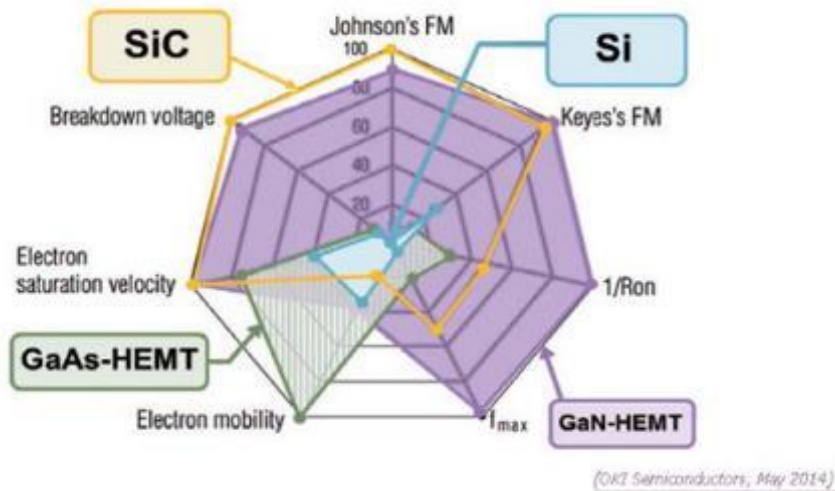


- In order to overcome the TWT, GaN will have to show extremely high power **and efficiency** also at higher frequency.
- **High power density (e.g. high operating voltage) of a single GaN device has to be maintained while increasing frequency of operation.**

GaN will cover the entire frequency range

Even though major challenges are still to be overcome beyond 30 GHz such as high V_{BK} , reliability and especially high PAE

GaN / SiC / Si / GaAs high power RF transistors comparison



Issues and limitations for mmW applications

- Bias operation:
 - ✓ $V_{DS} \leq 15 \text{ V}$ at 40 GHz and above
- Gate and drain leakage currents under high electric field
- Limited efficiency
 - ✓ PAE $\leq 40\%$ at 40 GHz +
- Reliability
 - ✓ Not yet demonstrated on sub-150 nm GaN technology

Limiting factors of GaN device PAE

- High gain at frequency of operation (i.e. high frequency performances)
- Low R_{ON} (minimizing the losses)
- Self-heating (i.e. $T_{channel}$) affecting the effective electron mobility under high bias
- Trapping effects both from surface and buffer to avoid dc to RF dispersion

Device robustness and reliability: crucial for any applications

- GaN RF industrial devices currently qualified up to K band (~30 GHz) using standard AlGaN/GaN structure with gate length down to 0.15 μm

Improved epilayers quality:

bulk traps,
interfaces, point
defects...

Technology:

Ohmic contacts
reproducibly $< 0.4 \Omega\cdot\text{mm}$

Schottky contact:
low gate leakage
current

Passivation: low
surface trapping

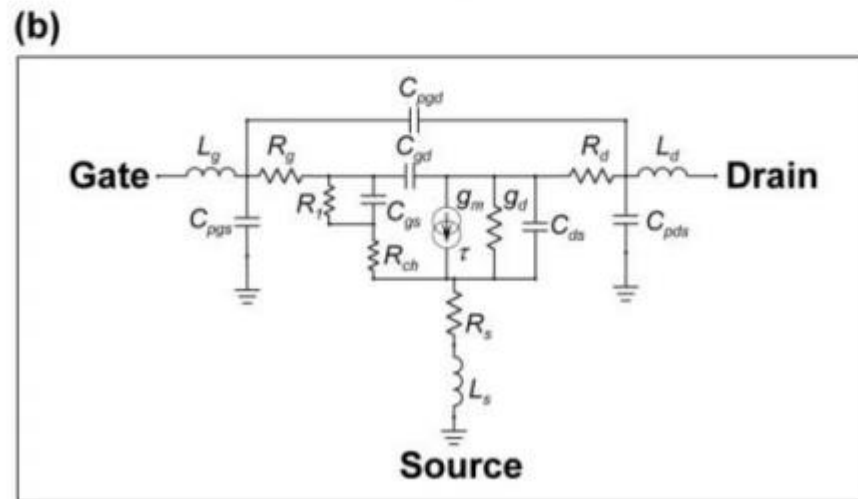
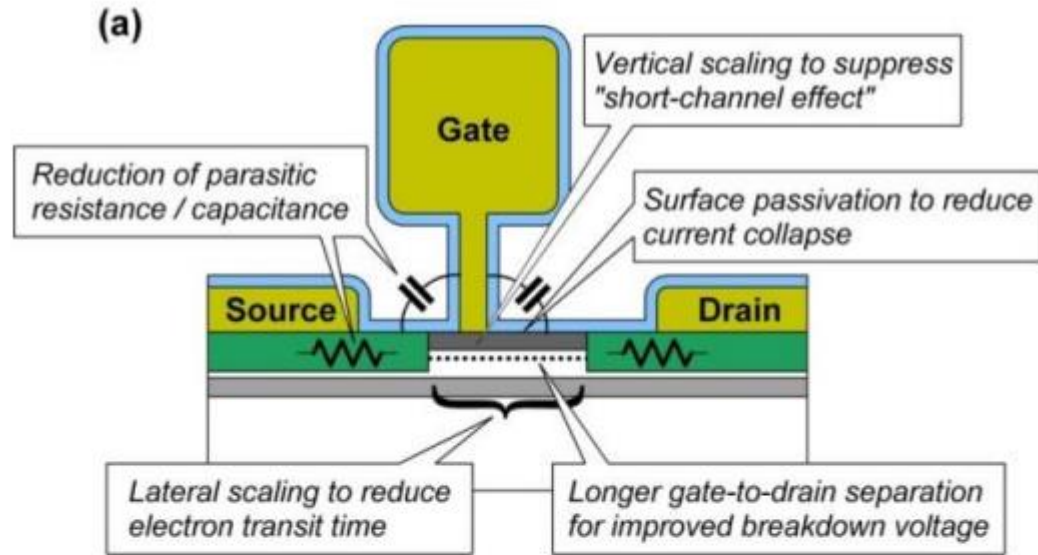
Epi & device design:

%Al into the barrier
layer and use of field
plates to reduce the
electric field peak
around the gate

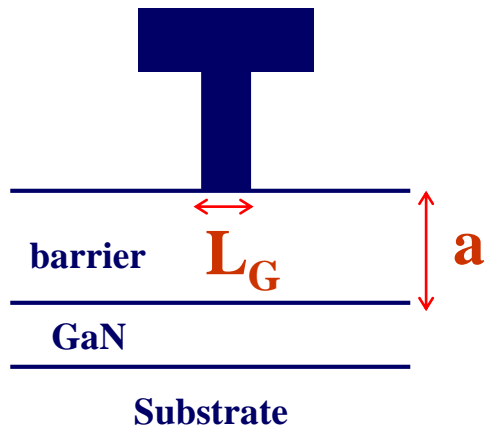
Larger device topology
in order to decrease the
self-heating

Key factors to achieve highly reliable GaN RF devices

Important device scaling features for high frequency operation (a) and an equivalent circuit model (b)



- For Ka band and above (35 GHz +), the power gain becomes an issue with standard AlGaN barrier by using $L_G \leq 0.15 \mu\text{m}$



To avoid short channel effects



$$\frac{L_g}{a} \geq 15$$

G.H. Jessen *et al*, EDL 54 (10), 2007

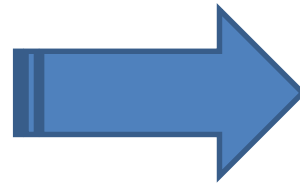
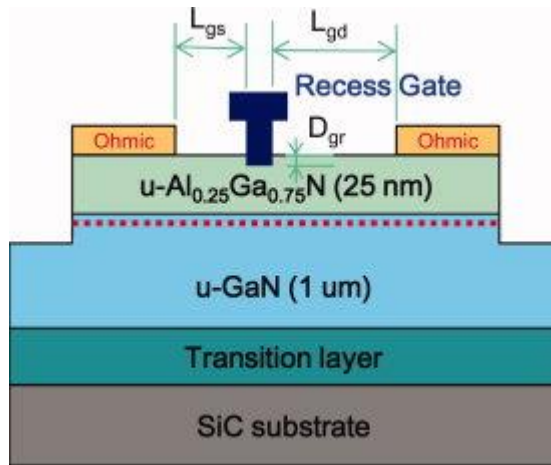


$$L_g = 100 \text{ nm}$$



$$a < 7 \text{ nm}$$

Gate recess for mmW GaN devices: not an option !



under high electric field
(defect induced by plasma
is the killer)

Because of the lack of efficient chemical
(low damage) etching solution for GaN-
based material



A solution is the use of an ultrathin barrier layer with
wider bandgap

To both maintain a high carrier density and achieving
a low gate to channel distance

InAlN

Gate leakage issue
not solved !

InAlGaN

AlN

Device robustness and reliability: crucial for any applications

For mmW apps, reduction of %Al, use of FP or large device design are not possible

Improved epilayers quality:
bulk traps,
interfaces, point
defects...

Technology:
Ohmic contacts
reproducibly $< 0.4 \Omega \cdot \text{mm}$

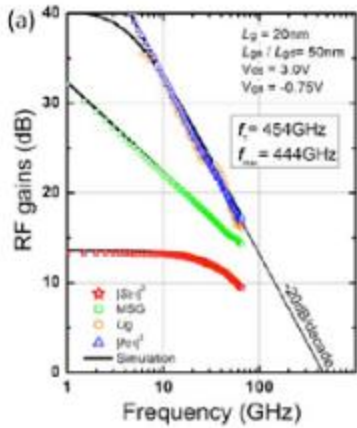
Schottky contact:
low gate leakage
current

Passivation: low
surface trapping

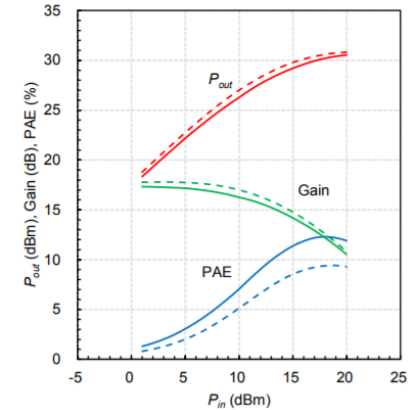
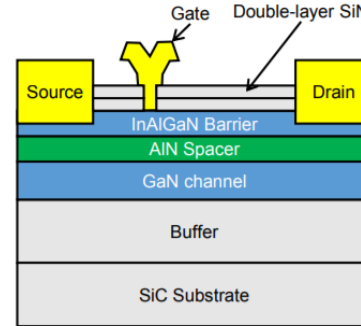
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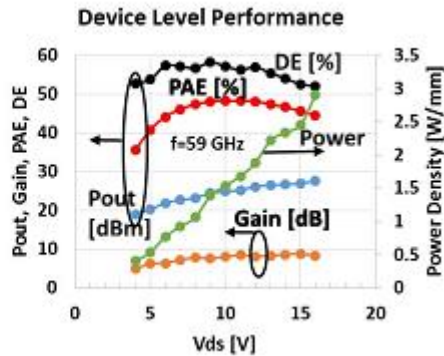
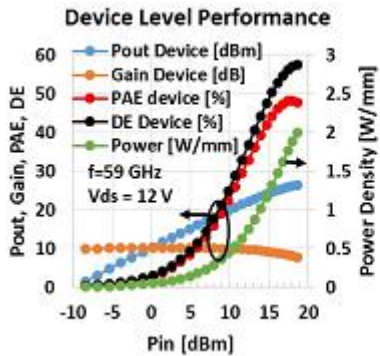
Top RF performances achieved with ultrathin Al-rich HEMTs up to the W-band



AlN/GaN HEMTs with $F_T > 450$ GHz
 Y. Tang *et al*, IEEE EDL, 2015 from HRL



3.6 W/mm High Power Density W-band InAlGaIn/GaN HEMT MMIC PA
 Y. Nida *et al*, IEDM 2016 from Fujitsu



AlN/GaN HEMTs with high PAE at V-band
 M. Micovic *et al*, IEEE EDL, 38 (12) 2017 from HRL

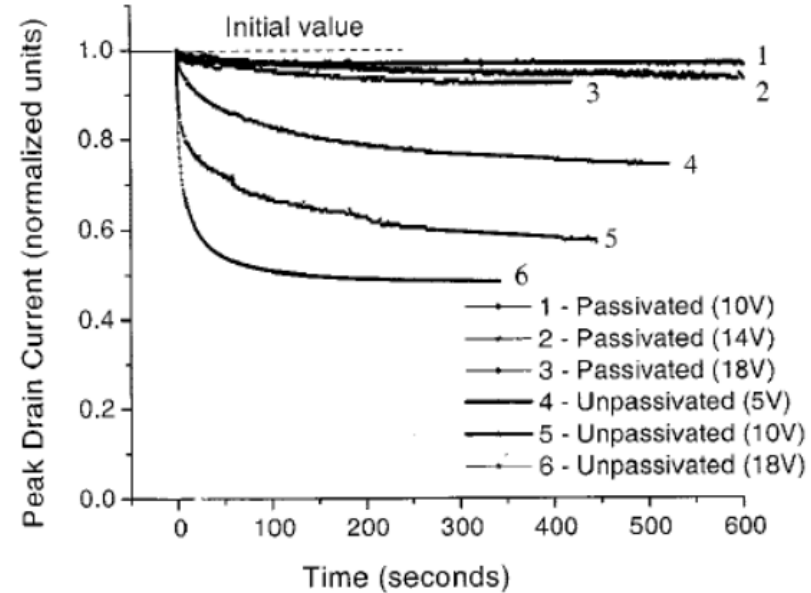
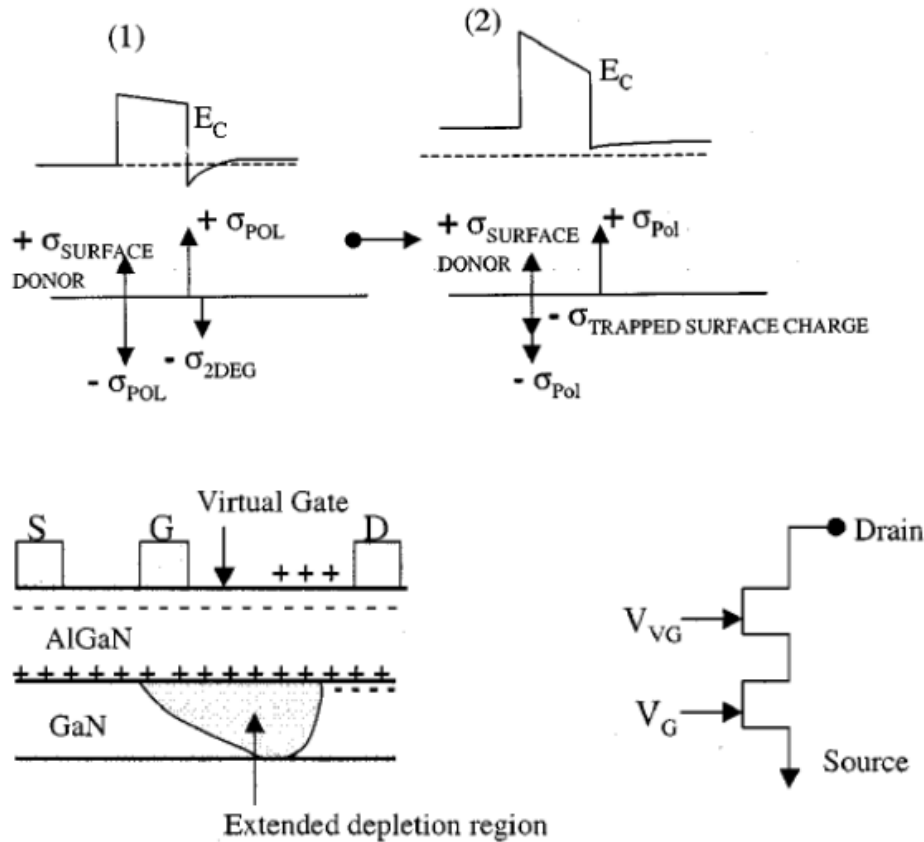
Significant progress in N-polar GaN devices up to W band also recently achieved

However still limited in terms of leakage current , breakdown voltage, and reliability (to be proven)

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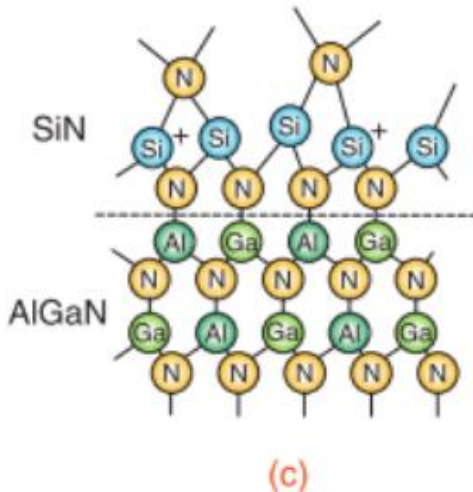
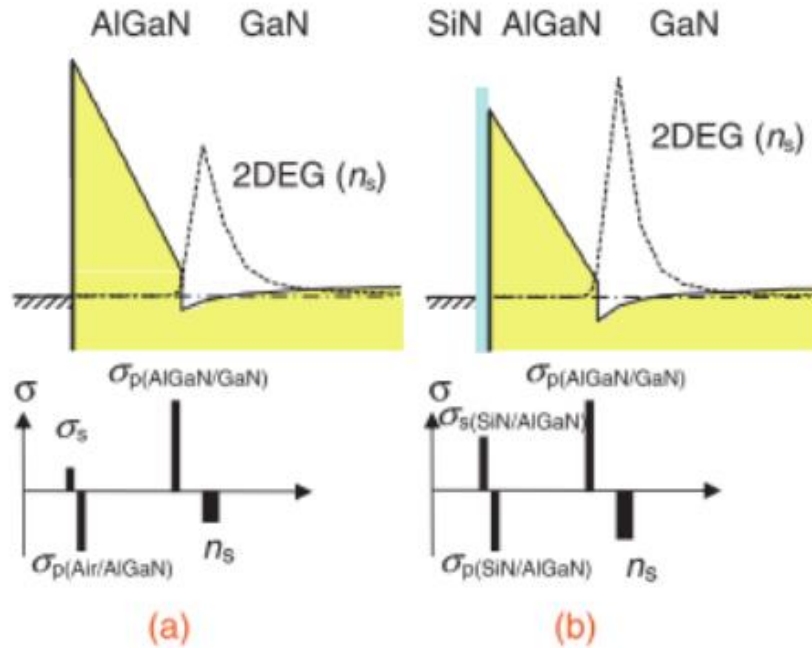
DC-to-RF dispersion



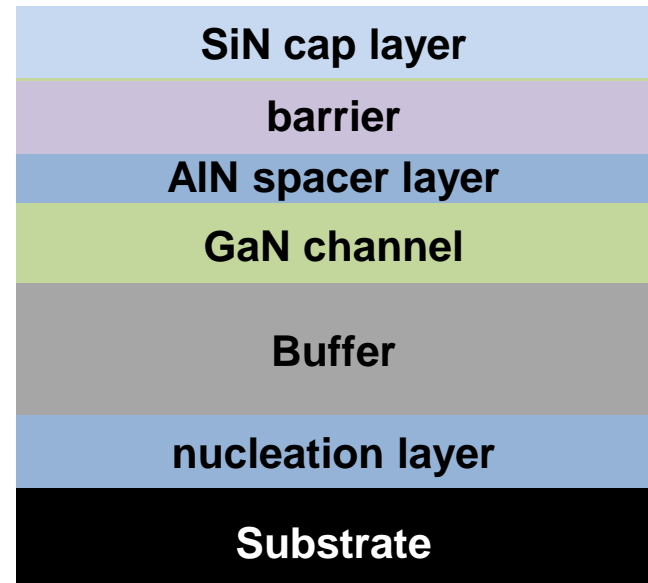
GaN-based heterostructures: inherent surface charges dependent on the electric field, directly interacting with the 2DEG and creating a so-called virtual gate that extends the depletion region, especially when the surface is close to the 2DEG.

Surface charges needs to be properly passivated, otherwise the maximum current available during a microwave power measurement will be limited.

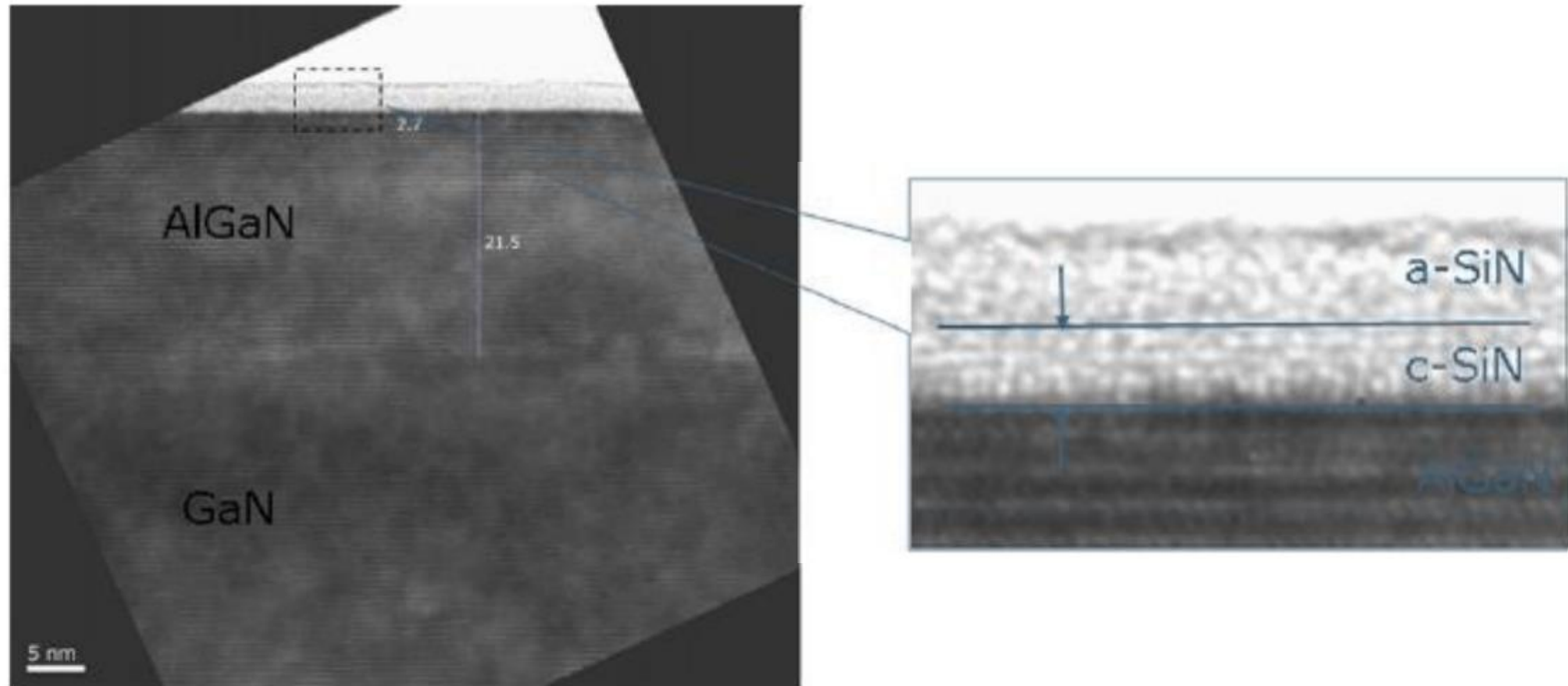
HEMT Surface Passivation with SiN



Cleaning procedures for GaN are based on nitridation (N₂ plasmas, NH₃ plasmas, (NH₄)₂S, Thermal treatments in N₂ or NH₃) + ex-situ SiN passivation



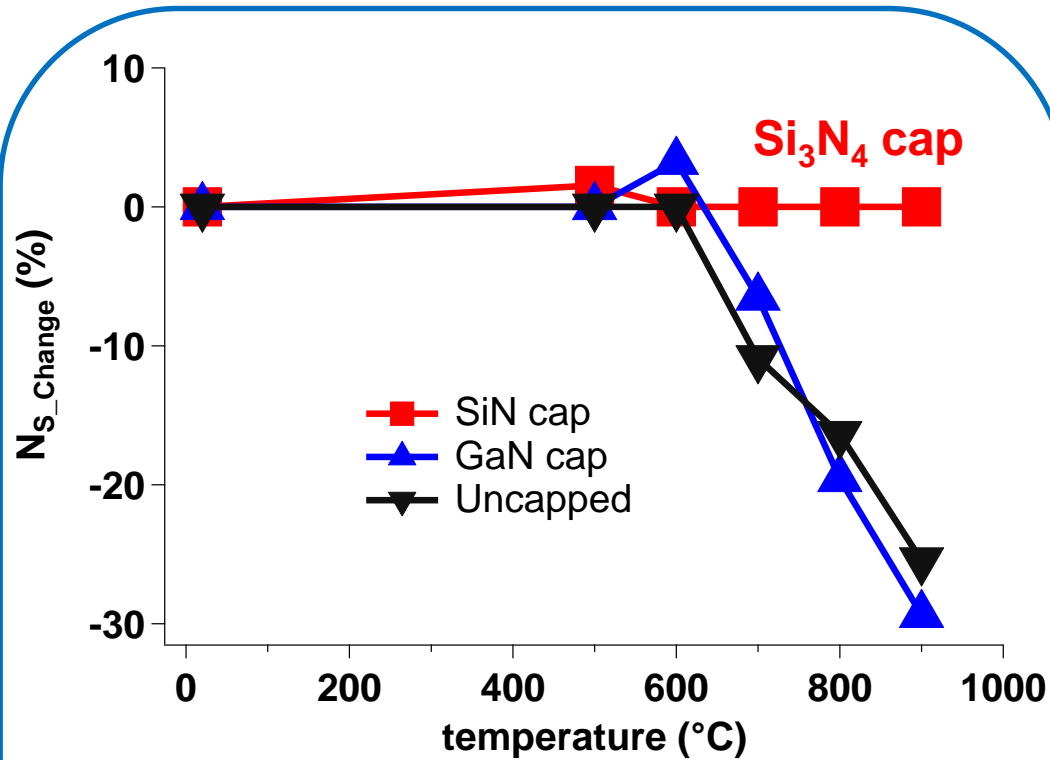
HEMT Surface Passivation with in-situ SiN



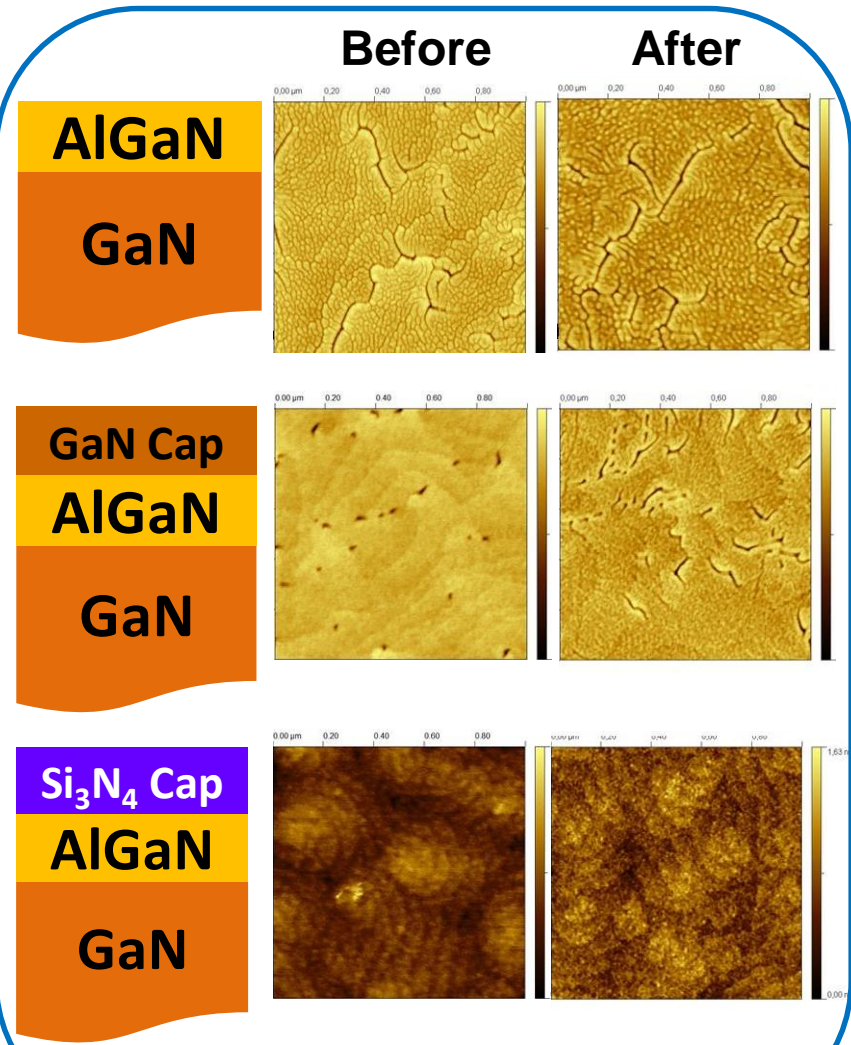
SiN deposited inside the MOCVD tool ending the heterostructure growth

- Clean interface
- Crystalline interface
- Relaxation prevention

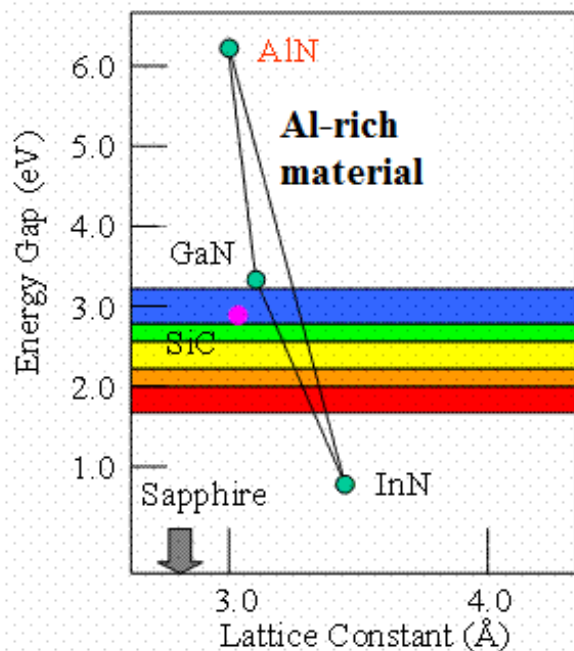
Benefit of in-situ SiN cap layer



EXPERIMENT : The temperature was ramped up in vacuum to 900°C using a step of 100°C for 30 min. After each step Hall measurement was performed at RT.



AlN/GaN heterostructure



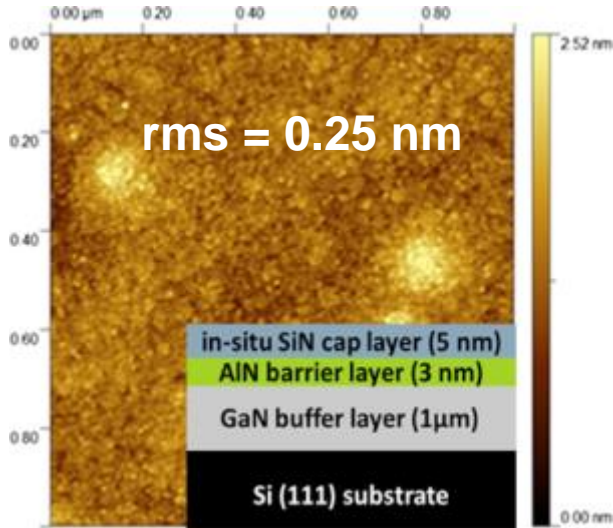
An old idea but difficult to achieve:

Use of the widest III-N bandgap (AlN), theoretically the most attractive material to maintain high polarization while using ultrathin barrier

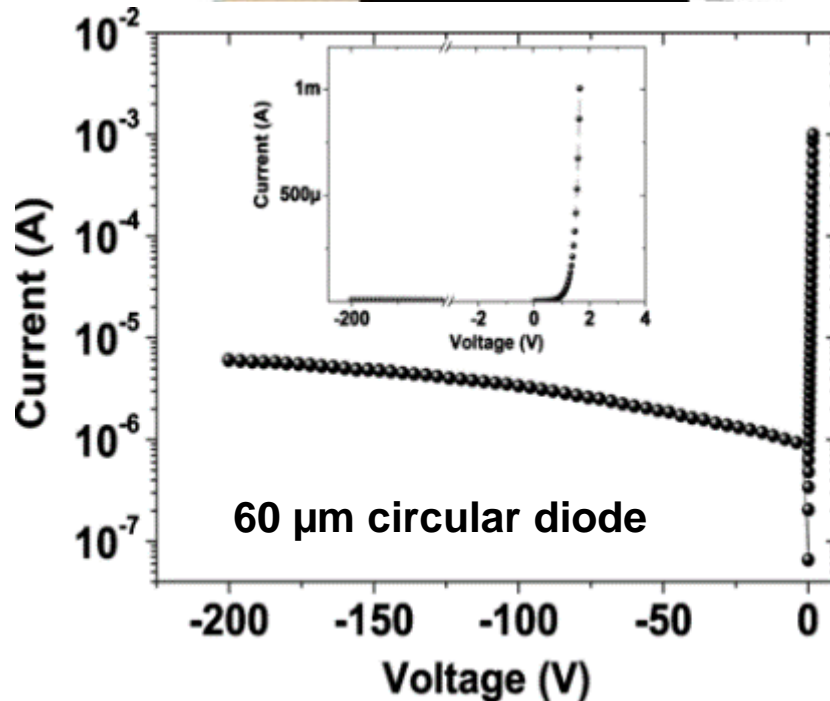
Challenges:

- Leakage through / on top of the ultrathin barrier
- Leakage following extra PECVD SiN passivation
- Leakage due to punch-through effects (electron injection into the buffer)
- Trapping effects: surface close to the 2DEG

Low gate leakage through only 3 nm AlN barrier



- High surface quality owing to the in-situ SiN preventing strain relaxation

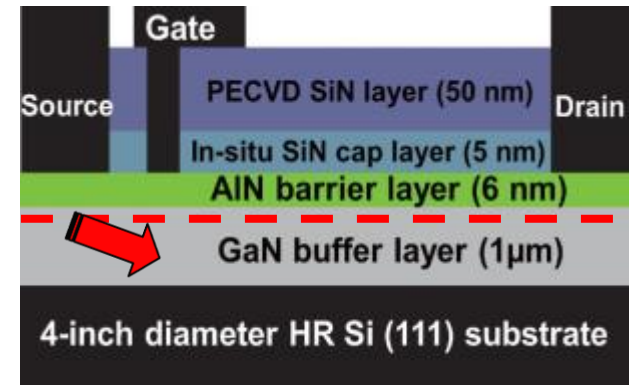
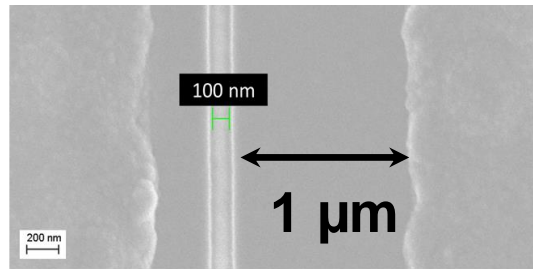
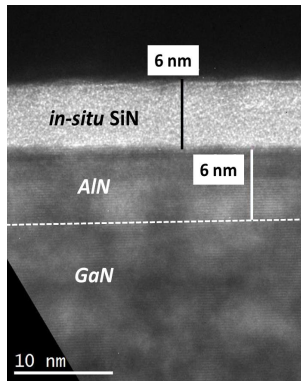


- Low Schottky gate leakage deposited directly on the AlN barrier layer (see forward diode)

Buffer confinement for high voltage operation

What about high voltage operation when using ultrashort GaN devices?

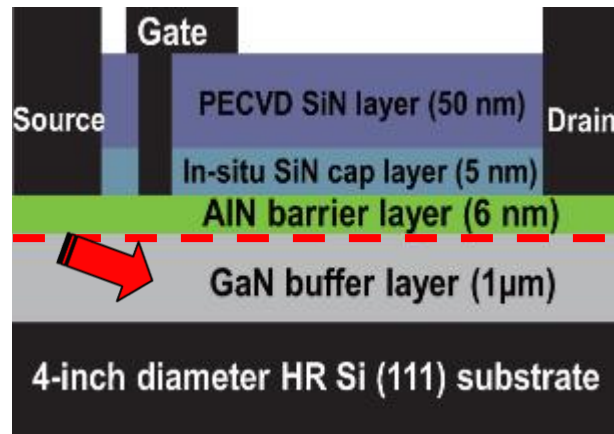
Ultrathin barrier + High $N_s > 2 \times 10^{13} \text{ cm}^{-2}$ + Short $L_{GD} \text{ \& } L_G$ + $V_{DS} > 20 \text{ V}$ = Extremely high electric field



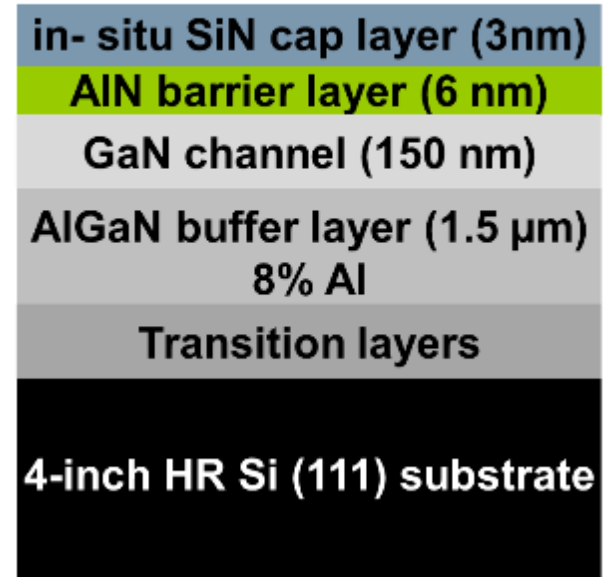
Poor electron confinement can be expected even if the material and processing are of high quality

Back barrier needed

Punch-through effect: Poor electron confinement even if the material and processing are of high quality



DHFET

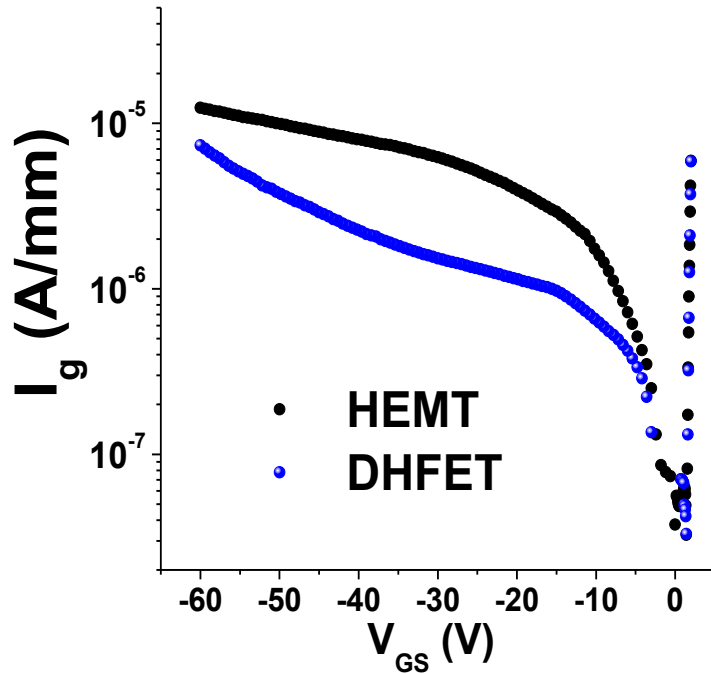


Introduction of an AlGaIn back barrier to prevent the electron injection under high bias (double heterostructure: DHFET)

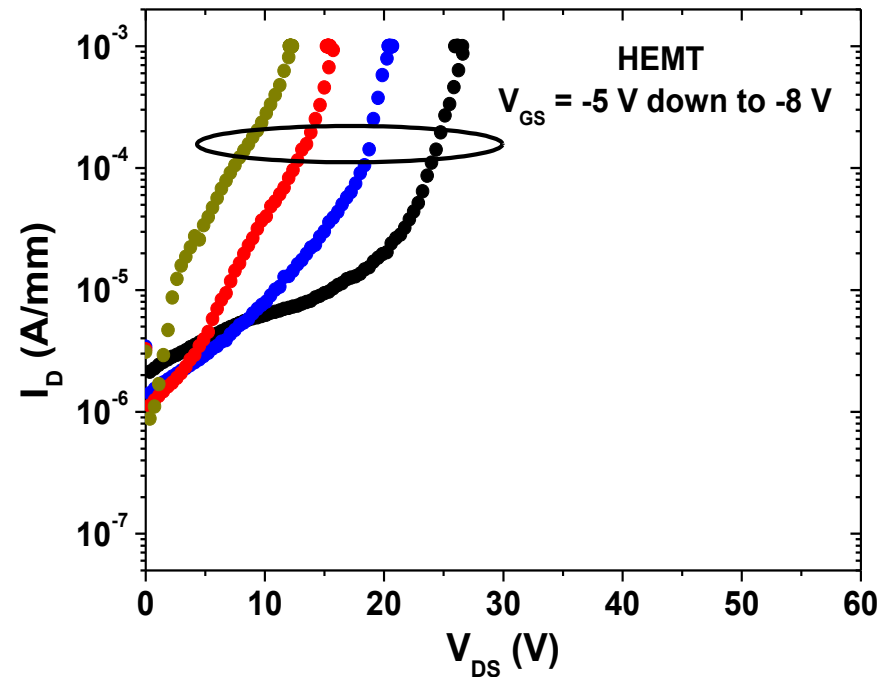
AlN/GaN DHFET under high bias

$L_G = 200$ nm

Gate leakage current



3-terminal breakdown voltage

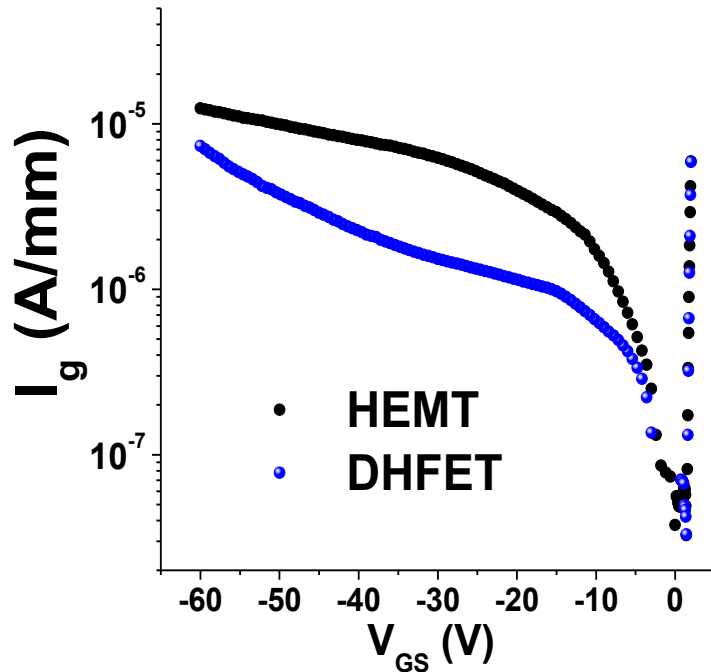


- Low Gate leakage current in both cases
- Huge drain leakage current: punch-through effect !

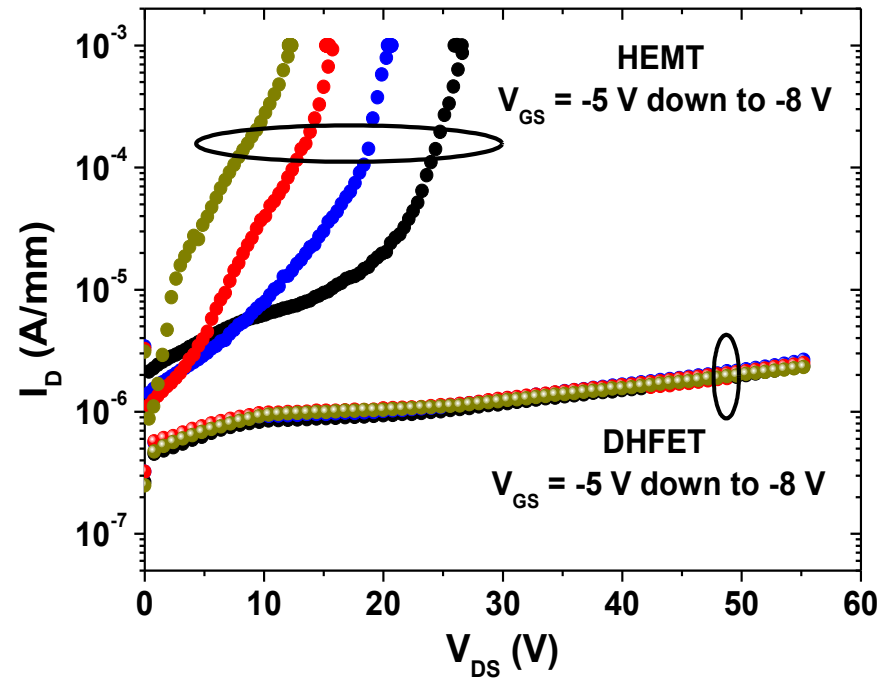
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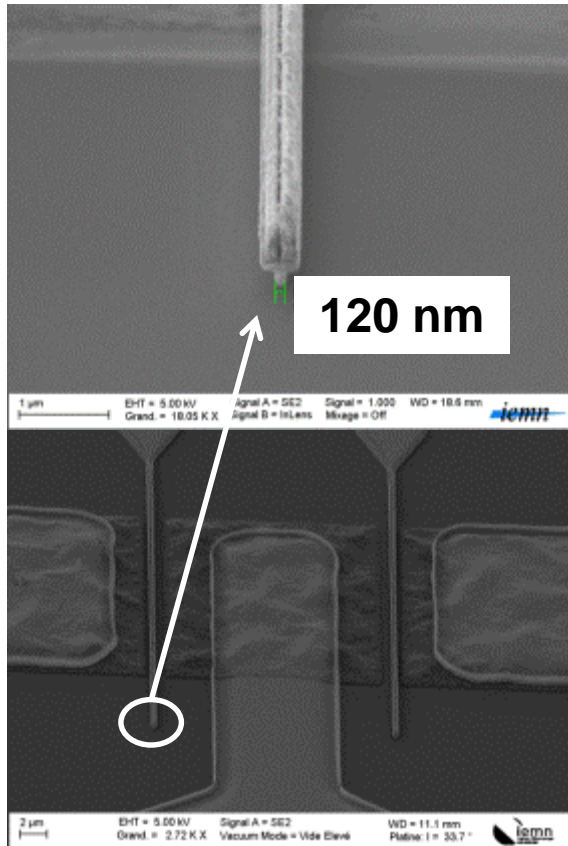


3-terminal breakdown voltage

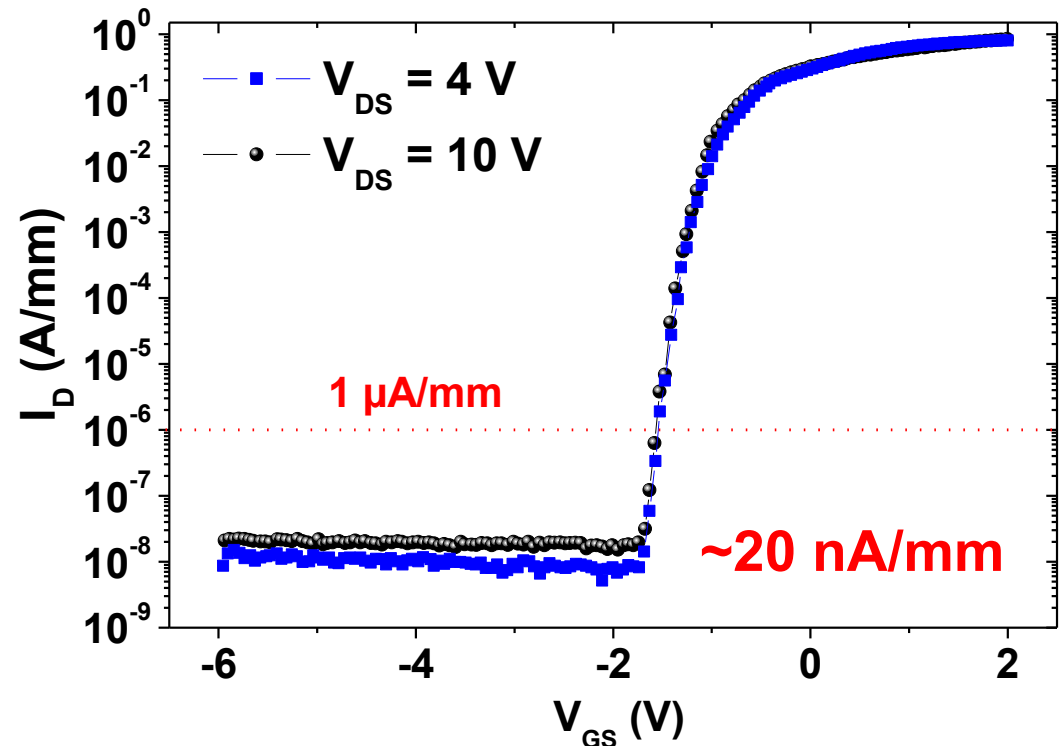


- Low Gate leakage current in both cases
- Low drain leakage: punch-through effect significantly reduced resulting in high V_{BK} ($2 \mu\text{A/mm}$ @ $V_{DS} = 50$ V)

Improvement of the electron confinement under high electric field to further push the GaN performance limits

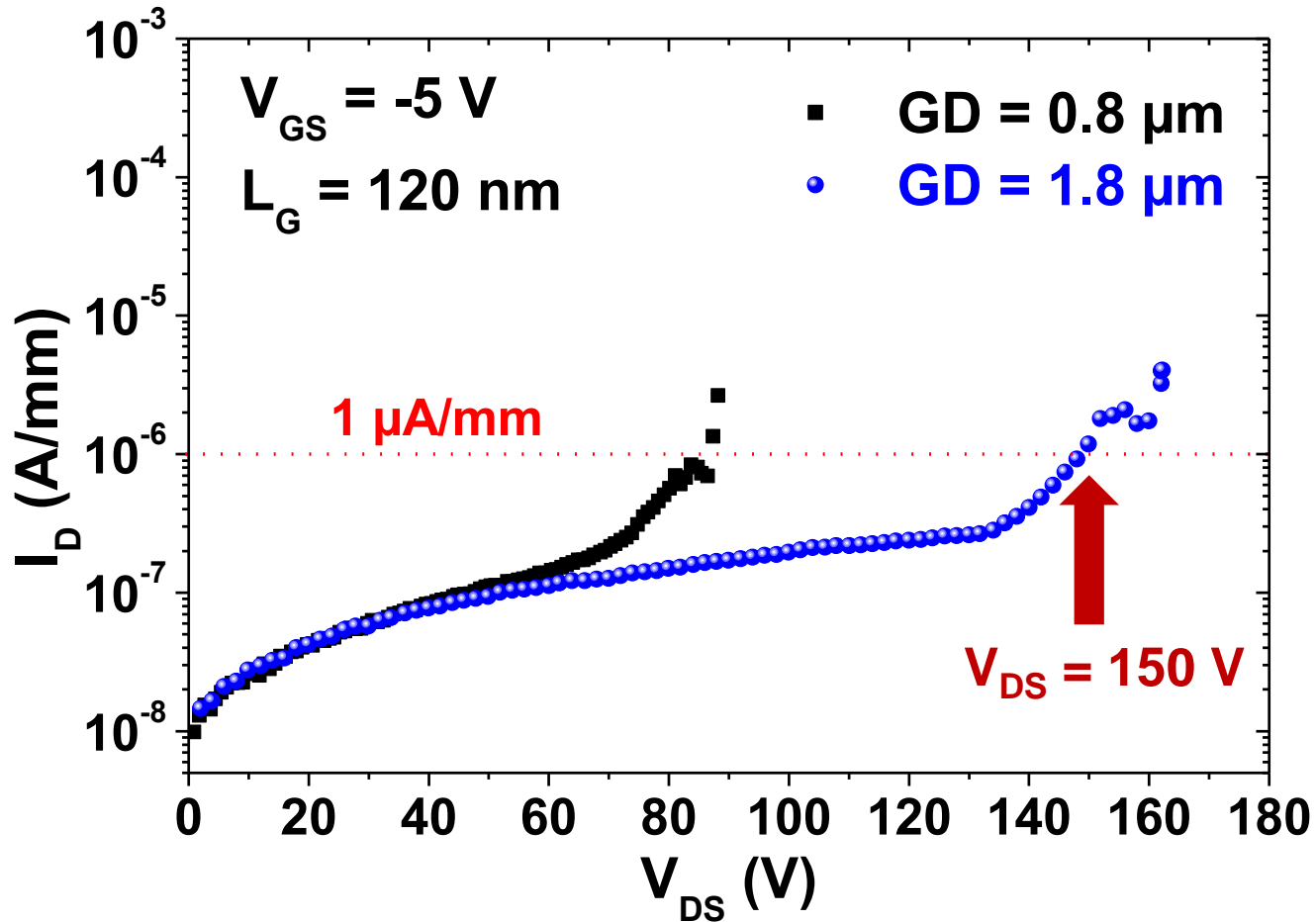


$L_g = 120 \text{ nm}$, $\text{GD} < 2 \mu\text{m}$



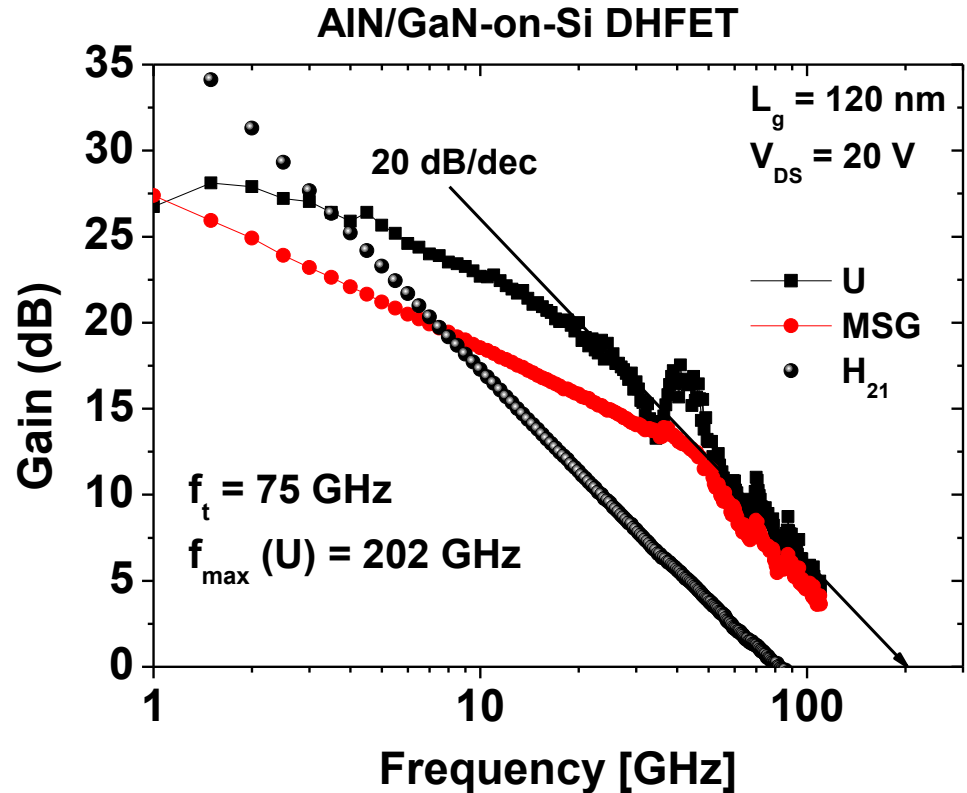
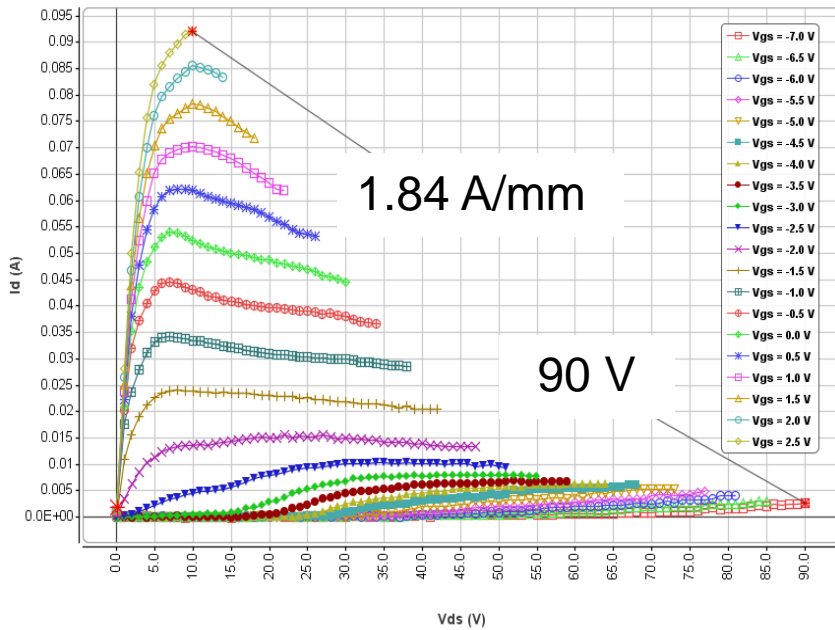
- Outstanding subthreshold leakage current $< 1 \mu\text{A/mm}$ for sub-150 nm L_g while using a Schottky contact on $< 5 \text{ nm}$ AlN barrier thickness showing an excellent electron confinement owing to an optimized buffer configuration

Improvement of the electron confinement under high electric field to further push the GaN performance limits



BV about $100 \text{ V}/\mu\text{m}$ for $GD < 2 \mu\text{m}$ while using L_g sub-150 nm with extremely low leakage current $< 1 \mu\text{A/mm}$ up to 150 V which is quite untypical

High combination: $f_{\max} \times V_{\text{BK}}$

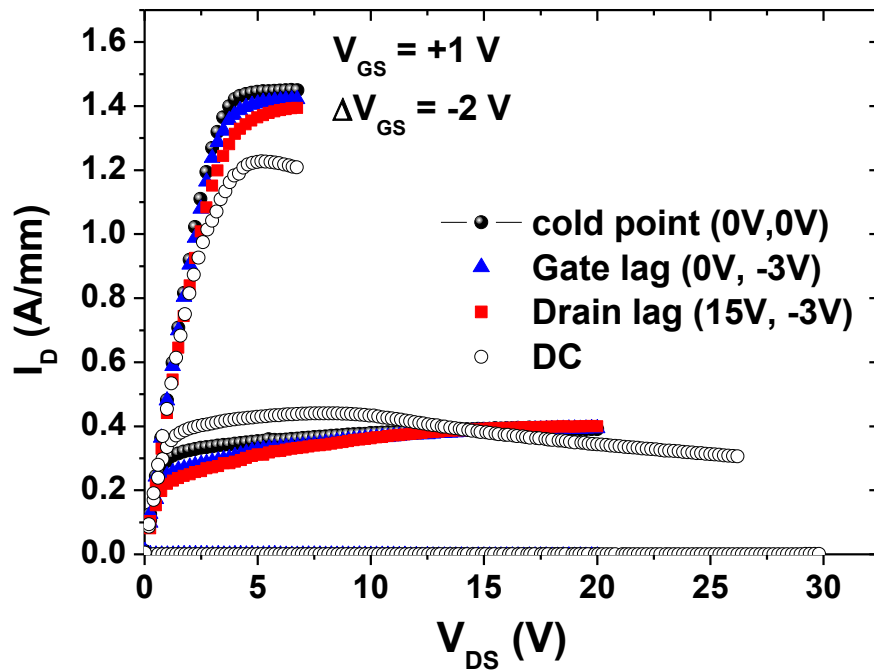


Fully reproducible devices delivering both high breakdown and high f_{\max}

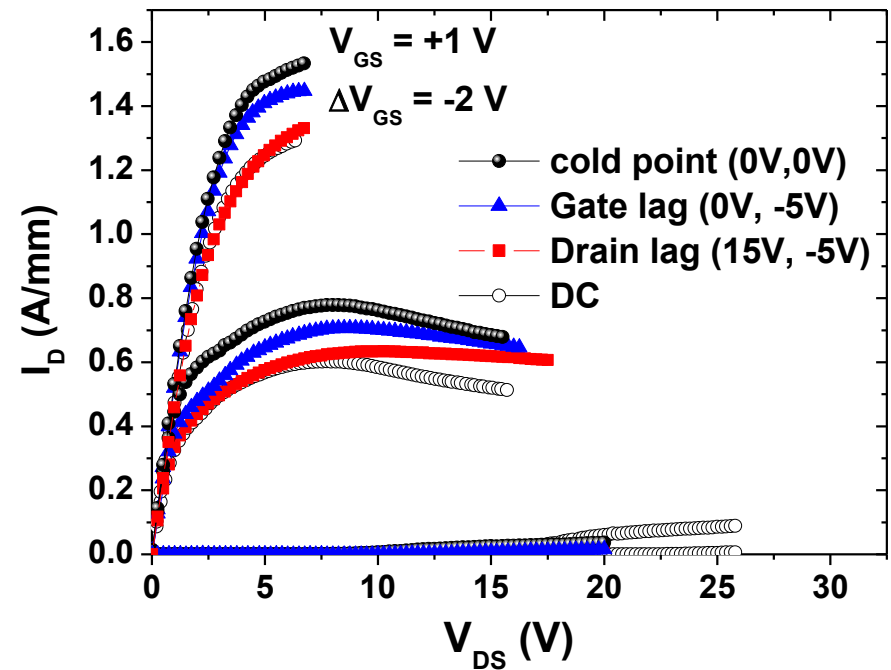
Improved dynamic behavior in short GaN devices

AlN/GaN devices using a critical SiN cap thickness
(L_G down to sub-100 nm)

DHFET: $L_g = 200$ nm



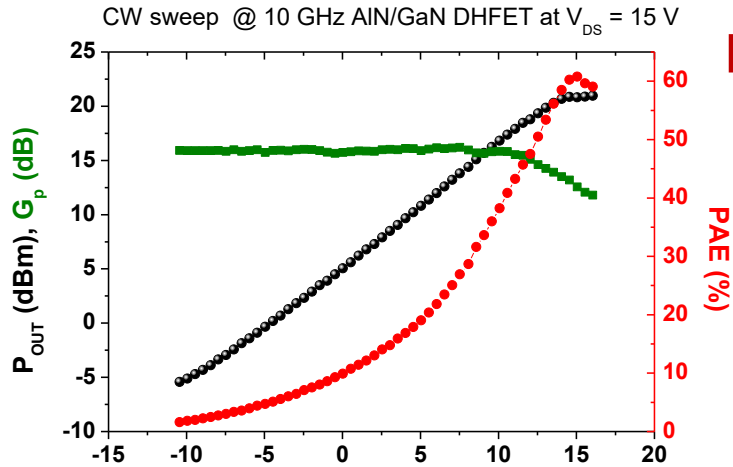
DHFET: $L_g = 80$ nm



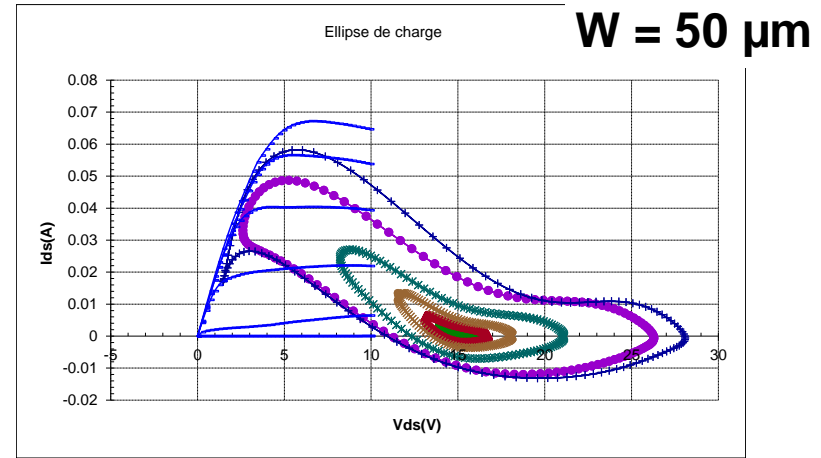
- Low trapping effects under 500 ns pulse width in highly scaled AlN/GaN devices

0.15 μm AlN/GaN-on-SiC power measurement @ 10 and 18 GHz

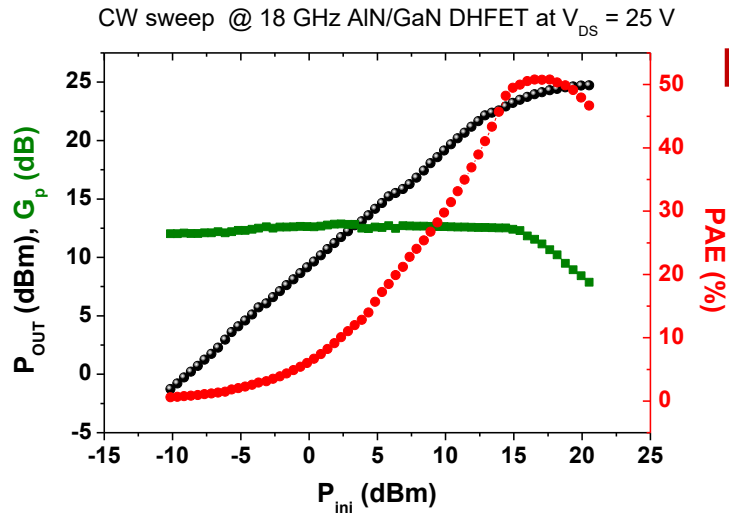
4 nm barrier thickness !



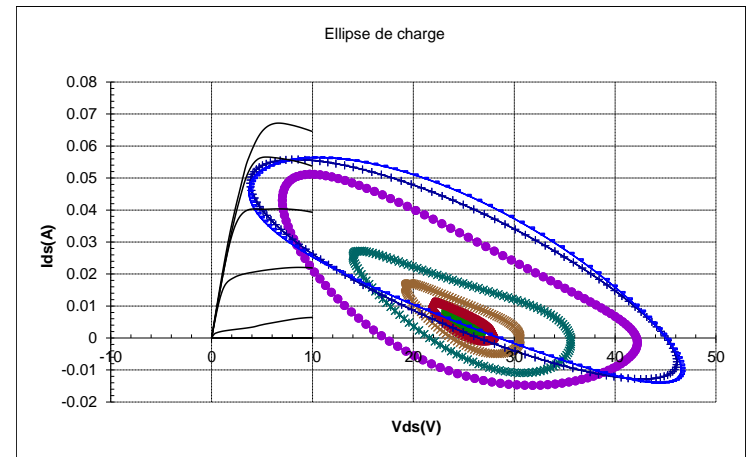
**PAE > 60%
@ 10 GHz**



Load lines reflect the low RF dispersion
The power gain confirms the high frequency performances



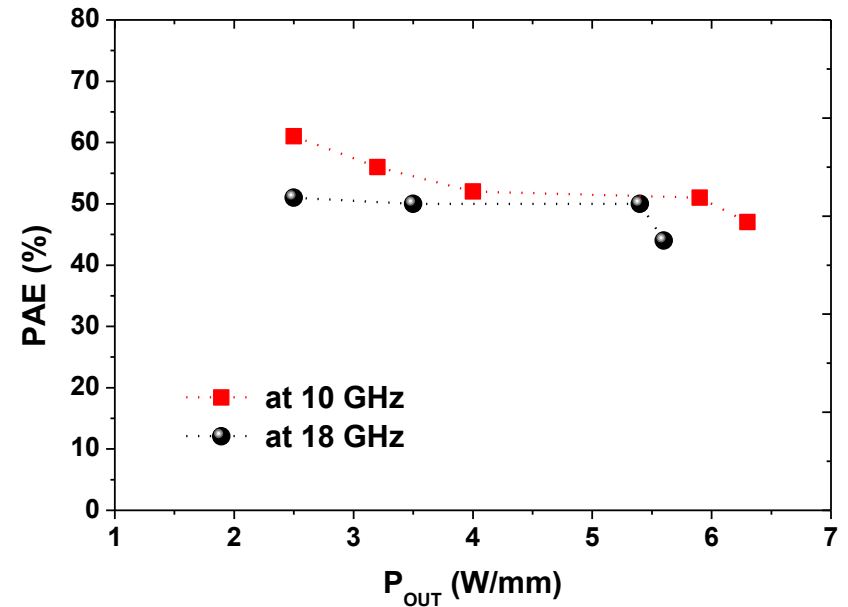
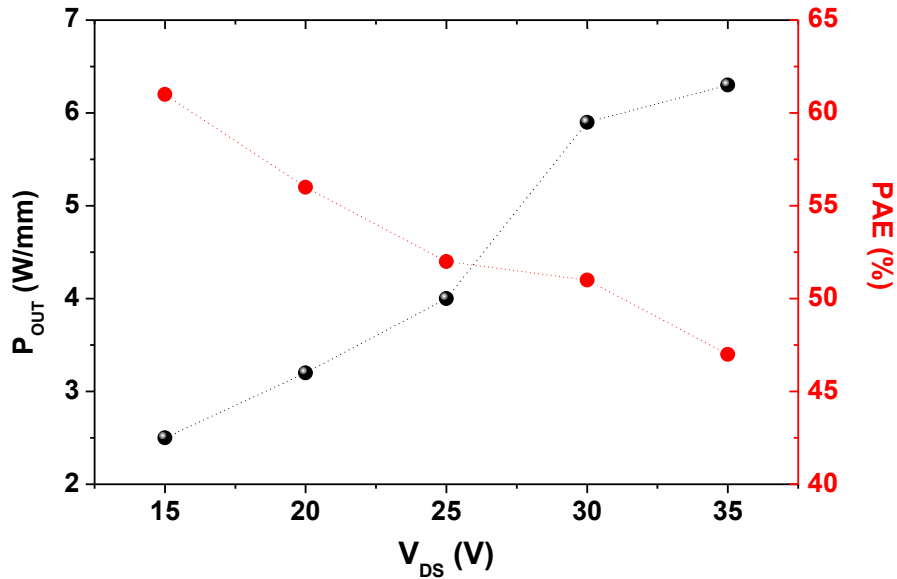
**PAE > 50%
@ 18 GHz**



High PAE for the first time on sub-10 nm barrier GaN devices

0.15 μm AlN/GaN-on-SiC power measurement @ 10 and 18 GHz

Power performance @ 10 GHz AlN/GaN DHFET vs. V_{DS}

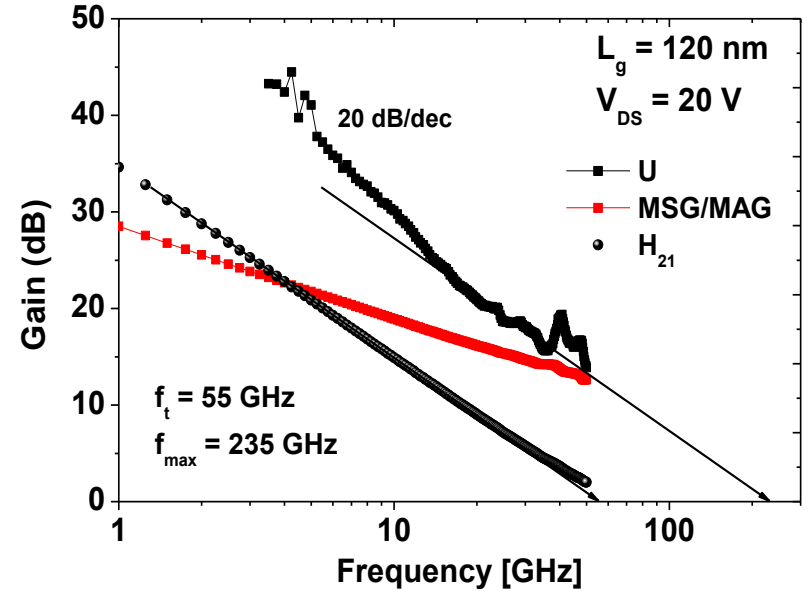
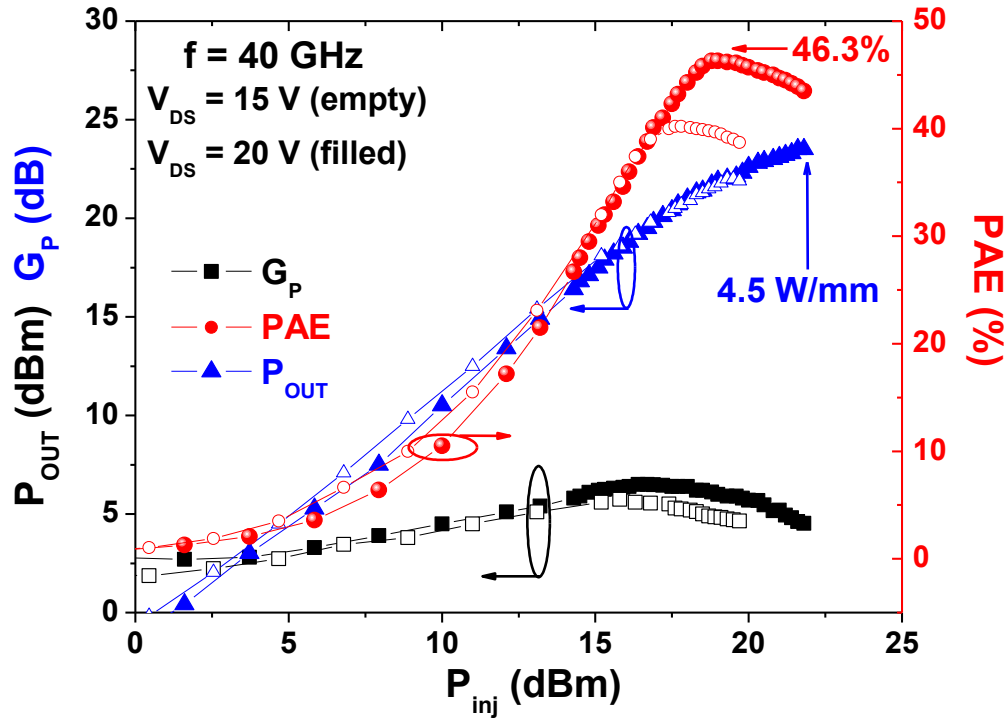


- High bias operation with ultrathin barrier GaN devices
- High PAE maintained up to high power densities

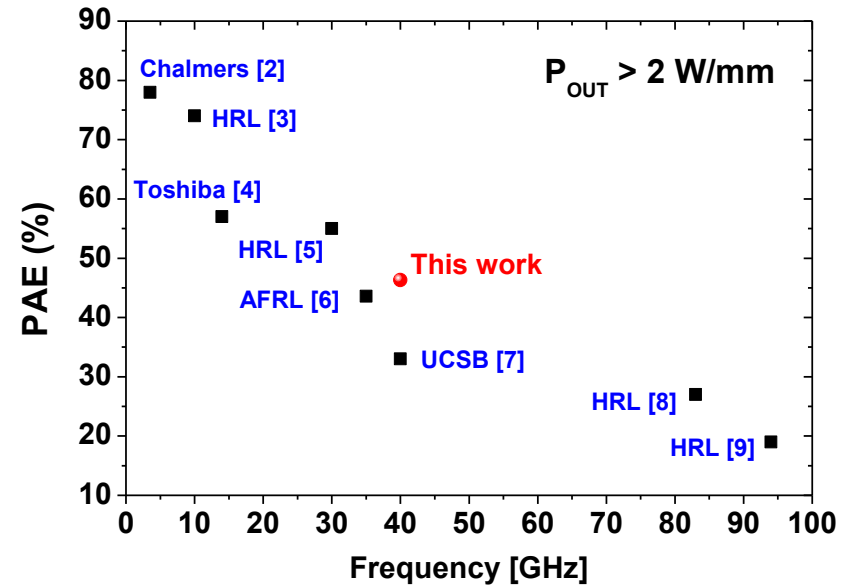
0.12 μm AlN/GaN-on-SiC power measurements @ 40 GHz

Barrier thickness of 4 nm

$W = 50 \mu\text{m}$



**State-of-the-art PAE @ 40 GHz
for GaN devices**



Off-state test: not an issue up to high bias

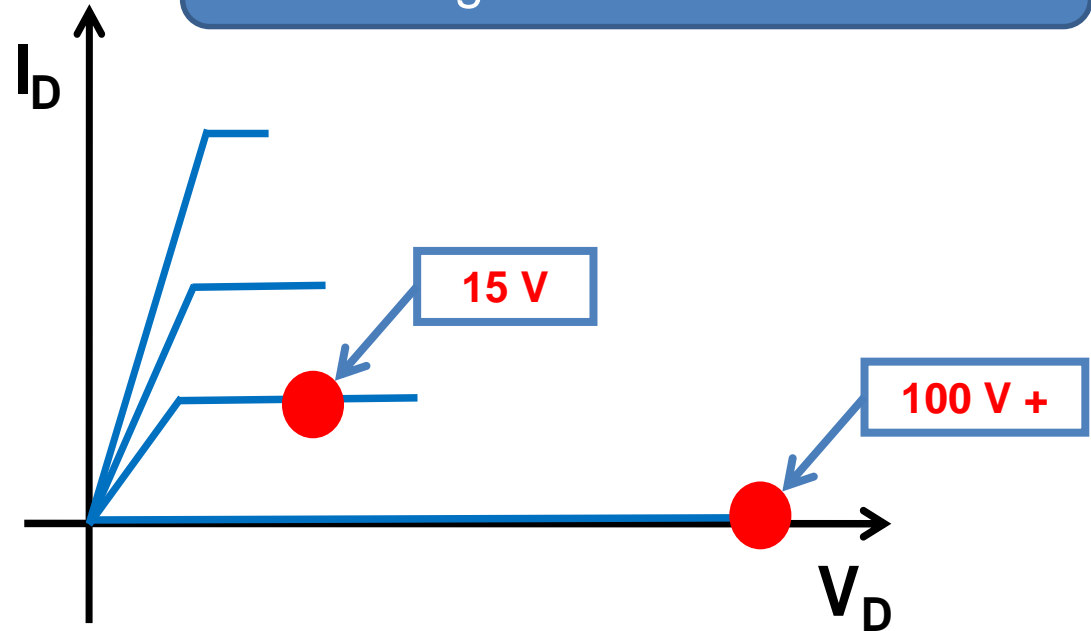
surface robustness enhancement owing to the in-situ SiN cap layer

Optimum electron confinement owing to the back barrier

$L_G = 150 \text{ nm}$

$GD = 2 \text{ }\mu\text{m}$

$f_{\text{max}} \geq 200 \text{ GHz}$



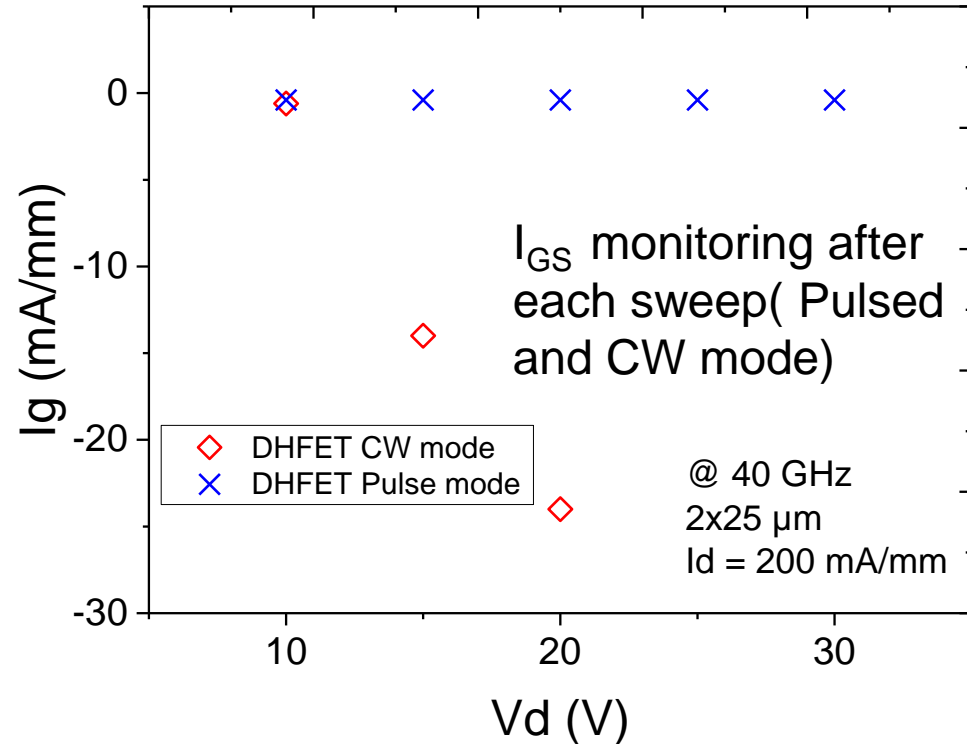
Thermally-limited in semi-on conditions for $V_{DS} \approx 15$ to 20 V

Poor thermal dissipation of the AlGaN back barrier

Device robustness

- DHFET in CW mode
 - Strong degradation
- DHFET in Pulse mode
 - No degradation

Pulse Mode reduces the self-heating effect in the transistor



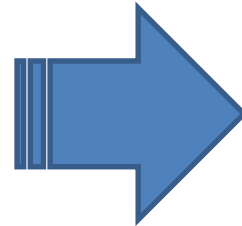
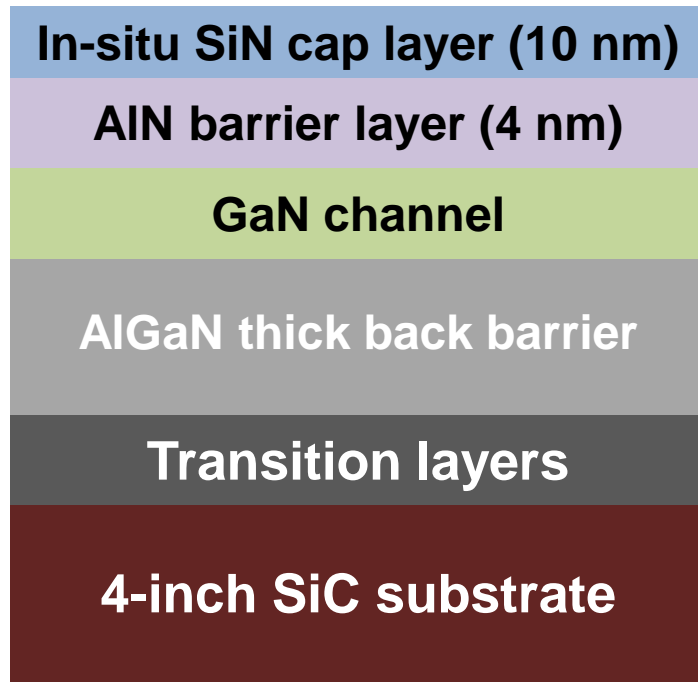
Degradation due to self heating resulting from the poor thermal dissipation of the thick AlGaN back barrier

AlN/GaN DHFET is a very good solution up to about 15 V drain bias operation with excellent performance but other buffer configurations are needed to operate beyond 15 V

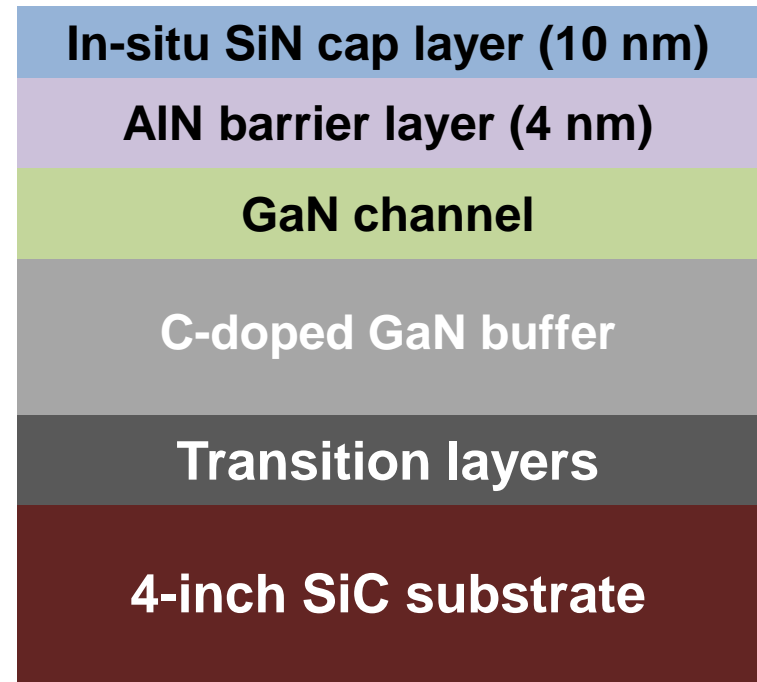
For short GaN devices, it seems that hot electron is one of the prime factor degrading the reliability.

Change in the buffer layers: From AlN/GaN DHFET to C-doped HEMT

DHFET

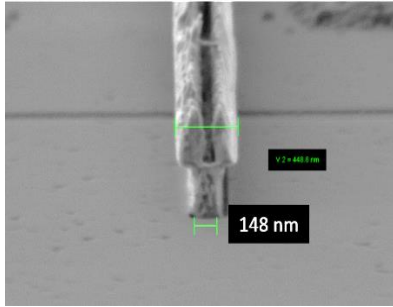


HEMT

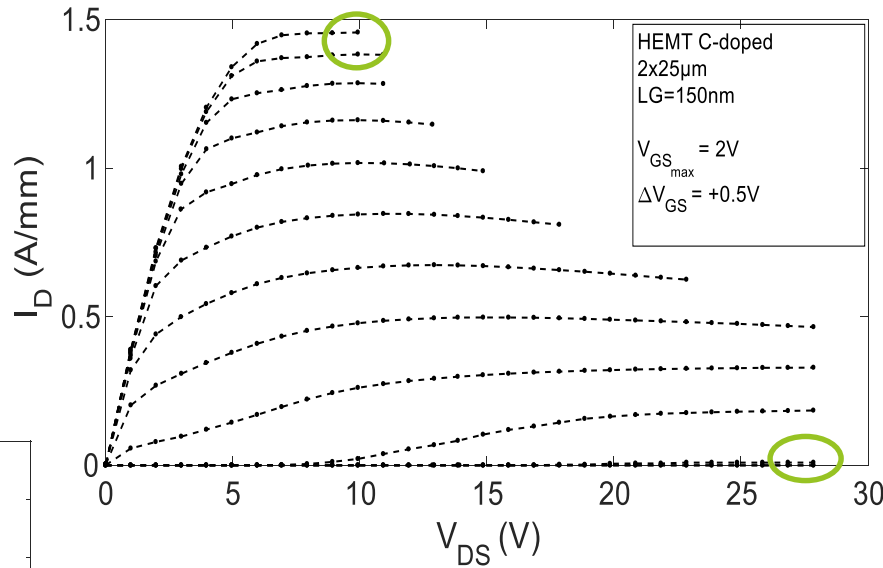


Much better thermal dissipation expected in HEMT configuration
but what about electron confinement and trapping effects

DC Characteristics of AlN/GaN C-doped HEMT



Lg=150 nm



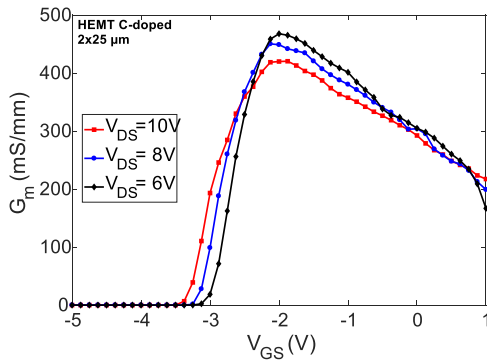
➤ **1.4 A/mm @ $V_{GS} = 2V$**
High current density
owing to high N_s

➤ **Low leakage current**
(<1μA/mm)

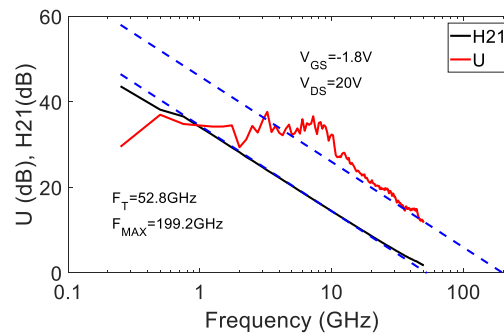
➤ **High electronic**
confinement

➤ **High frequency**
performance
 $F_T = 60GHz / F_{MAX} = 200GHz$

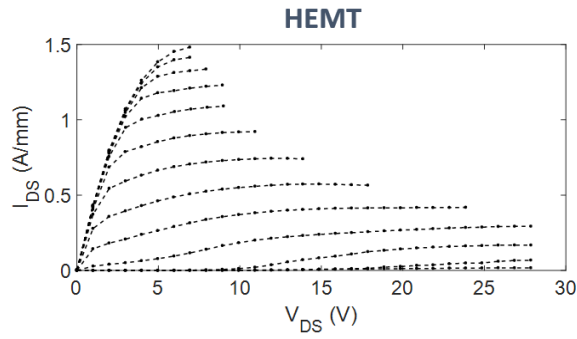
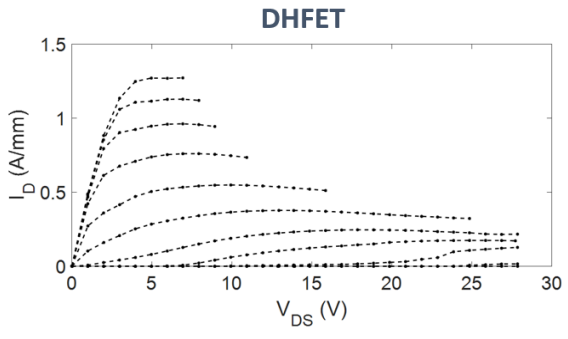
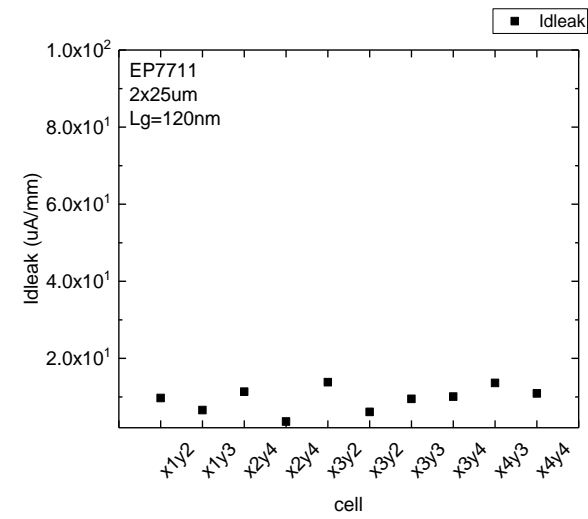
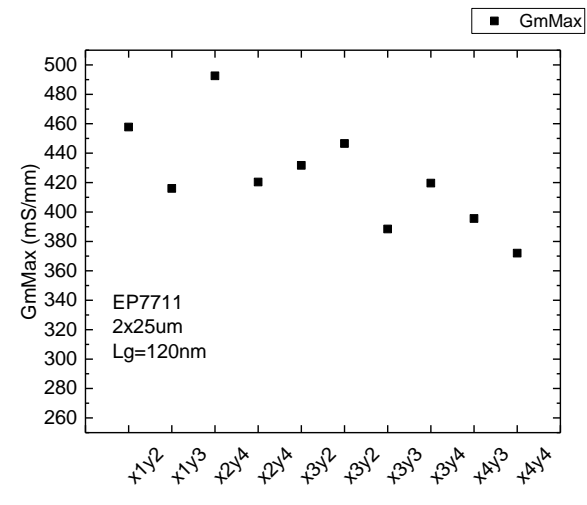
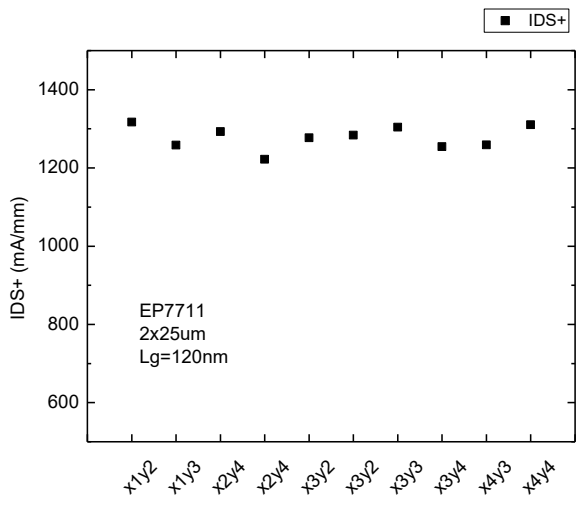
➤ **Operation bias up to**
30V with high gain @
40 GHz



450 mS/mm @ $V_{DS} = 10V$
High G_m due to the gate
length + barrier thickness

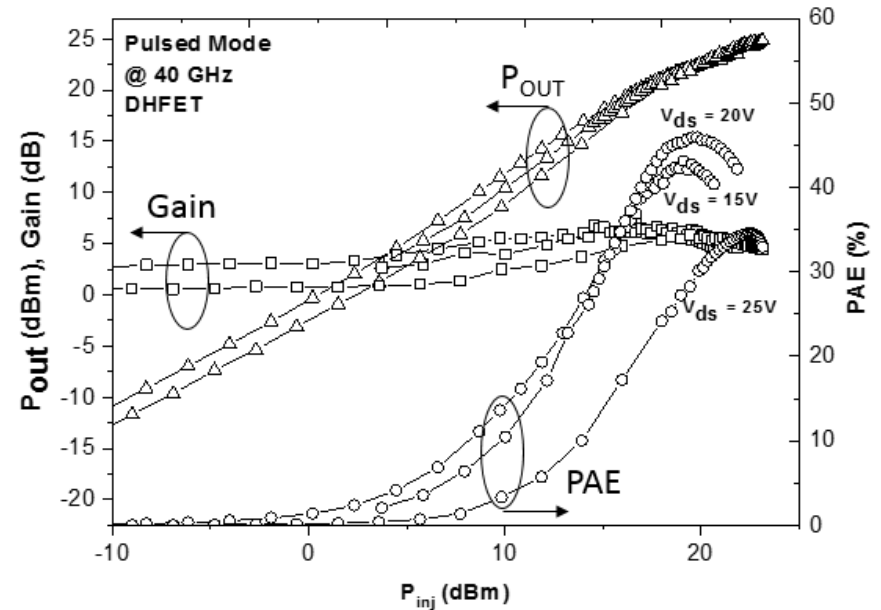
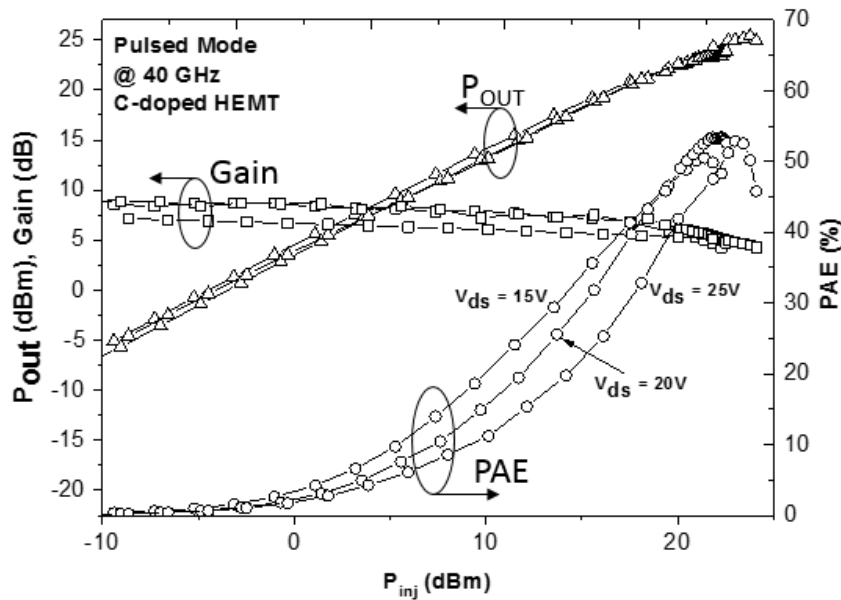


Comparison of the AlN/GaN DHFET and HEMT using $L_G = 120$ nm



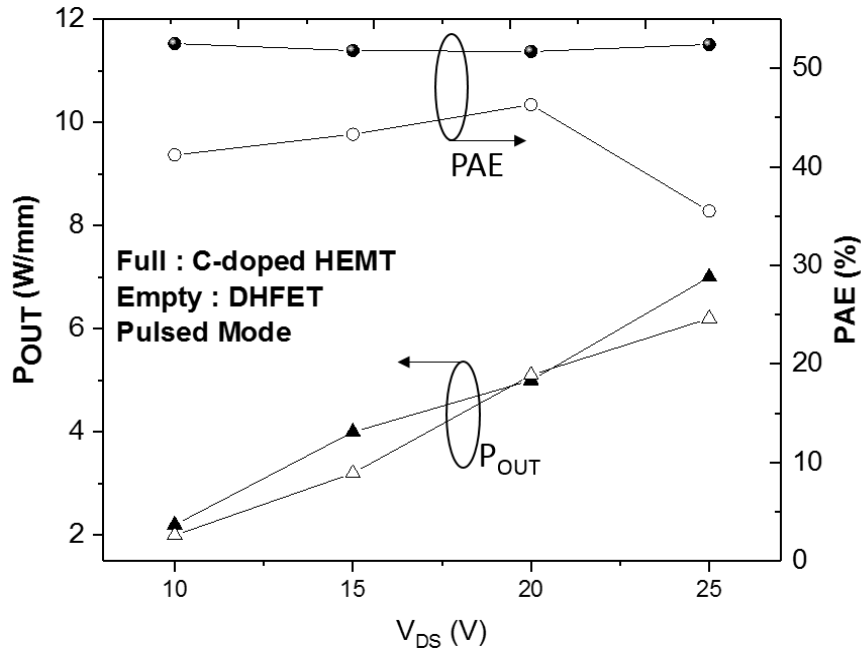
- ✓ Similar transconductance
- ✓ Higher current density (higher N_s)

Comparison of the AlN/GaN DHFET and HEMT using $L_G = 120$ nm

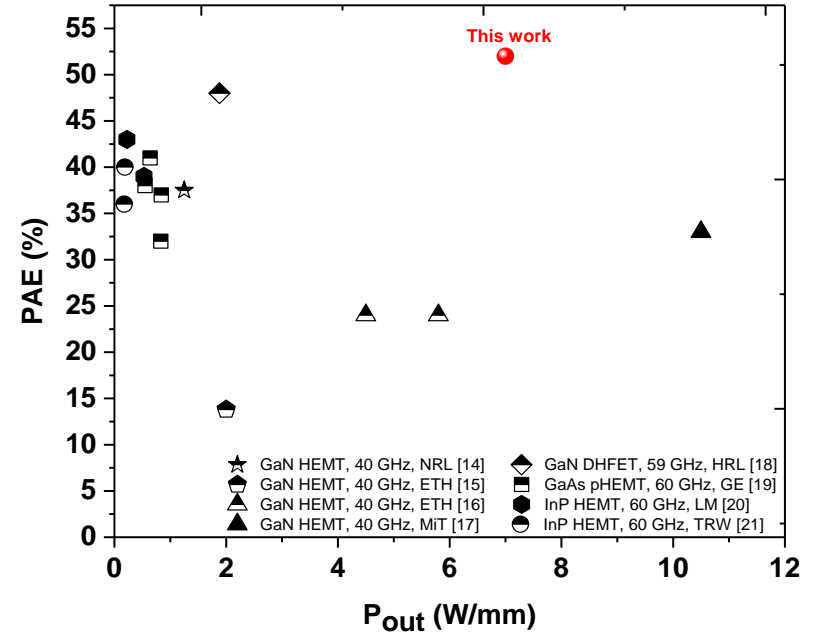


- ✓ High power density in both cases
- ✓ Strong degradation of the PAE at $V_{DS} = 25V$ for the DHFET due to self-heating despite the pulsed mode.

Comparison of the AlN/GaN DHFET and HEMT using $L_G = 120$ nm



PAE @ 40 GHz

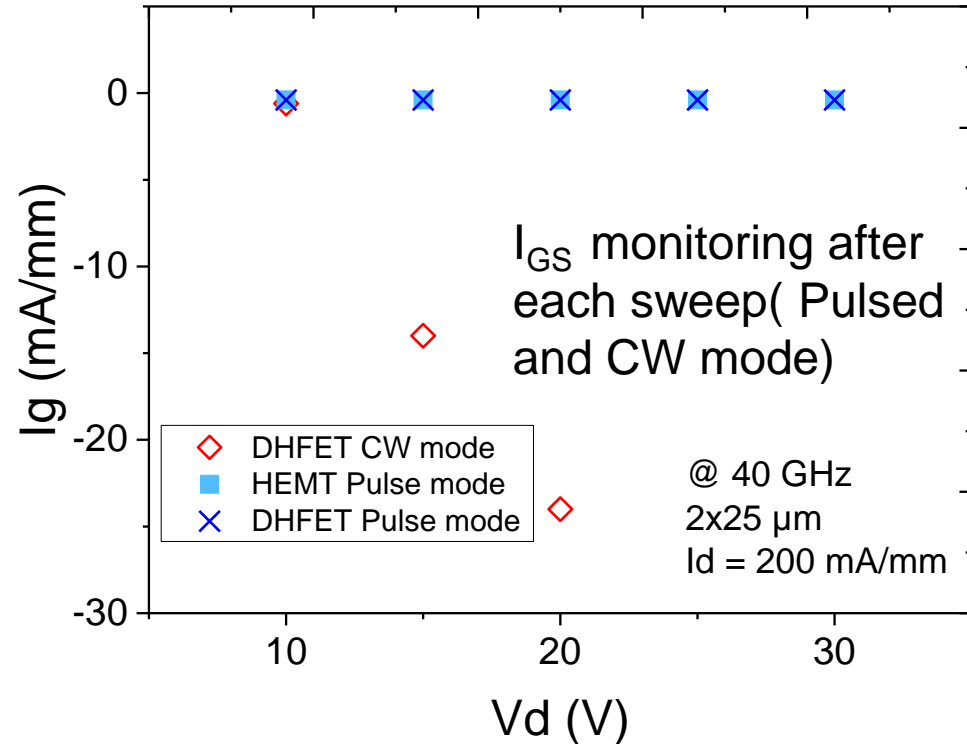


- ✓ Better PAE for the HEMT attributed to a better thermal dissipation
- ✓ State-of-the-art PAE @ 40 GHz

AlN/GaN Device robustness

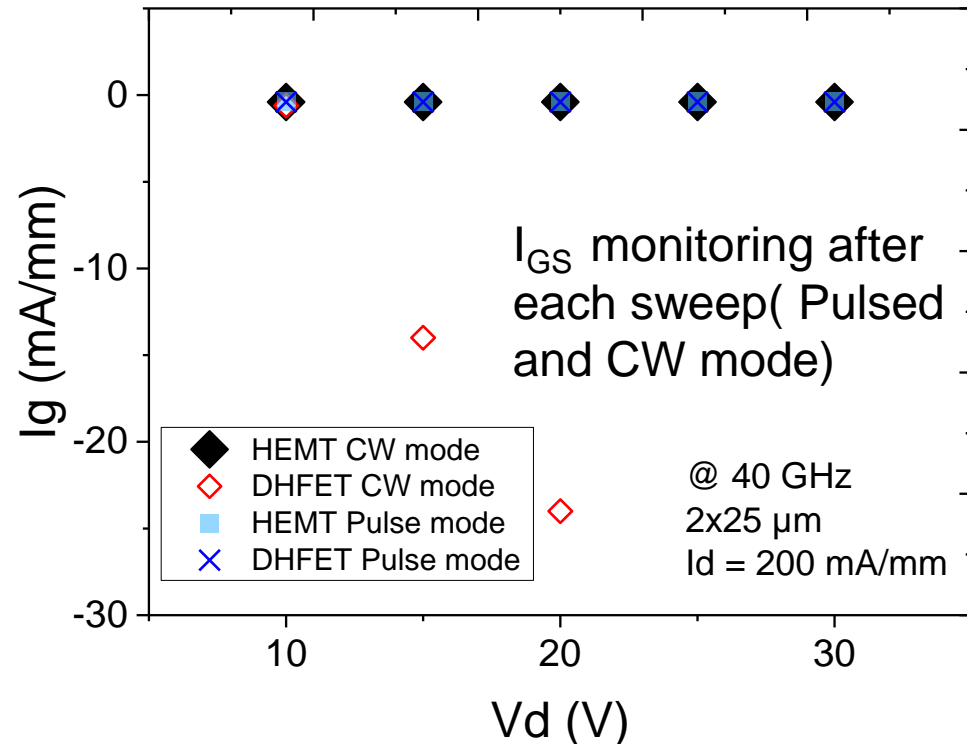
- **DHFET in CW mode**
 - Strong degradation
- DHFET in Pulse mode
 - No degradation
- HEMT in Pulse mode
 - No degradation

Pulse Mode reduces the self-heating effect in the transistor



AlN/GaN Device robustness

- DHFET in CW mode
 - Strong degradation
- DHFET in Pulse mode
 - No degradation
- HEMT in Pulse mode
 - No degradation
- HEMT in CW mode
 - No degradation



- The absence of degradation shows the superior thermal conductivity of the carbon-doped GaN buffer as compared to the AlGaN back barrier
- Owing to the better heat dissipation through the buffer, the C-doped HEMT can operate up to $V_{DS}=30\text{V}$ against $V_{DS}=15\text{V}$ for the DHFET

Conclusion

- Possibility to achieve high breakdown (close to 100 V/ μm) under high electric field, with low leakage, and high PAE while using highly scaled sub-10 nm barrier GaN devices
- A critical in-situ SiN cap layer thickness is helpful to enhance the surface robustness resulting in superior device performance and reliability
- Buffer configuration is a key to break the trade-off between electron confinement and self-heating

Bright future for GaN !

Overcoming all challenges in highly scaled nitrides for breakthrough RF performances up to 100 GHz and above will definitely be achieved !

