

Next generation of GaN-on-Silicon power devices

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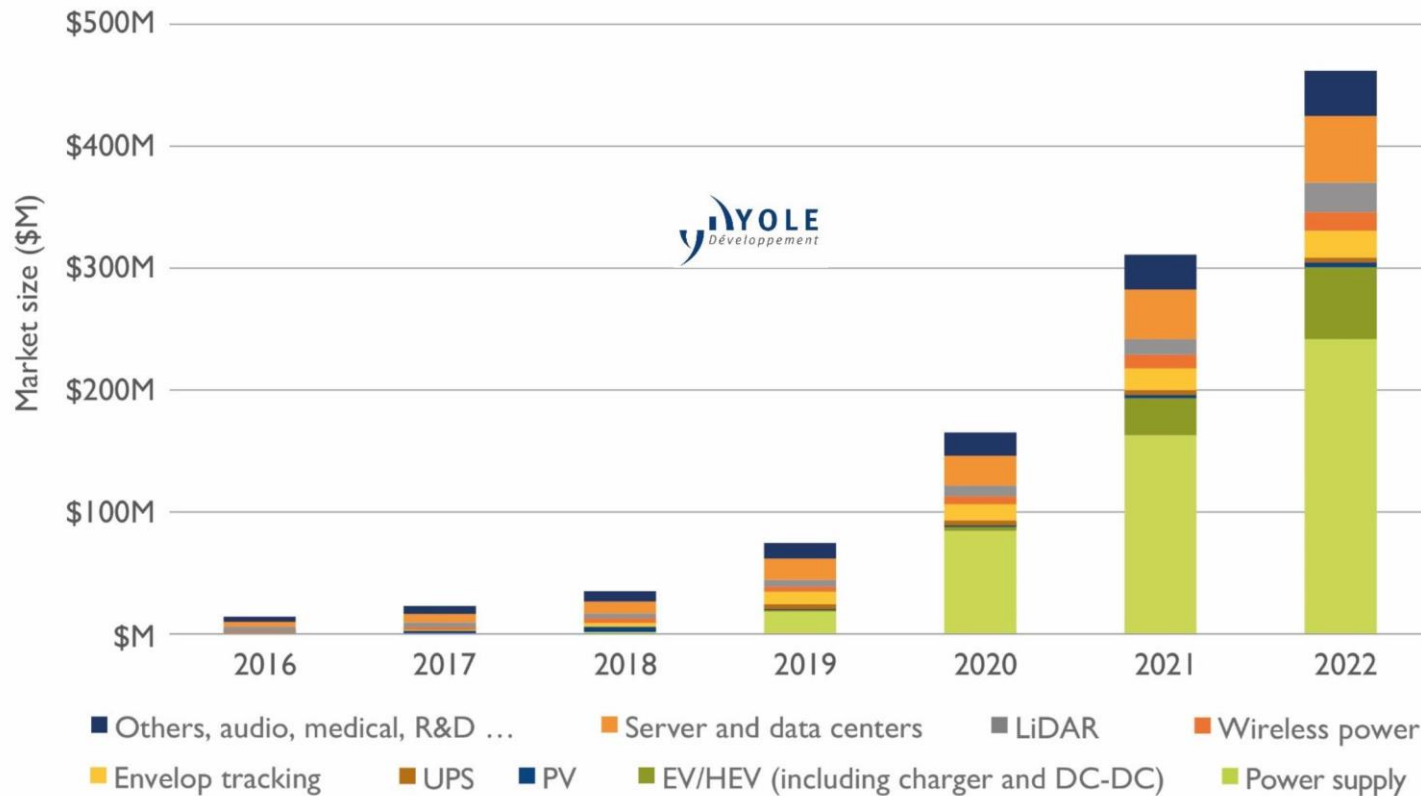


Outline

- Introduction
- Towards 1200 V-rated GaN/Si buffers
(2 examples of successful achievements)
 - High voltage epitaxy assessment
 - Substrate ramp up to 1200 V
- Enhancement of GaN/Si BV using substrate removal technique
 - High voltage DC characterizations
 - Trapping assessment up to 3 kV
- Conclusion

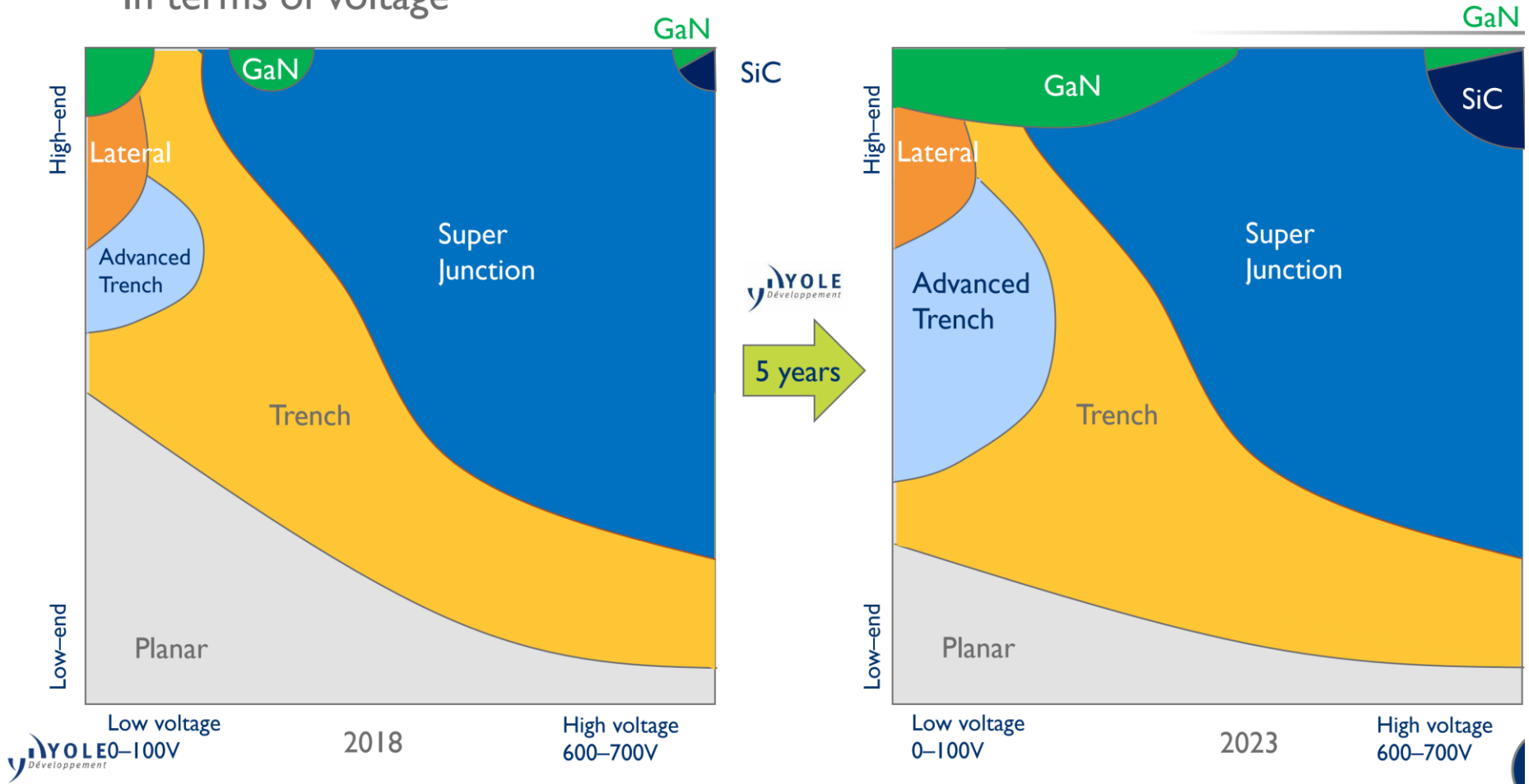
GaN power device market size split by application (\$M)

(Source: Power GaN 2017: Epitaxy, Devices, Applications, and Technology Trends 2017 report, Yole Développement, October 2017)



FUTURE MARKET DEVELOPMENT

In terms of voltage



YOLE Développement
LE0-100V

2018

High voltage
600-700V

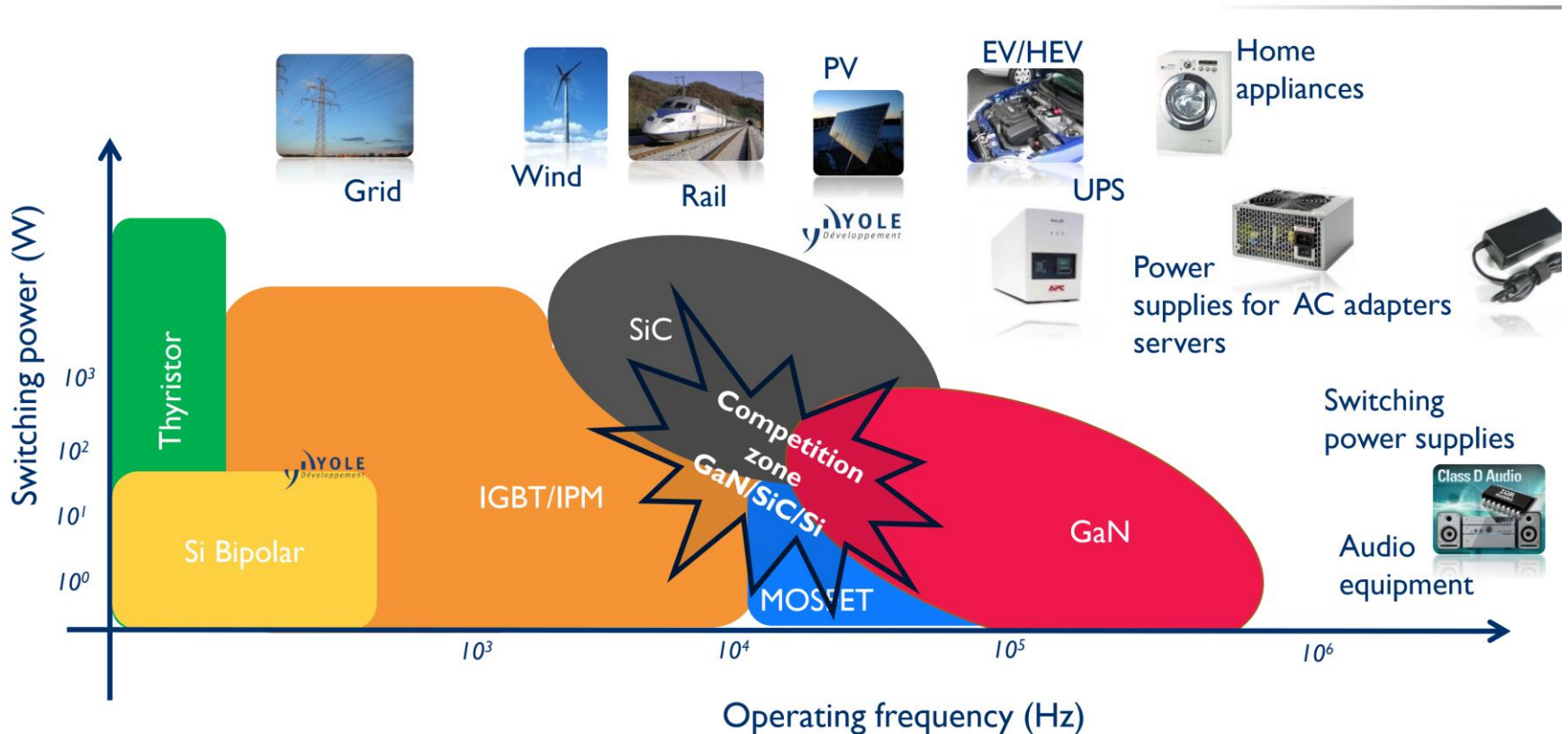
Low voltage
0-100V

2023

High voltage
600-700V

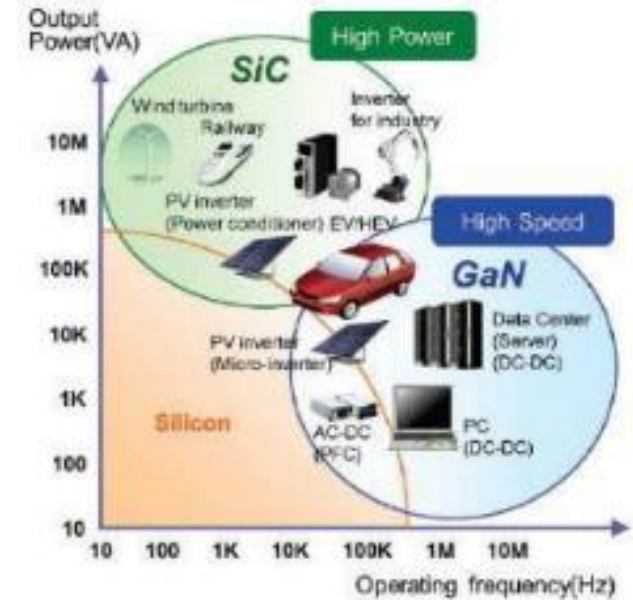
POWER VS FREQUENCY ON ELECTRONICS

Power device technology positioning (2018)



GaN best choice for high speed power devices

GaN LATERAL devices
→ highest electron mobility
→ operation at higher frequency



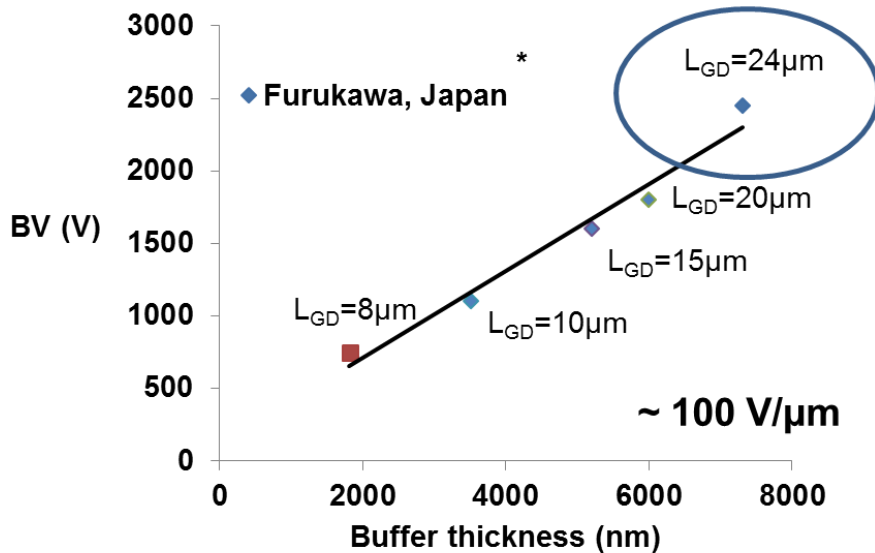
For any voltage range that GaN / Si LATERAL devices can cover in a reliable way (e.g. low trapping effects) and with high enough blocking voltage margin, it should be the best choice for power applications based on the cost / performance ratio

Breakdown limitation of GaN/Si

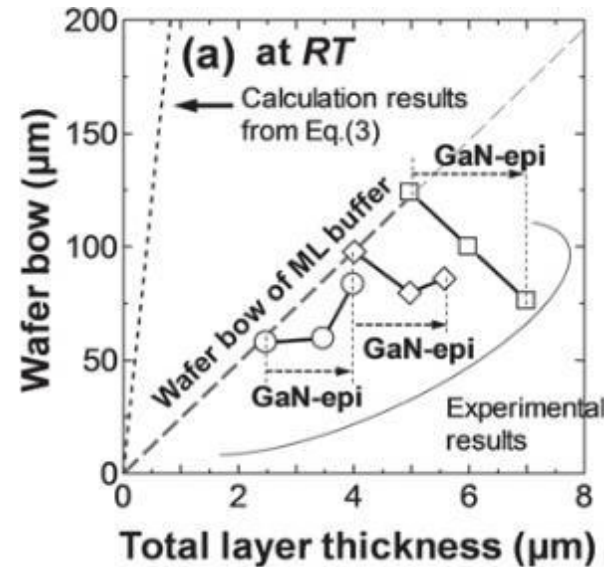
However, 1.2 kV applications currently not reachable by GaN / Si due to :

- Limitation of breakdown voltage (buffer thickness with low bow < 6 μm)
- Trapping assessment NEVER reported @ 1200 V yet

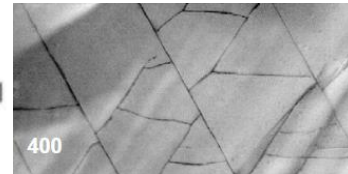
BV of GaN / Si scales with the buffer thickness but Thick buffers result in high wafer bow, high defect density and reliability issues



*N. Ikeda et al: in IEEE APEC 2010



Higher defect density
Higher strain
or even cracks



M Miyoshi et al, Semicond. Sci. Technol. 31 (2016) 105016

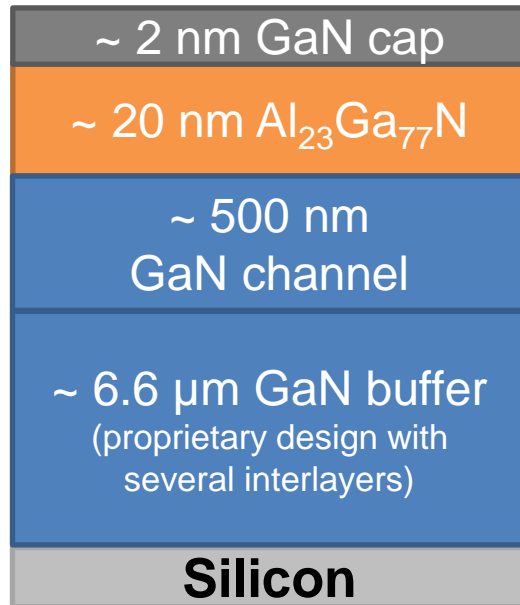
Targeting both higher vertical breakdown than available technologies WITH low trapping effects

A first example of a path for higher voltage GaN/Si operation **with the development of thicker and carbon-free buffer layers**

Epiwafer structure and properties

➤ Carbon-free (which is known to induce trapping effects)

Epiwafer structure

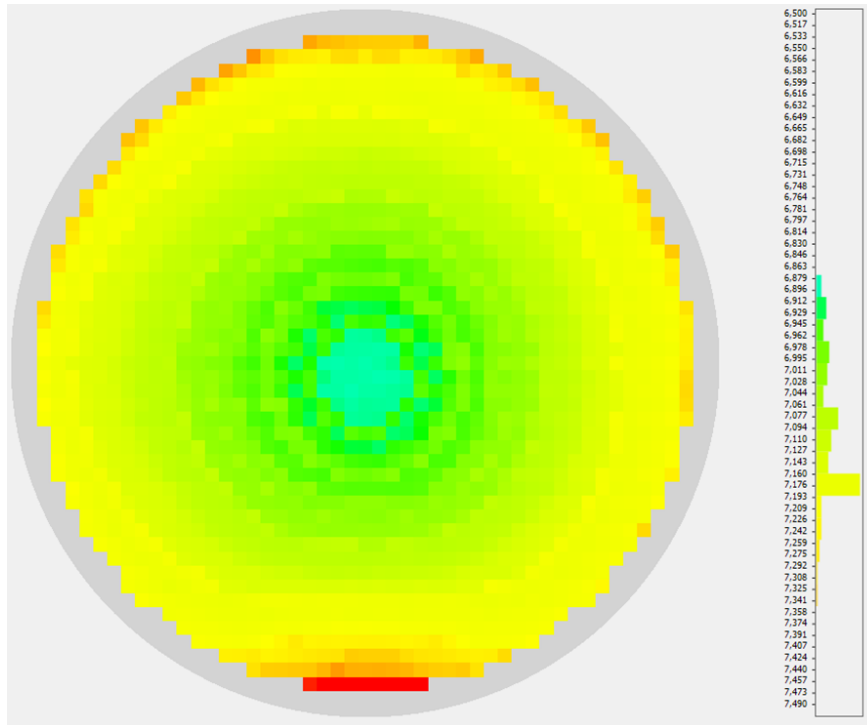


Parameters	Values
XRD (002)	395 arcsec
XRD (102)	423 arcsec
Thickness	7.1 μm
Thickness STDEV	1.55 %
Bow	-23 μm (concave)
Residual impurities in GaN measured by SIMS	C: 4~5 x10 ¹⁶ cm ⁻³ H: 2 x10 ¹⁷ cm ⁻³ O: 1~2 x10 ¹⁶ cm ⁻³
Mobility	2000 cm ² /Vs
Sheet resistance	340 Ohm/sq.
Sheet resistance STDEV	1.5 %

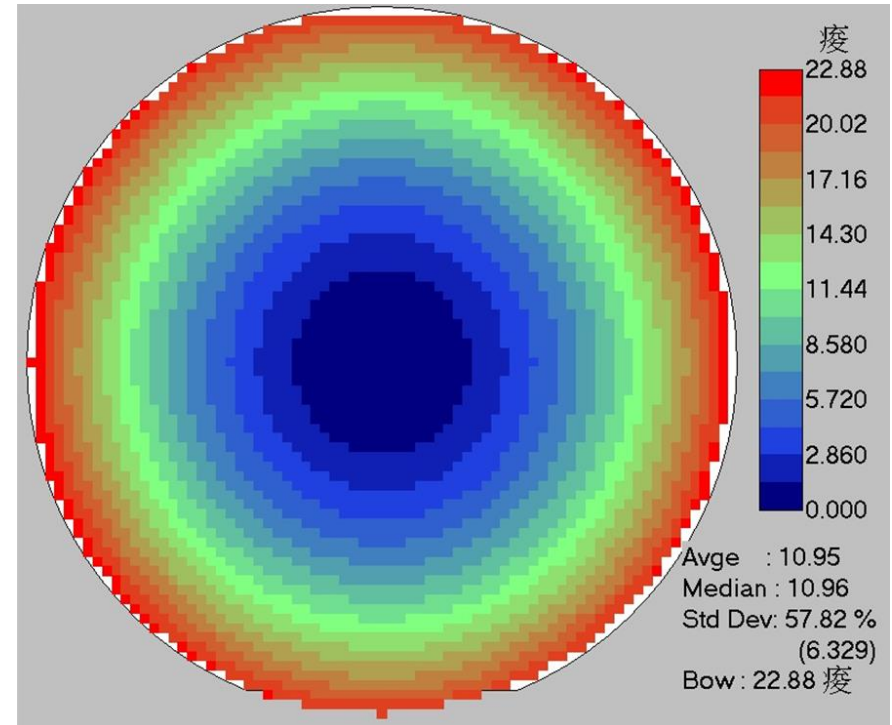


PL mapping and bow data for epiwafer

- Despite the very thick buffer, high thickness uniformity and low bow are observed: efficient strain management



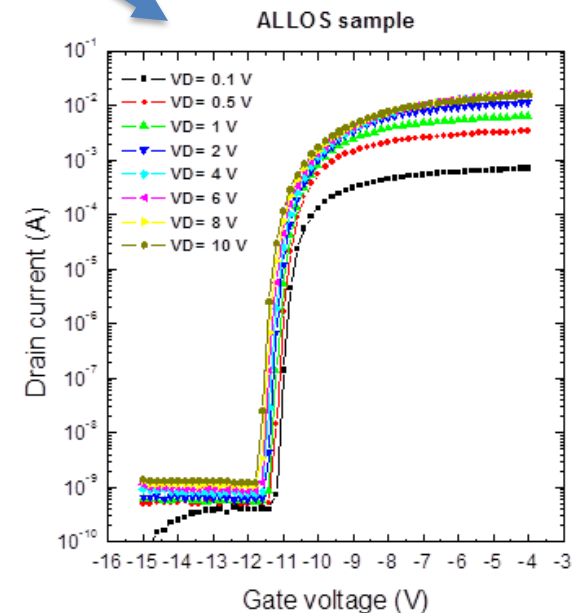
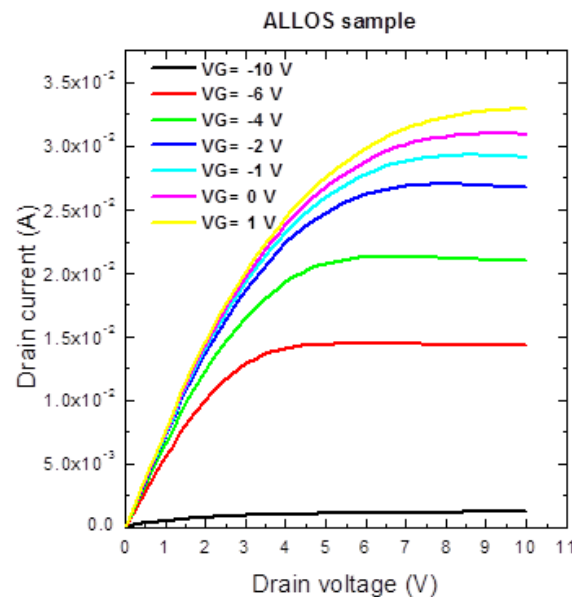
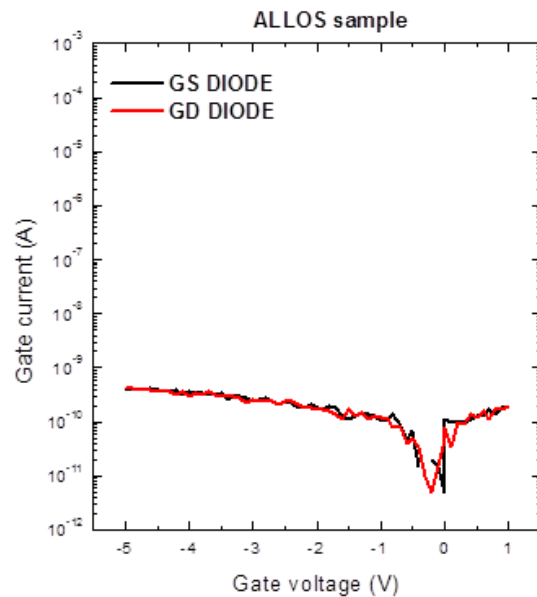
Average thickness: 7.1 μm
STDEV: 1.55%



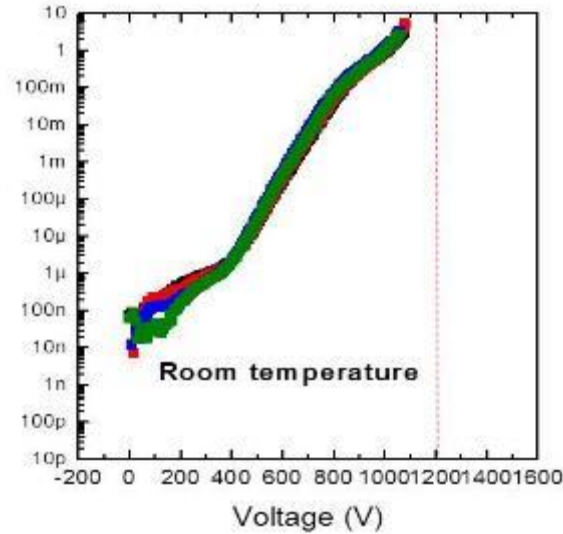
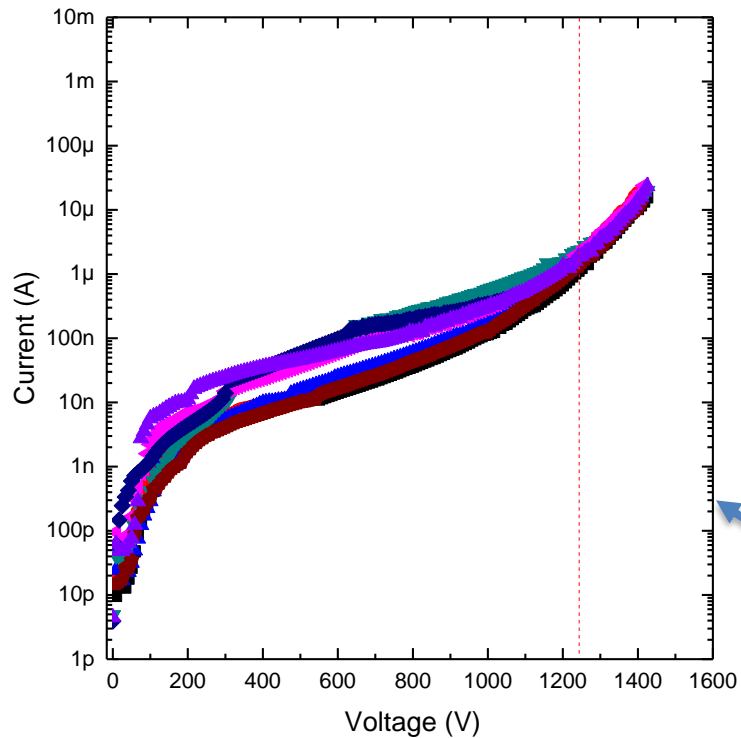
Bow: -23 μm

DC characterization of transistors

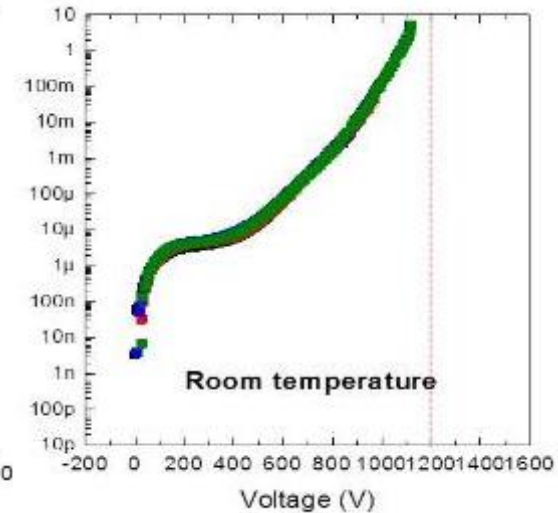
- Low gate leakage current (MIS gate configuration)
- **No evidence of punch-through effects despite the absence of carbon reflected by a high electron confinement**



Vertical breakdown



COM 1



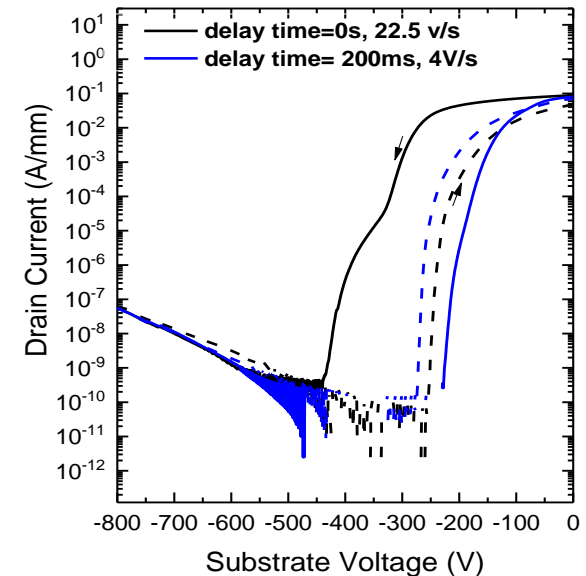
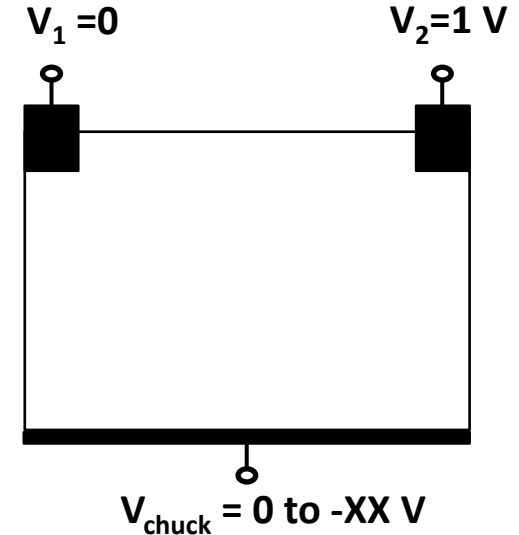
COM 2

**Vertical breakdown voltage above 1400 V,
owing to the thicker buffer
Still low leakage @ 1200 V favorably
comparable to the state-of-the-art**

Substrate ramp technique

- Simple and fast measurement giving information about the magnitude, the sign and the position relative to the 2DEG of stored charge
- By ramping the substrate to a high (negative) potential, mimicking the off-state operation under the drain contact in a transistor
- Any buffer charge trapping or storage will be visible in the substrate ramp characteristic

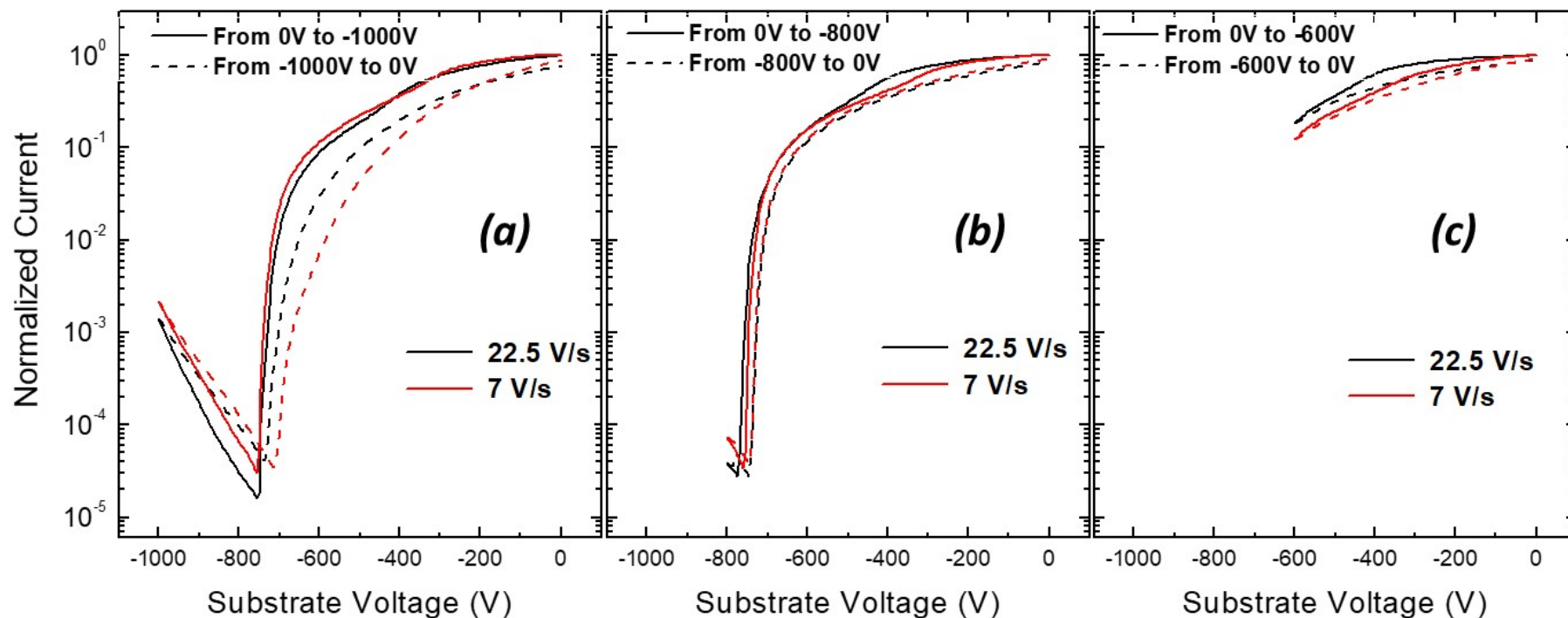
Example of sub. ramp measurements showing strong charge storage



Substrate ramp for different rates

On commercial state-of-the-art 650V-rated epi-layers ($\approx 6 \mu\text{m}$)

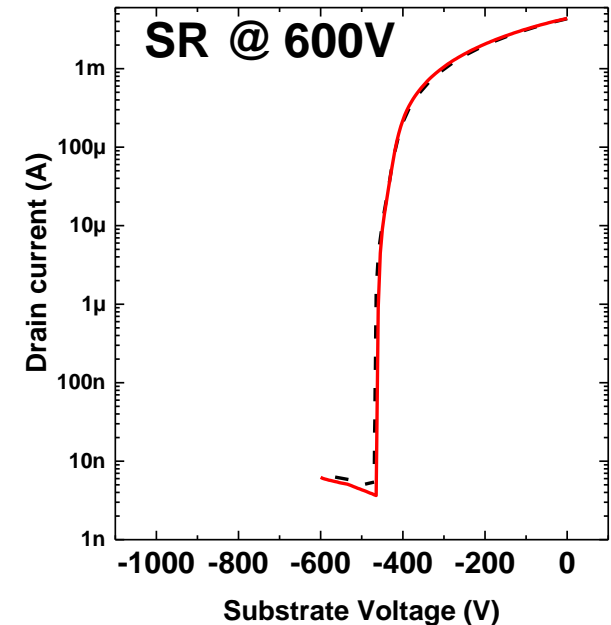
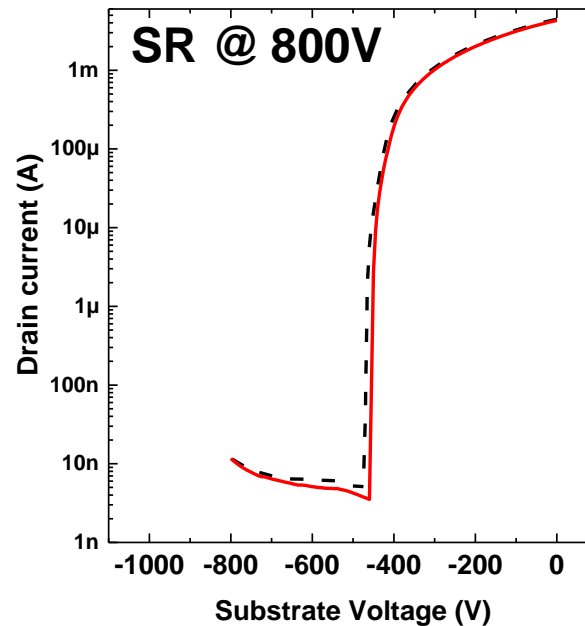
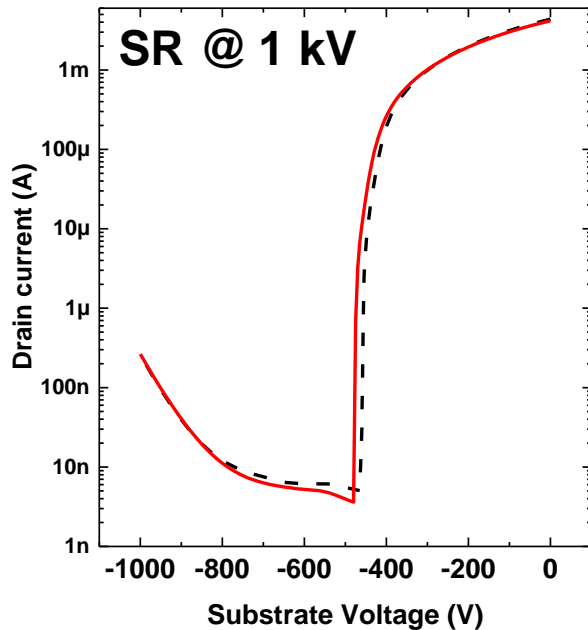
- No trapping observed up to 800 V
- Trap activation @ 1 kV
- No measurements possible beyond 1 kV (breakdown voltage limited)



Substrate Ramp measurements

On ALLOS carbon-free epi-layers : wafer 1

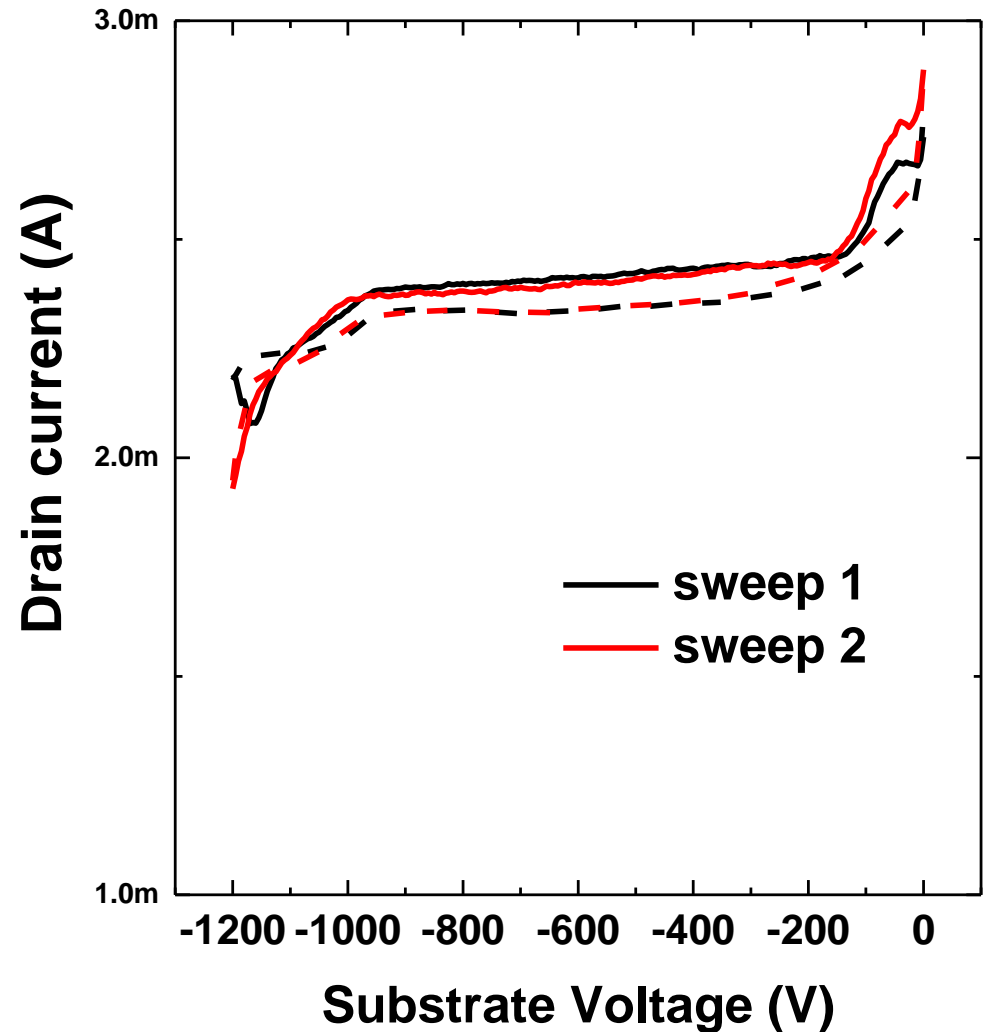
- Low trapping observed all the way to 1 kV



Substrate Ramp measurements

ALLOS carbon-free epi-layers: wafer 2

- Very low trapping observed up to 1200 V for various sweep rates
- Paves the way to GaN-on-silicon for 1200 V applications



Targeting both higher vertical breakdown than available technologies **WITH** low trapping effects

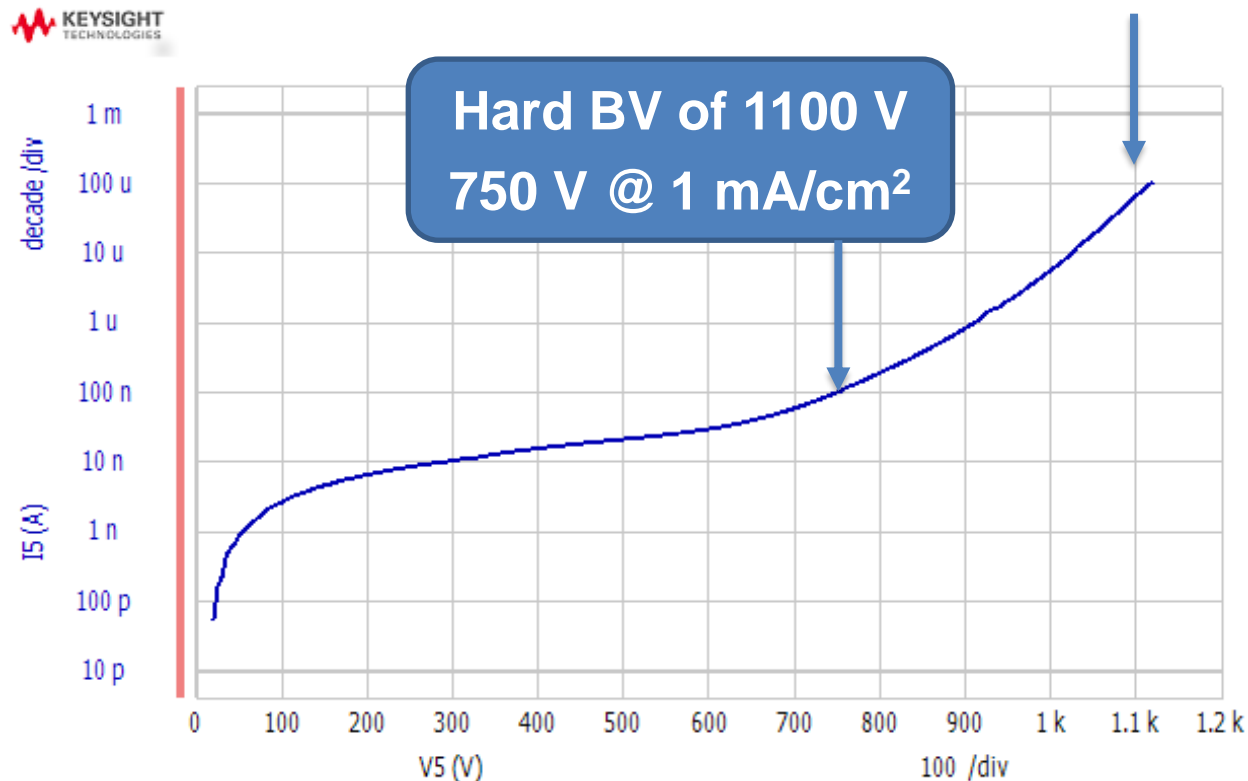
Another example of a path for higher voltage GaN/Si operation **with the implementation of SL into the buffer layers**

Vertical breakdown

Reference buffer optimized for 650 V applications :

Specific double heterostructure

Total thickness = 5.5 μm



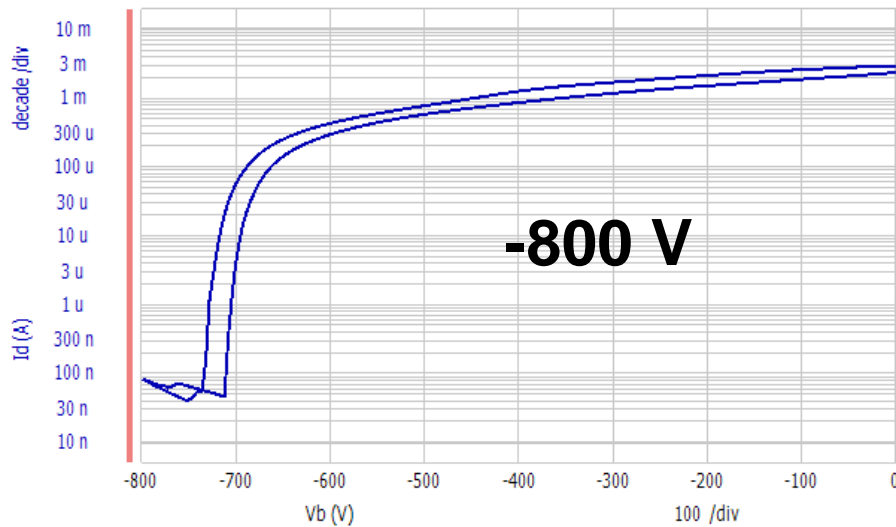
Substrate Ramp measurements

Reference buffer optimized for 650 V applications :

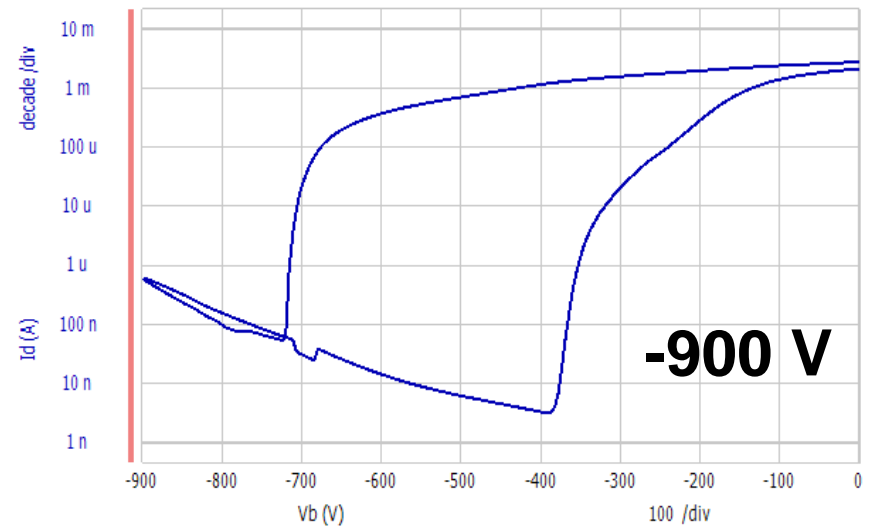
Specific double heterostructure

Total thickness = 5.5 μm

KEYSIGHT
TECHNOLOGIES



KEYSIGHT
TECHNOLOGIES



Low trapping up to 800 V



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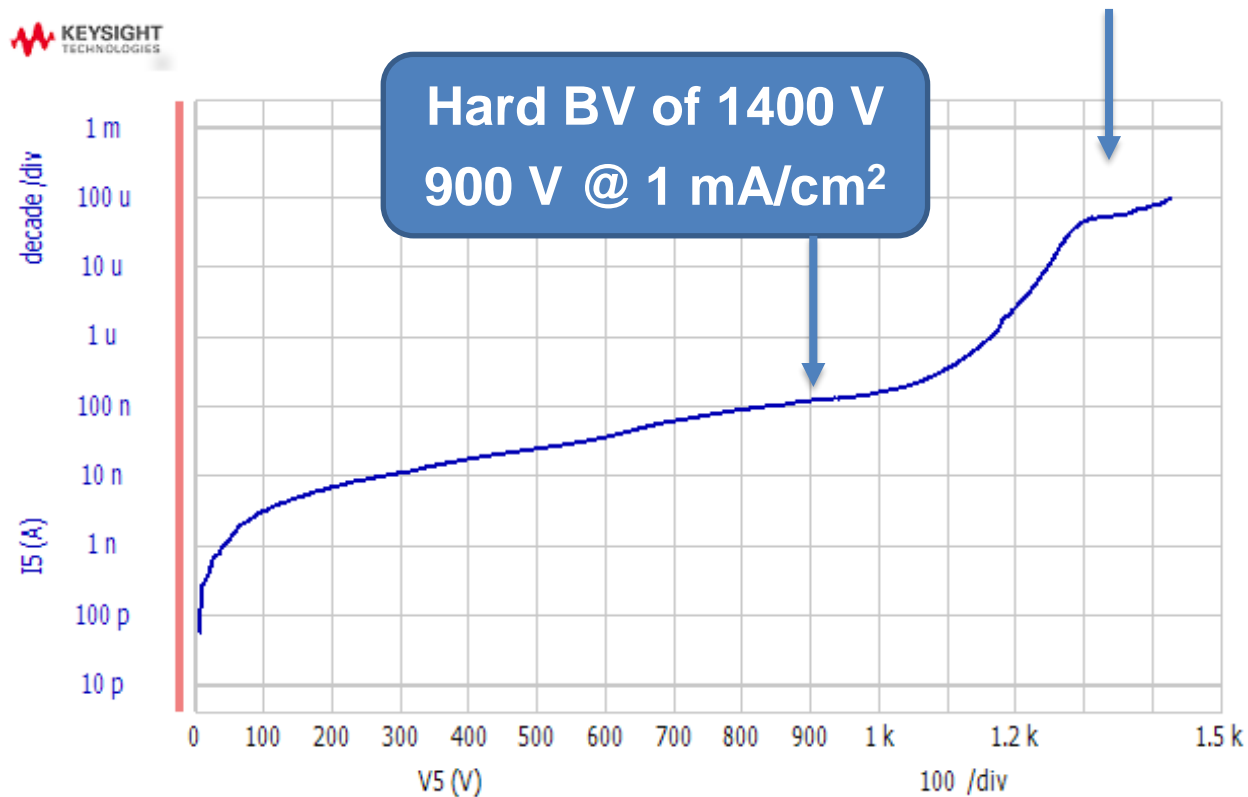
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International Conference on
Emerging Electronics

Vertical breakdown

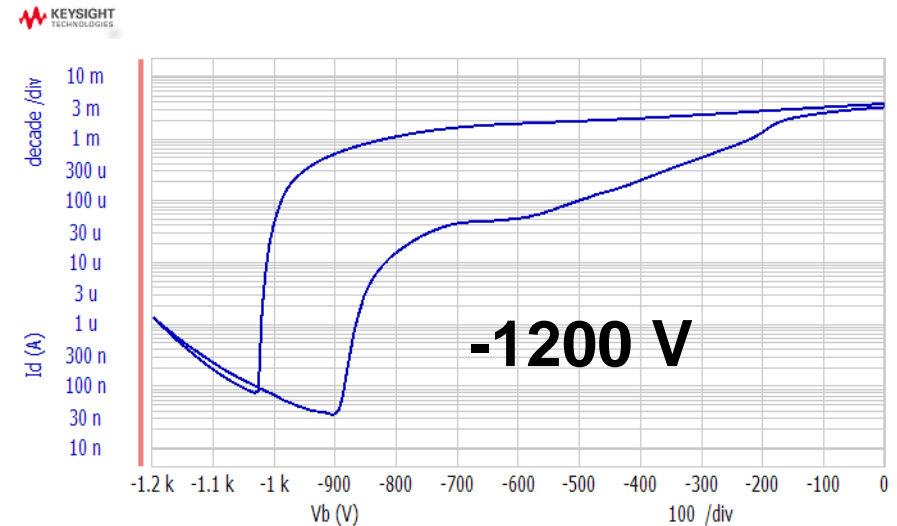
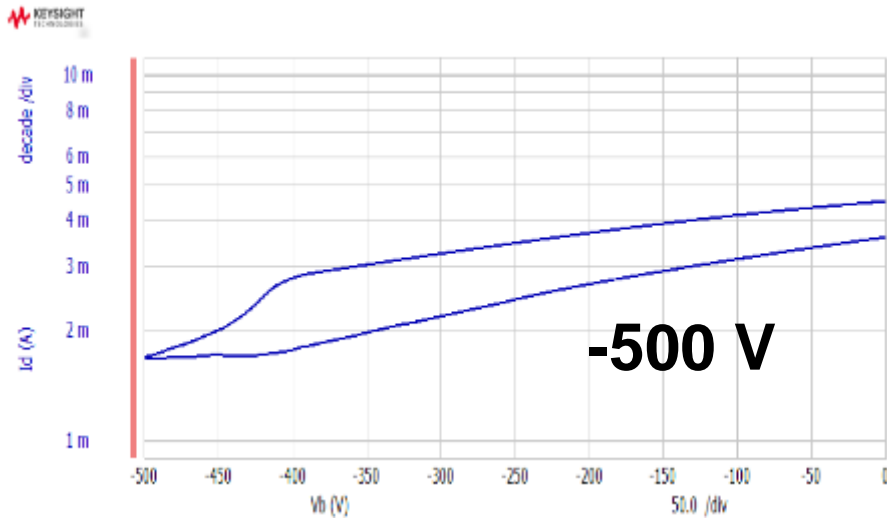
Buffer including SL for higher voltage operation :
Total thickness = 5.5 μm



Substrate Ramp measurements

Buffer including SL for higher voltage operation :

Total thickness = 5.5 μm

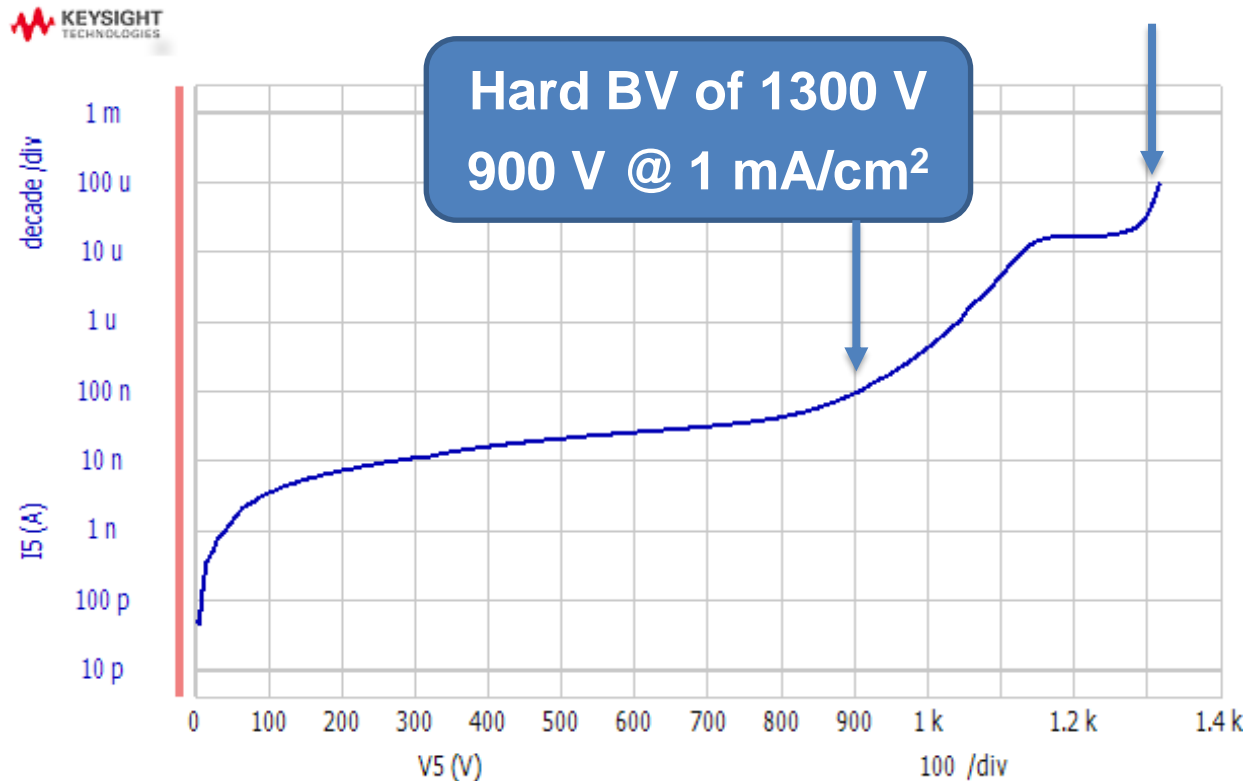


Severe trapping even @ 500 V

Vertical breakdown

Further optimized Buffer including SL for higher voltage operation :

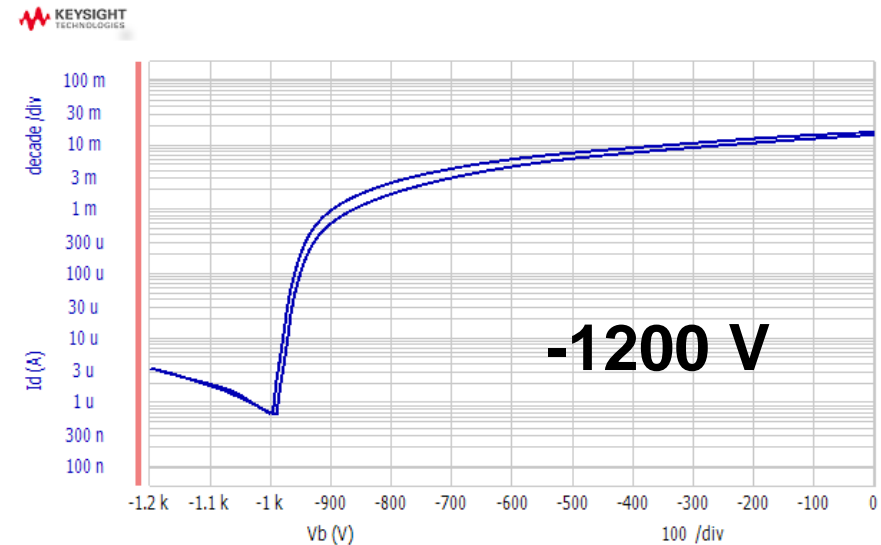
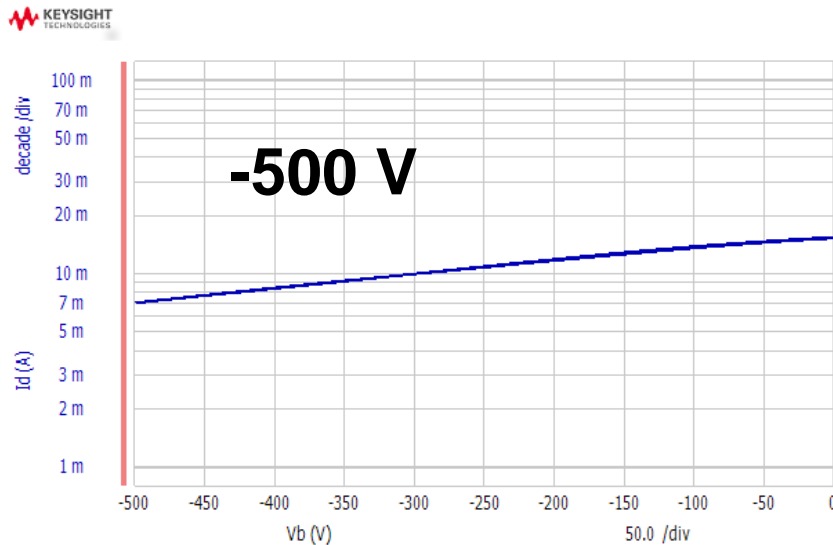
Total thickness = 5.5 μm



Substrate Ramp measurements

Further optimized Buffer including SL for higher voltage operation :

Total thickness = 5.5 μm

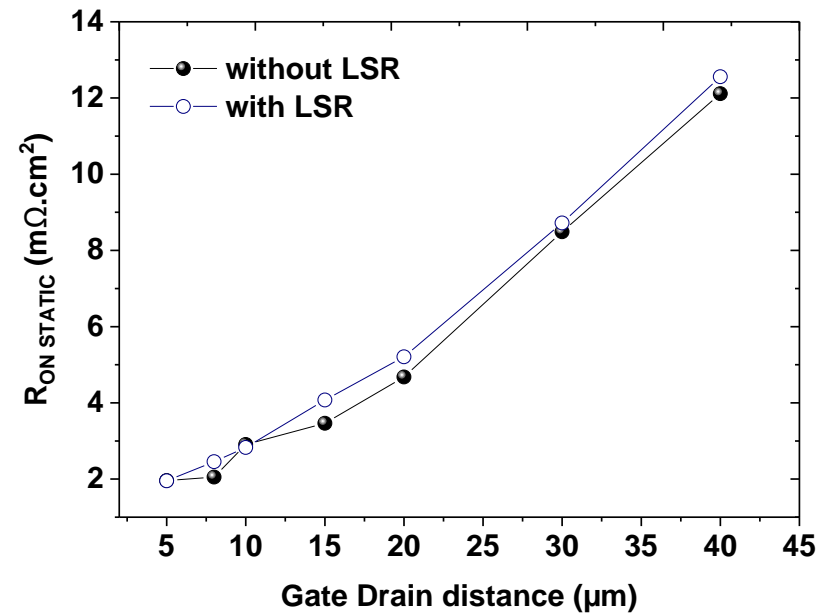
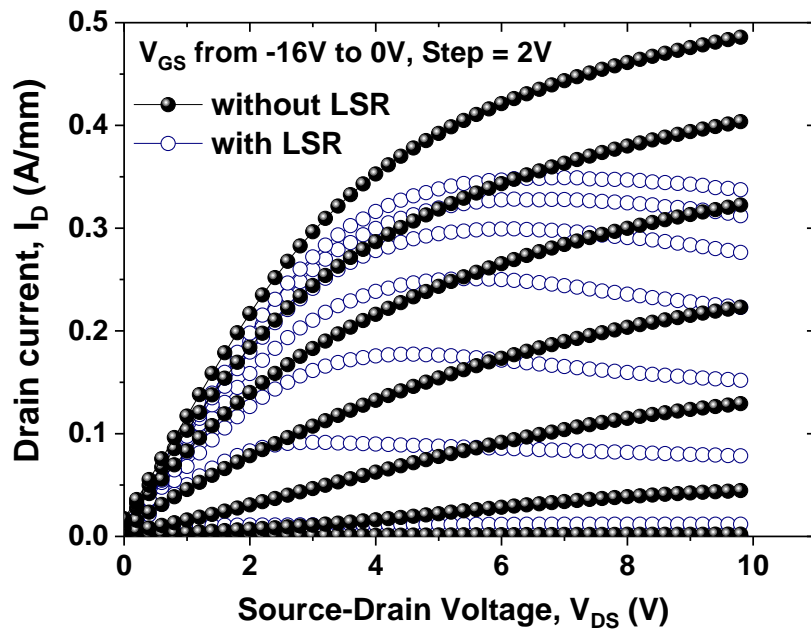
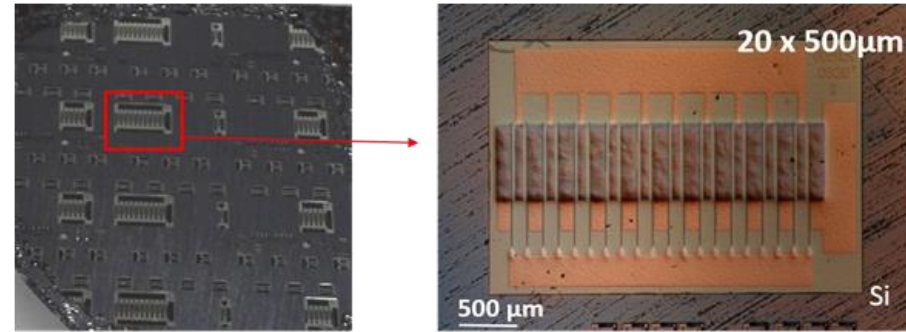
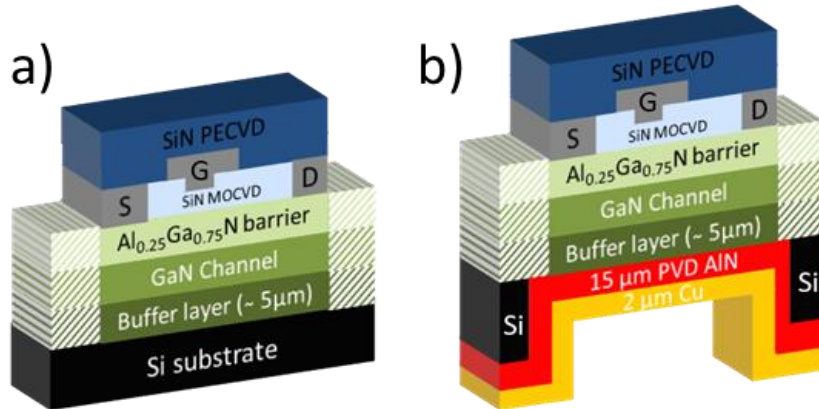


Very low trapping observed all the way to 1200 V uniformly

Targeting both higher vertical breakdown than available technologies **WITH** low trapping effects

A last example of a path for higher voltage GaN/Si operation **with the use of a local substrate removal technique and subsequent replacement with AlN ultra-wide bandgap**

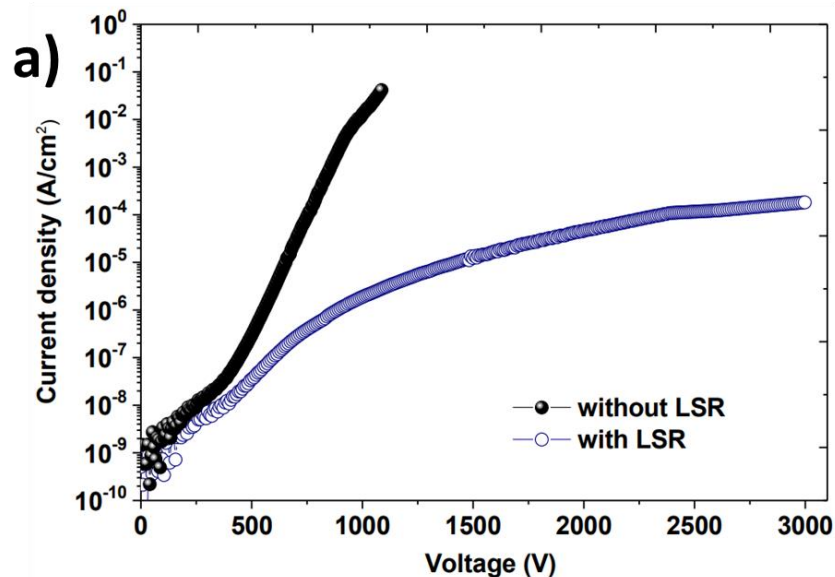
Local substrate removal technique



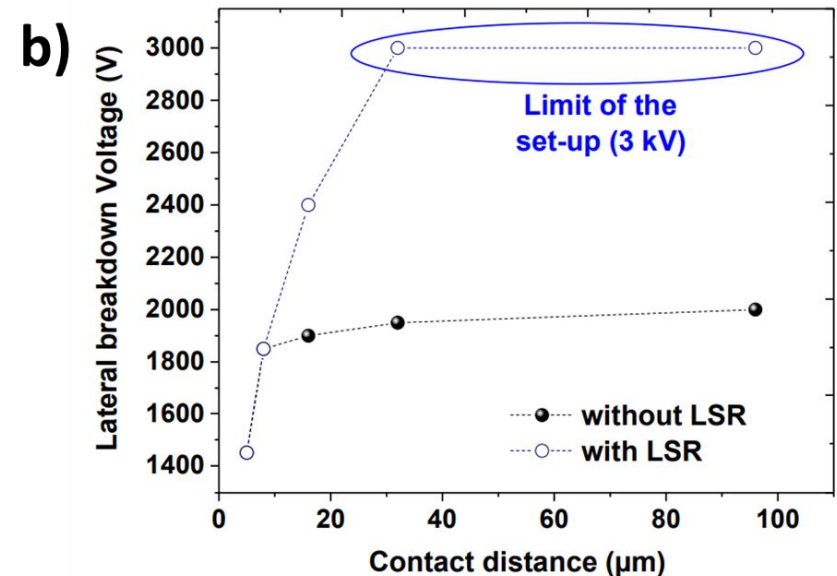
Local substrate removal technique

2-terminal breakdown voltage

vertical

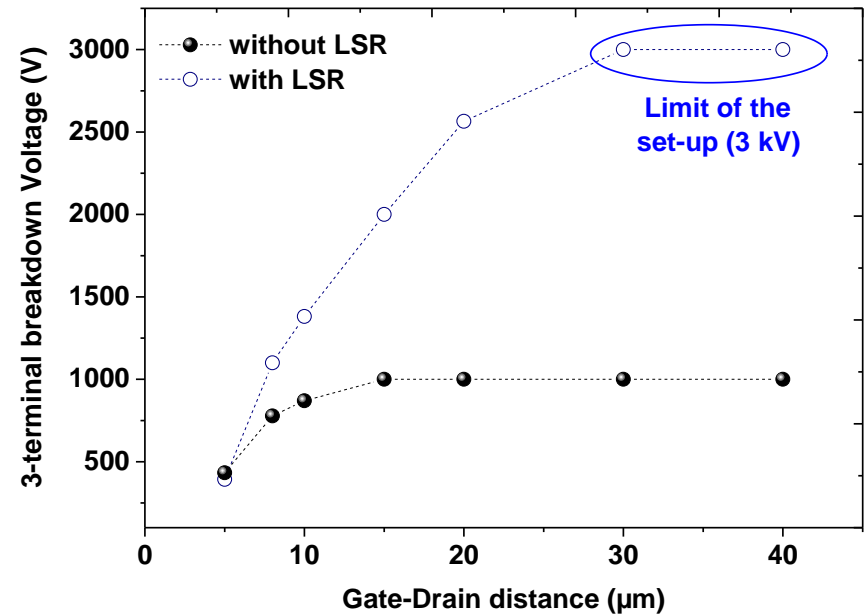
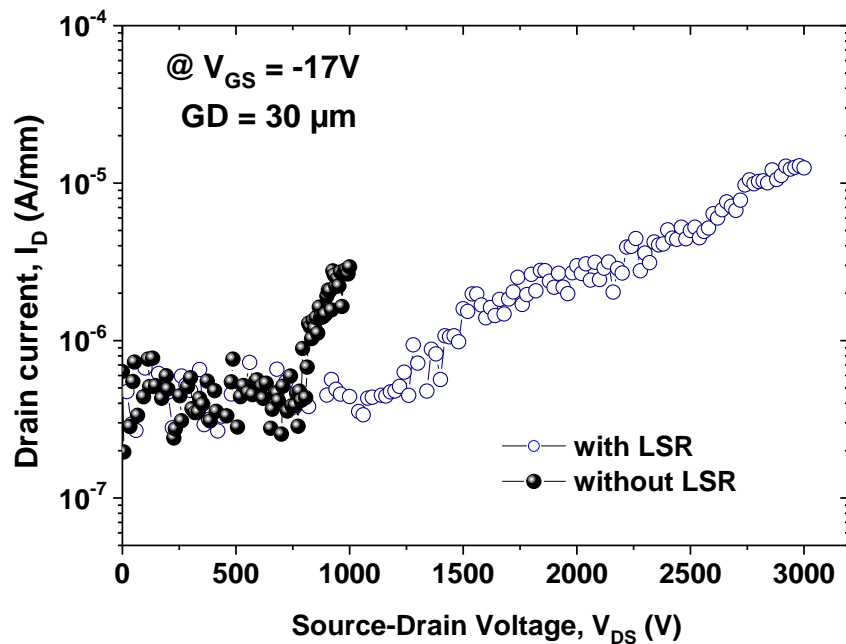


Lateral floating sub.



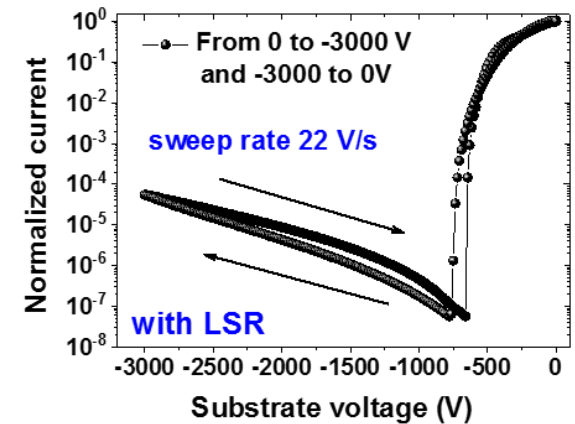
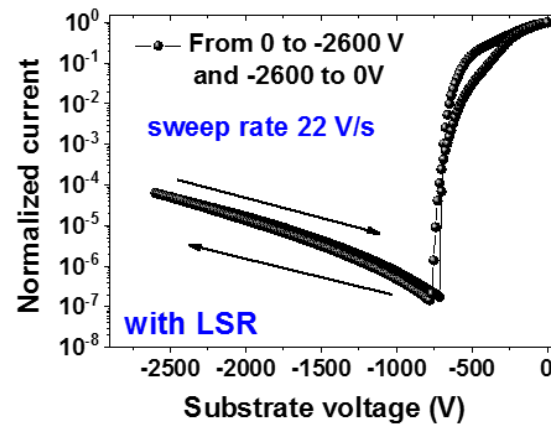
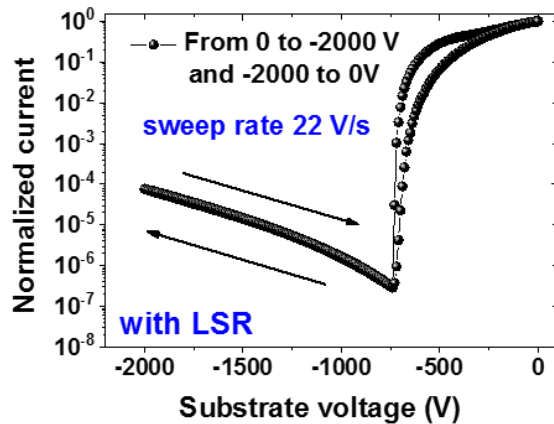
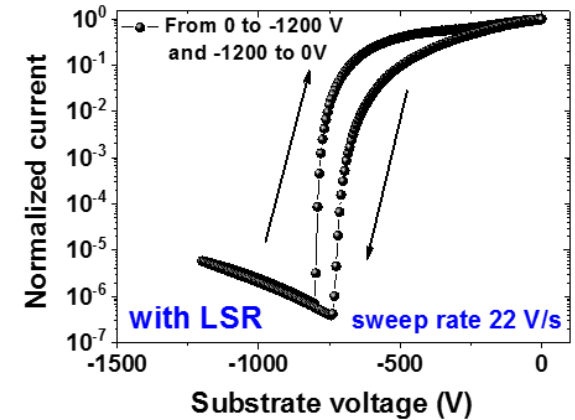
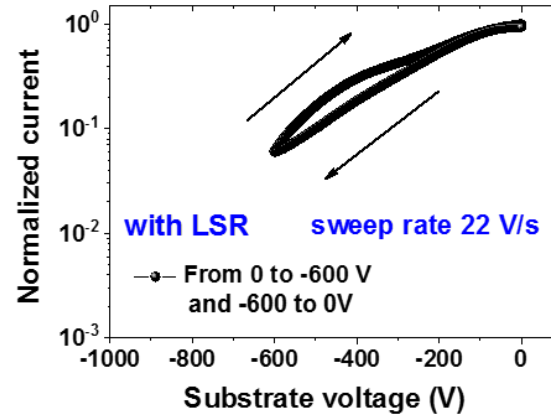
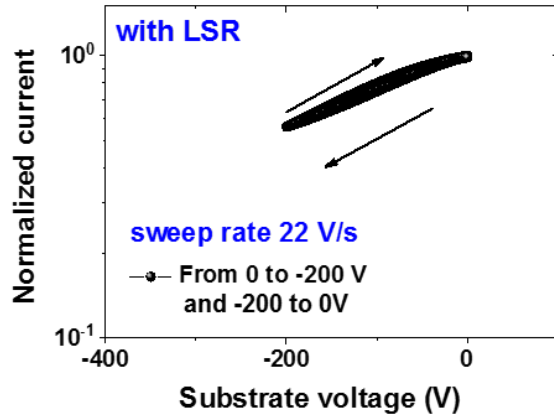
Local substrate removal technique

3-terminal breakdown voltage



Substrate Ramp measurements

Demonstration of low trapping using GaN/Si up to 3 kV for the first time



Conclusion

- C-free and thicker (7 μm) GaN buffer on Si allows low leakage current and state-of-the-art vertical breakdown voltage above 1400 V
- Optimized SL implementation enables 1200 V + BV with low trapping effects
- **LSR enabled not only to drastically enhance the BV of GaN/Si HEMTs but also does not induce any additional trapping effects**

These results show that several ways for the improvement of lateral GaN devices are already available in order to satisfy 1200 V applications