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Current status and challenges of GaN millimeter-wave transistors

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Abstract— In this work, we show that a careful architecture of buffer layers should be employed in order to perform high performance millimeter-wave GaN devices. The use of higher bias operation ($V_{DS} \geq 20$ V) will be possible while using short gate length only if the thermal resistance induced by the buffer layers is reduced. In particular, it is shown that a thick AlGaIn back barrier (DHFET structure) results in a huge drop of the PAE at $V_{DS} = 25$ V despite the pulsed mode conditions. With an enhanced thermal dissipation as compared to the DHFET, the carbon-doped structure delivers much higher performances illustrated by a state-of-the-art combination of PAE ($> 50\%$) and an output power density of 7 W/mm at 40 GHz and $V_{DS} = 25$ V.

Index Terms—GaN transistors, millimeter-wave, power, efficiency, robustness

I. INTRODUCTION

With the development of wireless communication such as 5G or SATCOM, the need and requirements for millimeter-wave compact solid-state high power amplification has significantly increased. In this frame, excellent power densities have been achieved with GaN transistors up to the W-band, confirming the potential of this material system. However, achieving high power-added-efficiency and output-power-density combination in the millimeter-wave range represents currently one of the key goal for the GaN technology despite some few initial results obtained so far. Indeed, higher PAE not only saves electrical power usage but also can reduce the size and cost of high power amplifiers (HPAs), due to the lower amount of heat dissipated. For instance, in space applications, the traveling wave tube amplifiers (TWTAs) are still widely used, because of the high PAE while delivering high P_{OUT} . Even though attractive efficiencies on GaN devices (well-beyond 40%) have been already demonstrated up to Ka band, rather limited PAE has been reported so far in the Q band (40 GHz) and above. Furthermore, the device robustness and related reliability under high electric field ($V_{DS} \geq 20$ V) have not been yet demonstrated on ultrashort GaN power devices (sub-10 nm barrier thickness and sub-150 nm gate lengths).

Actually, a number of parameters can be responsible for short GaN device degradation such as:

- The gate leakage current, especially when using Al-rich ultrathin barriers
- A poor electron confinement resulting in drain leakage current
- The so-called current collapse
- The self-heating due to a reduced thermal dissipation

In this presentation, we will discuss some potential device design enabling to overcome the above-mentioned issues and properly operate in the millimeter-wave range under high drain bias > 20 V with high performance.

II. RESULTS AND DISCUSSIONS

The key features of the proposed structures are the use of:

- an in-situ grown SiN cap layer with a critical thickness, which is used both as early passivation as well as to prevent strain relaxation,
- an ultrathin AlN barrier layer delivering high polarization while having a deep sub-10 nm thickness, favorable for high frequency operation.

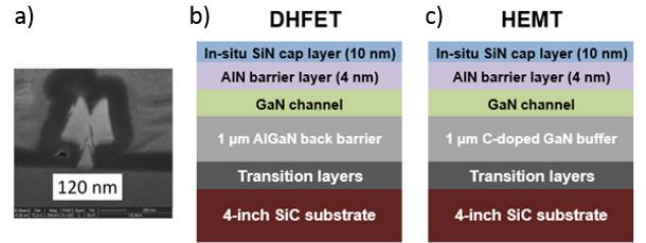


Fig. 1. a) FIB view of the 0.12 μm T-gate and schematic cross section of b) DHFET and c) C-doped HEMT.

Another key parameter is the buffer configuration that should be designed in order to maintain an excellent electron confinement under high electric field without inducing trapping effects. In this work, we compared a double heterostructure field effect transistor (DHFET) to a carbon doped GaN high electron mobility transistors (HEMTs). It is observed that the carbon doped HEMT structure shows superior electrical characteristics, with a maximum drain current density I_d of 1.5 A/mm, an extrinsic transconductance G_m of 500 mS/mm and a maximum oscillation frequency f_{max} of 242 GHz while using a gate length of 120 nm. The HEMT structure delivering high frequency performance together with an excellent electron confinement under high bias enabled to achieve a state-of-the-art combination at 40 GHz of output power density ($P_{OUT} = 7$ W/mm) and power added efficiency (PAE) above 52% up to $V_{DS} = 25$ V in pulsed mode. The performance enhancement is attributed to the better thermal dissipation within the C-doped GaN HEMTs as compared the DHFETs.