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Pushing the Limits of GaN-based Power Devices and Power Electronics

*Latest Research Results on the EU Public Funded Project
'InRel-NPower'*

The InRel-NPower research project reaches for maximum power efficiencies in power electronics' applications by exploring group III Nitride-basing power devices.

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Introduction

Power electronics demands the highest efficiency for converter and inverter applications. The continuous innovation requires the exploration of the latest GaN, AlGaN and AlN semiconductor materials. Within this context, the European Union's Horizon 2020 research and innovation programme funded the "InRel-NPower" project (Innovative Reliable Nitride based Power Devices and Applications) in order to improve functional performance and reliability of Nitride-based wide band gap power semiconductors. Generally, advances in power semiconductor technology addresses improvements in efficiency, size, weight and cost of power electronic systems. At present, IGBTs, and MOSFETs represent modern switching devices. New components based on wide band gap materials (SiC and GaN) are on the way to be introduced for next generation of advanced applications. (1)

As shown in Figures 1 and 2, wide band gap Semiconductors (WBG) such as SiC, GaN, AlN and diamond show superior material properties in comparison to Silicon.

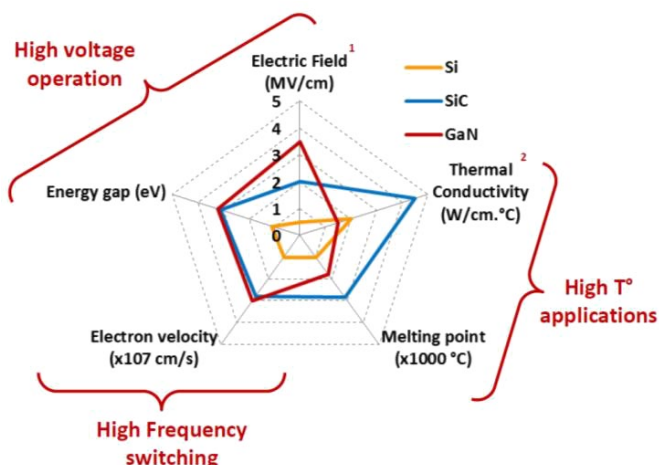


Figure 1: Superior material properties of wide band gap semiconductor material in comparison to Silicon (2).

The main strategic target of this project is to offer reliable and robust devices processed on GaN-based and AlN-based substrates (available within Europe for high and medium power application), which can help to address important and worldwide relevant social issues, like measures against climate change, sustainability in energy consump-

tion, electrical energy savings, E-mobility and so forth. Packaging is also carefully addressed in this project thanks to two innovative packaging solutions that will allow the exploitation of the full capability of the GaN material. This requires the combination of the indicated expertise over the stages of the value-chain, paired with a physical understanding of processes and mechanisms acting inside the device. The vision is that this work and the knowledge of the partners involved will help to generate a deeper understanding of the technology issues related to semiconductor devices based on wide band gap materials. The target is to bring the European semiconductor value chain partners a step further towards the frontiers of the production and application of robust high and medium power devices.

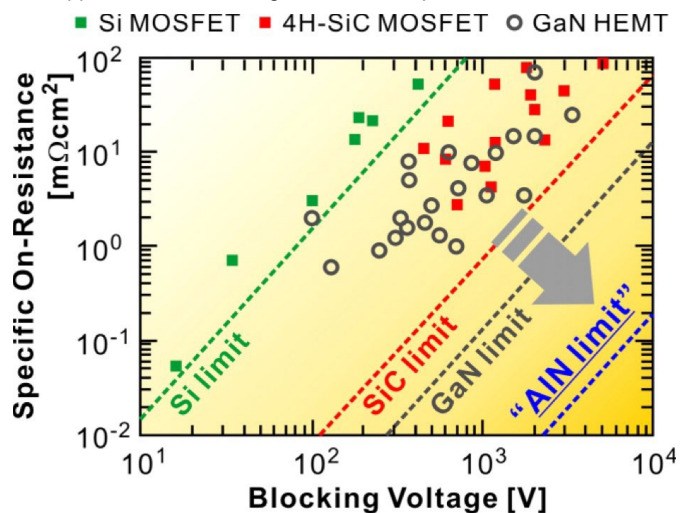


Figure 2: Superior material properties of wide band gap semiconductor material in comparison to Silicon (3), (4).

Whereas the great potential of GaN based converters has already been demonstrated at the application level there are still relatively few early adopters for this game-changing technology. The main reasons for this reluctance to switch to GaN technology is due to three factors: cost, uncertainty about long term reliability and conservatism among power converter circuit designers. InRel-NPower envisions to contribute to the medium to long term solution of the energy saving issue aspects by providing a clear reliability assessment methodology for GaN, together with convincing and improved device lifetime data, as

well as by developing two demonstrators proving the superiority (in terms of efficiency and costs) of the GaN devices developed within this project. In parallel, this project will push the boundaries of WBG technology by studying the implementation of AlN-based technology, which compared to GaN (and any other WBG semiconductor) has even better material properties.

Additionally, it shall be emphasized, that the nine InRel-NPower EU research partners are completed by two Japanese universities, the University of Mie and the University of Kyushu, as associated research members in a very special EU public funded project structure. The references (5) and (6) as examples provide an insight of their research work, tasks, contributions and results.

Improving group III-Nitride semiconductor compound material

The activities on the improvement of the GaN epitaxy and material can be roughly split in two parts: improving the HEMT heterostructure that will define the properties of the active device on the one hand and the use of different starting substrate materials together with buffer techniques on the other hand.

Due to its physical properties the GaN is probably one of the materials with the potential to develop major importance beside Silicon. However, the maturity of the fabrication processes for the most prominent novel GaN based devices, the high electron mobility transistors (HEMT), has still to improve. The HEMT structures are usually fabricated on silicon wafers with all the physical feedback and consequences a hetero epitaxial system creates. The native freestanding GaN wafers are only negligible available in small diameters and at high costs. So, the heteroepitaxy on silicon, which is available in large diameters and for low price, is the way of choice.

This is physically the more difficult situation but, epitaxy scientists all over the world have developed techniques in metal organic vapour phase epitaxy (MOVPE) for mastering the major problems arising from thermal and structural mismatch of the two materials. Although difficult, at the point in time the growth of GaN based device structures on silicon works quite successful.

The MOVPE deposition works at relatively high temperatures above 1000°C, consequently the GaN as the material with a larger coefficient of thermal expansion, shrinks faster than the Si substrate upon cooling down the system to room temperature after growth. As a result, the epitaxial layers experience huge strain and may crack. Additionally, the wafer develops an unfortunate large bow, which is not acceptable for later processing. The advanced epitaxial techniques now allow to introduce complex sequences of strain moderating layers which generate opposite strain states and thereby mitigate the bowing of the wafer.

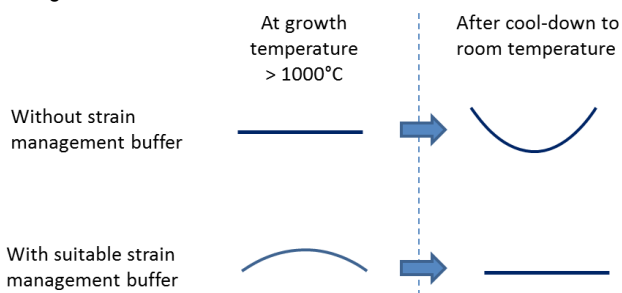


Figure 3: Mastering the wafer bow in GaN on Si heteroepitaxy.

On the other hand, the silicon substrate and the many hetero-interfaces introduced a large number of misfit dislocations because of the

required strain balancing do not match structure wise. Typically, the dislocations can be drastically reduced over the height of the semiconductor layer stack. However, a remaining dislocation density in the order of 10⁹ cm⁻² in the topmost layers remains. It is the electrical behavior of these extended defects (and other point defects), which causes difficulties for the functionality of the devices, reliability and robustness.

Improving the reliability of GaN HEMTs and designing new device architectures

Reliability assessment of e-GaN devices plays a crucial role in determining long-term stability and functionality. Initial part of such assessment involves the understanding of the conduction mechanisms under both forward and reverse bias conditions for different ambient temperatures as different gate processing techniques arises different leakage conduction mechanisms, such as Poole-Frenkel, thermally assisted tunneling (TAT). As can be seen from Figure 4, Poole-Frenkel is the main conduction mechanism under reverse bias and under forward bias there are two different conduction models. Between 1.5 V and < 4 V, conduction is basically thermionic emission (TE) based and for V_G > 4V up to breakdown it is TAT. Time-dependent dielectric breakdown measurements were done on Gate-Source diodes on p-GaN-gate based e-GaN devices. Lifetime calculations, shown in Figure 5, indicate a 10 years gate life for V_G > 6.5 V at room temperature using TAT model.

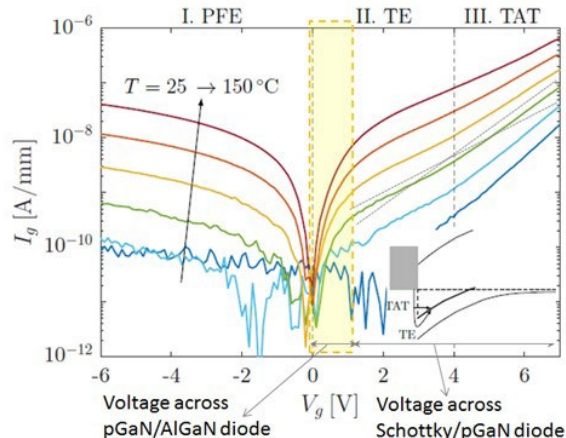


Figure 4: Figure showing the forward and reverse gate leakage characteristics for a typical pGaN gate structure as a function of temperature. Different conduction regimes are indicated.

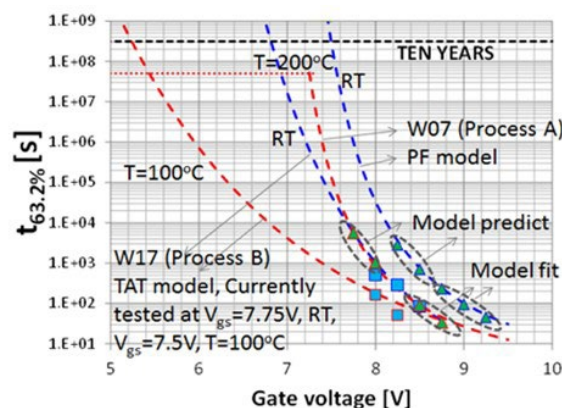


Figure 5: Operating lifetime prediction under forward bias condition at RT and 200°C based on thermally assisted tunneling and Poole-Frenkel model. Measured data (blue squares) are in line with the predicted lifetime models.

GaN-on-Si transistors suffer from poor critical electrical field strength of the Si substrate together with a parasitic conduction at the buffer/substrate interface leading to device breakdown. That is why, the highest reported three-terminal breakdown voltage values for grounded-substrate GaN-on-Si HEMTs defined at an off-state leakage current of 1 $\mu\text{A}/\text{mm}$ are still below 1.5 kV, which is basically limited by the Si substrate and associated material quality. In order to suppress the parasitic conduction phenomenon, local Si substrate removal (LSR) was proposed in 2010. The Si substrate removal around the drain electrode enabled electrical isolation of the gate and source from the drain across the buffer layer/Si interface, leading to an enhanced blocking voltage of GaN-on-Si HEMT above 2 kV. Using this method, we recently achieved for the first time GaN-on-Si MISHEMTs with LSR under the entire device followed by a backside deposition of the ultra-wide bandgap AlN material (see Figures 6 and 7). The use of an in-situ SiN gate dielectric combined with the LSR technique together with 15 μm thick AlN layer enabled state-of-the-art GaN based HEMTs with remarkably low off-state leakage current ($<1 \mu\text{A}/\text{mm}$) up to 3 kV (see Figure 8). The next step is to apply this process to industrial high current ($> 10 \text{ A}$) power devices in order to demonstrate the manufacturability of this approach.

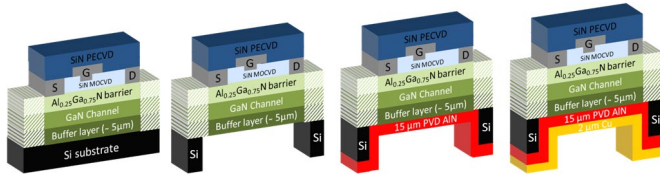


Figure 6: Schematic cross-section of AlGaIn/GaN MISHEMT after the front side process, the LSR technique, 15 μm thick PVD AlN deposition, and the 2 μm Cu deposition on the back-side.

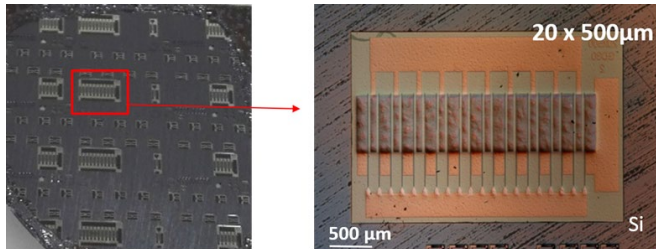


Figure 7: Optical backside image of the wafer with and without LSR removal patterns, and a 20x500 μm GaN-based MISHEMT after LSR.

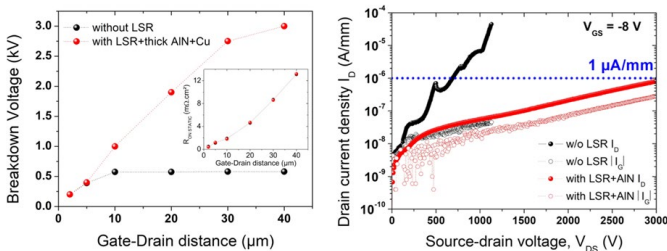


Figure 8: Evolution of LGD-dependent device breakdown and specific on-resistance (inset) of AlGaIn/GaN HEMTs with and without LSR/thick AlN/Cu by defining the blocking voltage at 1 $\mu\text{A}/\text{mm}$, and off-state leakage current characteristics of AlGaIn/GaN MISHEMTs with and without LSR / thick AlN deposition.

Modern low-inductive power module design for GaN-HEMT

For the module designs, the selected assembly and inter-connection technologies (AIT) have to support maximal the outperformance of the wide-band-gap power semiconductors in use. For instance, this refers to maximum operating junction temperatures, maximal reachable power cycle robustness and enabling a low-inductance module

characteristic. Therefore two promising module concepts with their accompanying design elements, one all ceramics substrate design and one hybrid ceramics-laminate design, are under deeper research investigation.

Due to the needed cooling performance and hot spot management, the common base substrate in both concepts will be a Si3N4-AMB (Active Metal Brazing) substrate. In addition, due to the needed power cycle robustness in hard switching inverter applications, the GaN-chip backside will be attached on this AMB-substrate in both concepts by the Silver sintering technology (or sometimes called as Low Temperature Joining Technology LTJT).

Furthermore, one has to notice: all three chip terminals – Source, Gate and Drain – have to be contacted on the chip top side due to its lateral nature as a HEMT (High Electron Mobility Transistor) device. The selected ‘counter substrate’ and its design has to enable the needed circuitry dissolution for a proper functionality.

All Ceramics Substrates Design

For this concept, the dissolution of the circuitry facing the top side of the GaN-chip will be realized with a multilayer LTCC (Low Temperature Co-fired Ceramics) counter substrate (see Figure 9). One very important task is the development of a double-sided Ag-sintering process for the new GaN devices: with the die-attach (as the Si-wafer backside) sintered on the AMB and the chip-terminals sintered to the LTCC. First trials towards this, while applying the Ag-sinter process on LTCC metallization, succeeded. (7)

A second important task is the design of the half-bridge. In power mechatronics for power modules in drive inverter applications the transition from topology and schematics into a concrete power module design in terms sub-components’ and materials’ selection, AIT processes and their order of implementation in the manufacturing line is one of the biggest challenge. A first rough sketch about this transition for the all ceramics module concepts gives Figure 9.

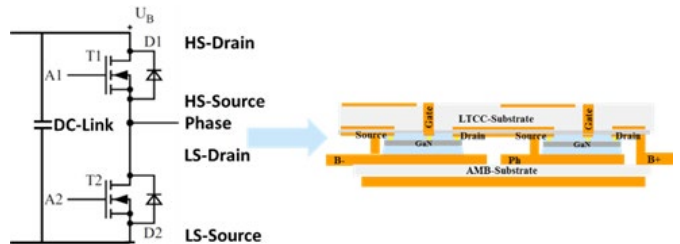


Figure 9: Rough sketch about the transition from half-bridge topology to power module design.

Ceramics-Laminate Hybrid Design

Towards the hybrid ceramic-polymer concept a compact interconnection technology replacing conventional wire bonding is being developed. For this purpose flexible planar metal interconnects on insulating layers are employed, providing the required low inductance and improved thermal management.

The packaging approach comprises

- low inductance interconnects with flexible planar interconnection and
- higher frequency drive operation
- and compact packaging with higher reliability, robustness and reduction of system size and
- includes embedded active and passive components, sensors, gate drive unit and cooling.

Figure 10 shows a draft of an integrated system applying the innovative planar packaging technology. The ceramic substrate with planar interconnect technology is embedded into a PCB with integrated passives, gate drive unit and heatsink

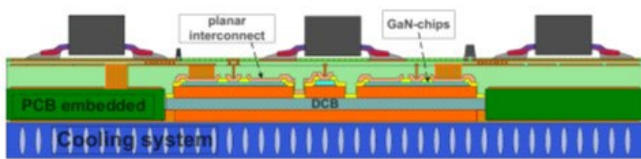


Figure 10: Compact system with planar packaging technology and improved thermal management (3D packaging).

Due to researchers' resources efficiency reasons the base substrate design strategy has been defined as to use the same AMB base substrate design and layout in both power module low-inductive concepts described above. Hence, the first step was to define which functional inputs and outputs are needed in principal for the later design flexible AMB substrate layout, e.g. like battery plus/minus, phase leg, logical connections, sensing connections etc.. The result of this consideration in terms of the defined AMB layout shows Figure 11.

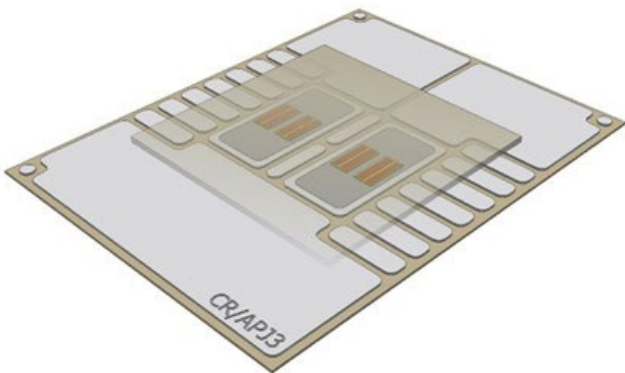


Figure 11: Defined AMB-layout: the planed position of the LTCC counter substrate is shown shaded above the chips.

The second step was to describe the thermal situation under the target characteristics of the new InRel-NPower GaN HEMT (25 mOhm RDS, on channel resistance @ 150°C maximum Tjunction) and the chosen power class of the full B6-bridge demonstrator between 20 up to 30 kW. Due to the small size of the devices, the loss density of the devices is very high. For a proper design of the distance between the devices, first simple simulations were carried out with different heat transfer coefficients. The results for a high heat transfer coefficient are shown in Fig. 12.

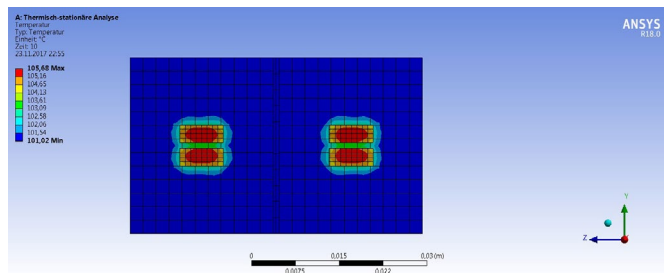


Fig. 12 Simulations of two GaN devices in parallel per switch with variation of distance on a heatsink with high cooling performance.

Summary

All power electronic systems of the future will take full advantage of the GaN-based and AI-based devices developed within this project.

These advantages include:

- Reduced heat sink requirements, lowering cooling requirements and energy saving;
- 80% reduction in system volume and weight, lowering overall system cost and material usage (due to the much smaller inductors, transformers and capacitors);
- Lower voltage drop for unipolar devices, lowering conduction losses and saving energy
- Increased output power, leading to more efficient power systems;
- Improved transient characteristics and switching speed, reducing switching losses;
- Reduced electrical noise from smaller system packages, allowing more robust circuits.

This project will focus on this lack in methodology and data, by combining the knowledge and expertise of European Centers-of-Excellence in this field and linking it to an EU-based commercial device manufacturer and substrate producers, allowing assessing large-area power devices on a large statistical sample base (rather than focusing on a few R&D samples).

Acknowledgement

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