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Recent Progresses in Deep Depletion Diamond Metal Oxide Semiconductor Field Effect Transistor

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Abstract.

Diamond has been explored to develop prototypes of Field Effect Transistors (FET). At present time, different architectures are still under investigation mostly for power electronics applications, and well suited for high temperature and high radiation environments. Recently, Diamond Deep Depletion Metal-Oxide-Semiconductor FET (D3MOSFET) concept has been introduced and demonstrated as a good candidate to design efficient diamond MOSFETs. In this paper, a general introduction of the deep depletion concept is given. Then, the key issues concerning the design and fabrication of such kind of diamond MOSFETs are described and discussed in terms of quasi static performances (on state and off state). A demonstration of working regimes of a fabricated normally-on D3MOSFET is commented, reaching at least a 5.4 MV/cm critical field at a drain-source bias of -175 V, without electric field relaxation structures. The minimum on-state resistance was measured at $R_{ON,S} = 50$ mΩ.cm^2 at 250 °C. Finally, the perspectives of the D3MOSFET is contextualized in a more global research effort to develop diamond power FETs. Some of the main challenges regarding the fabrication of competitive D3MOSFETs and more generally power diamond devices are discussed.

1. Introduction

Ultra wide bandgap semiconductors (UWBGS), like AlGaN, BN, diamond, Ga_2O_3, have been attracting a lot of attention in recent years because of their interest in many application fields [1]. UWBGS are commonly considered as the obvious next step of wide band gap semiconductors (WBGS) roadmap, like GaN or SiC, because of their

higher breakdown voltage capabilities thanks to their larger band gaps. The approach is to make the same devices but with higher performances thanks to superior properties of UWBGS. The same approach occurred for WBGS next to Si. This incremental approach is limiting the concepts to well-established devices, which are not fully exploiting the new playground proposed by UWBGS. The energy scale offered by UWBGS are opening numerous new opportunities for many original device concepts. The deep depletion diamond metal oxide field effect transistor (D3MOSFET) is based on one of this new concept [2, 3, 4].

Among these materials, diamond appears as the best candidate for power electronics because of its exceptional physical properties such as a wide band gap (5.5 eV), a high breakdown electric field (between 5 and 15 MV/cm) [5], an outstanding thermal conductivity (20 W/cm/K) [6] and high carrier mobilities (hole: 2000 cm^2/Vs [7] and electron: 1000 cm^2/Vs [8, 9, 10]). The combination of these exceptional properties makes diamond an ideal semiconductor for high power and/or high frequency electronics, which should surpass other materials like silicon, silicon carbide or gallium nitride [11]. Its capability to withstand very high breakdown fields and high current density, thus allows a miniaturization of power electronics devices able to operate in harsh and extreme environments.

Numerous diamond field effect transistors (FET) are under investigation: H-terminated accumulation FET (H-FET) [12], O-terminated inversion channel (I-FET) [13], metal-semiconductor FET (MESFET) [14] and junction FET (JFET) [15]. Considering the conduction nature of the channel, one can classify these FETs in two categories: surface channel for H-FET and I-FET or bulk channel for MESFET and JFET. The D3MOSFET transistors are based on bulk diamond properties.

Since the report of the basic concept [2] to the fabrication of first D3MOSFET [3, 4], efforts have been done in order to improve the FET performances and also to propose the best structures. The goal of this review is to deliver the recent progresses and an overview of the D3MOSFET perspectives. First, the basic background of the deep depletion concept is described. Then, the basics physics and trade off for the design of the D3MOSFET will be discussed in details including the on-state resistance temperature dependence and the trade off between on-state resistance and breakdown voltage. Finally, the fabrication and characterization of the transistor will be detailed and analysed in order to evaluate the potential capabilities of such new UWBG transistor.

2. Deep Depletion MOSFET: a concept for wide bangap semiconductor

2.1. Deep depletion regime: a steady state regime in wide bandgap semiconductor transistor

To explain the novelty of the deep depletion regime in wide band gap semiconductors, it is useful to remind the working regimes of a MOS Capacitor (MOSCap). Fig. 1 a)

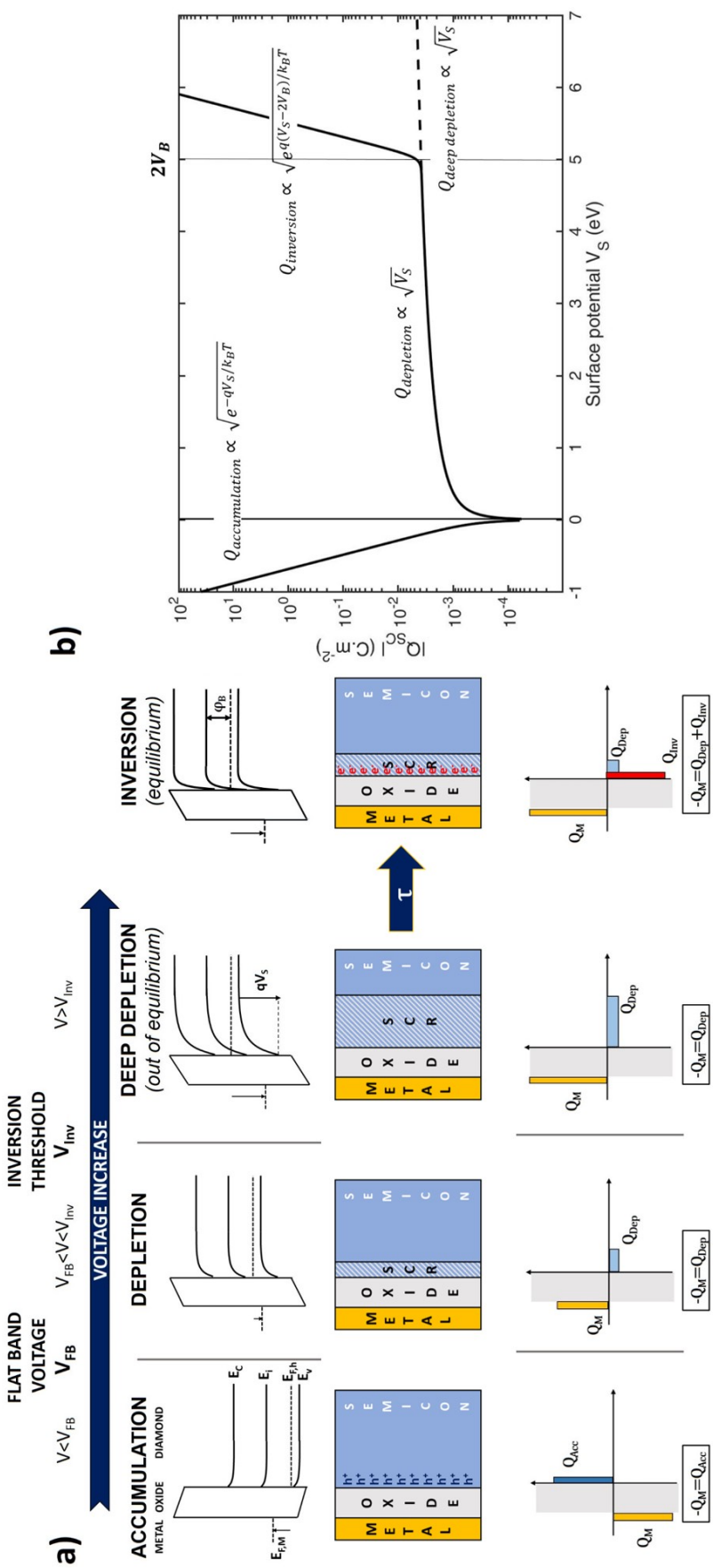

Figure 1. a) Different regimes of a p-type MOSCap with their respective schematic band diagram, cross section view and charge equilibrium equation. b) Charge as function of the surface potential in a p-type MOSCap.

illustrates the three main working regimes of a $p-$type MOSCap following the charge equilibrium equation [16]:

$$Q_{SC} = -sign(V_S)\frac{\sqrt{2}k_B T\epsilon_0\epsilon_{SC}}{qL_D}F(T, V_S, V_B) \tag{1}$$

where Q_{SC} is the charge in the semiconductor side of the MOS, $L_D = \sqrt{\frac{k_B T\epsilon_0\epsilon_{SC}}{q^2 p}}$ is the Debye length, in which p is the hole density in the neutral region under equilibrium, V_S is the surface potential and $V_B = \frac{k_B T}{2q}log(\frac{ni(T)}{p_0(T)})^2$ corresponds to the difference of energy between the Fermi level in the neutral region and the intrinsic Fermi level. $q \simeq 1.602^{-19}$ C is the elementary charge, $k_B \simeq 1.381^{-23}$ J/K is the Boltzmann constant, $\epsilon_0 = 8.85^{-12}$ F/m is the vacuum permittivity, ϵ_{SC} is the relative dielectric constant of the semiconductor (5.7 for diamond) and T the temperature. V_S is connected to the bias voltage applied on the gate metal V_G by $V_G = V_S + V_{OX}$ depending on the potential drop across the oxide V_{OX}, given by $V_{OX} = \frac{Q_{SC}}{C_{OX}}$ where C_{OX} is the oxide capacitance. $n_i(T)$ is the intrinsic bulk carrier density.

The function $F(T, V_S, V_B)$ is defined as:

$$F(T, V_S, V_B) = \sqrt{[e^{\frac{-qV_S}{k_B T}} + \frac{qV_S}{k_B T} - 1] + e^{\frac{-2V_B}{k_B T}}[e^{\frac{qV_S}{k_B T}} - \frac{qV_S}{k_B T} - 1]} \tag{2}$$

From this equation, different regimes can be delineated with their charge equation plotted in Fig. 1 b):
(i) For $V_S < 0$, the exponential part of the left term of Equ. 2 is dominant, the MOS is in forward regime (also referred as accumulation regime), majority carriers are accumulated in a 2D hole gas at diamond/oxide interface, no depletion layer occurs. The charge accumulated $Q_{accumulation}$ at the interface at semiconductor side scales as:

$$Q_{accumulation} \propto e^{\frac{-qV_S}{k_B T}} \tag{3}$$

(ii) For $V_S < 2V_B$, the MOS is in the depletion regime. An insulating depleted region, also called Space Charge Region (SCR) extends versus bias voltage from the semiconductor interface to bulk. The depletion charge $Q_{depletion}$ versus surface potential exhibits a square root dependence:

$$Q_{depletion} \propto \sqrt{V_S} \tag{4}$$

(iii) For $V_S > 2V_B$, the MOS reaches the inversion regime under equilibrium. This regime appears for gate voltage above the threshold V_{Inv} defined by the condition $V_S = 2V_B$. To reach the thermal equilibrium, electrons carriers are thermally generated from the valence band to the conduction band since at the oxide/semiconductor interface the Fermi level is closer to the conduction band. It results in the creation of a 2D electron gas. The inversion charge $Q_{inversion}$ is proportional to the exponential part of the right term of Equ. 2:

$$Q_{inversion} \propto e^{\frac{q(V_S - 2V_B)}{k_B T}} \tag{5}$$

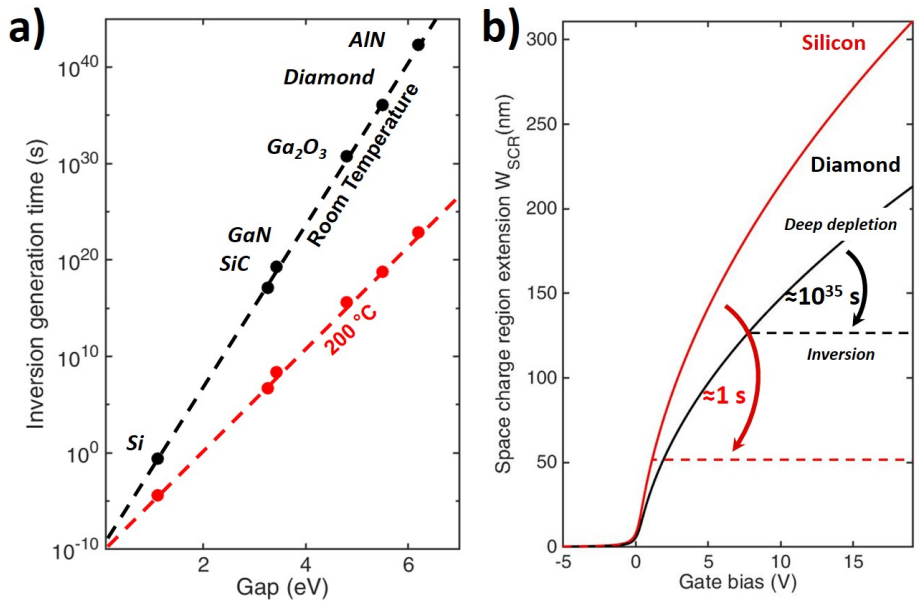

Figure 2. a) Approximated inversion generation time as function of band gap using Equ. 6 for Si (1.11 eV), 4H-SiC (3.26 eV), GaN (3.43 eV), Ga_2O_3 (4.8 eV), diamond (5.5 eV) and AlN (6.2 eV). The dashed lines are only a guideline to show the exponential trend. b) Comparison between the SCR extension in a silicon and a diamond MOS for a doping level of 2×10^{17} cm^{-3} and an oxide (Al_2O_3) thickness of 50 nm, the typical values used in devices of this work. The threshold voltage V_{Inv} and W_{Inv} values are respectively 1.1 V and 52 nm in the Si MOS and 7.7 V and 126 nm in the diamond MOS.

In this regime, any change of the charge δQ_{SC} will result mostly in a change of the inversion layer charge, due to its exponential dependence, so that $\delta Q_{depletion} << \delta Q_{inversion}$. As a result the SCR thickness W_{SCR}, defined by $W_{SCR} = \frac{Q_{depletion}}{qN_A}$ in case of homogeneous doping level N_A, appears to be pinned for $V_G > V_{Inv}$ at a value W_{Inv}, limiting the channel thickness that can be used for the depletion MOSFET.

The inversion regime at equilibrium establishes versus time with a characteristic time constant τ_{Inv}. Minority carriers have to be generated from valence band to conduction band. Here, we considered the fastest case of trap assisted thermal generation by a midgap state:

$$\tau_{Inv} = \frac{2}{v_{th}\sigma N_V} e^{\frac{E_C - E_V}{2k_B T}} \tag{6}$$

where v_{th} is the mean thermal velocity of carriers $v_{th} = \sqrt{\frac{3k_B T}{m_h^*}} = 1.2 \times 10^7$ cm/s at room temperature using the diamond effective hole mass $m_h^* = 0.908 m_0$ [17], σ is the capture cross section of the midgap state typically in the order of 10^{-16} cm^2 and N_V is the equivalent density of states, evaluated at $N_V = 2(2\pi m_h^* k_B)^{3/2}/h^3 = 2.18 \times 10^{19}$ eV^{-1}.cm^{-3} at room temperature.

Fig 2 a) shows the lower limit values of τ_{Inv} for Si, SiC, GaN, Ga_2O_3, Diamond and

AlN at room temperature and 200 °C. The inversion charge generation time constant, which is of the order of the s in case of Si, is larger than 10^5 s in case of WBGS and UWBGS. Even at high temperature, inversion regime cannot be observed without any external source of minority carriers (like source drain in inversion MOSFET or subbandgap light excitation). This specific properties operates in D3MOSFET. The extension of depletion regime for bias voltage larger than the inversion threshold, generally called deep depletion, is a steady state in WBGS and UWBGS. This specific property allows to design deep depletion MOSFET having thicker channel than in traditional depletion MOSFET, and thus less resistive, without disturbance of minority carrier generation during the commutation of the device. Fig 2 b) shows the space charge extension as function of the gate bias for a doping level of 2×10^{17} cm^{-3} and an oxide (Al_2O_3) thickness of 50 nm of Si and diamond. Silicon is limited to 50 nm by the apparition of inversion regime while diamond is only limited by the maximum gate bias the oxide can sustain or required by the application.

Equ. 1 and equ. 2 can be rewritten:

$$Q_{SC} = \sqrt{2\epsilon_0\epsilon_{SC}p_0(T)}\sqrt{[e^{\frac{-qV_S}{k_BT}} + \frac{qV_S}{k_BT} - 1]} \tag{7}$$

Thanks to this concept, we proposed to fabricate diamond deep depletion transistor.

2.2. Diamond deep depletion MOSFET working principle

The working principle of the D3MOSFET is detailed in [2]. It can be summarized by the schematic cross section depicted in fig. 3. The lateral conduction between the drain and source ohmic contacts in on-state (fig. 3 a)) is made through the bulk of a $p-$type (boron doped) diamond layer grown on a 1b diamond semi-insulating substrate. For the time being, the bulk mobility of carriers (1000-2000 cm^2/(V.s)) is higher than values reported in current diamond H-terminated MOSFET (50-500 cm^2/(V.s)) [18]. However, recent reports demonstrate that high mobility should be reached in 2D hole gas at the interface between dielectric and diamond [19, 20], even larger than the one of bulk. The main advantages of bulk channel is the better understanding of the physical mechanism behind the electrical conduction and blocking capabilities. Indeed, the surface accumulation of 2D hole gas (2DHG) obtained by the surface transfer mechanism is difficult to control, with non reproducible characteristics and it is not clear how the electric field is distributed in the off-state of these devices. A linear relationship between the drain-gate distance L_{GD} is observed. The breakdown voltage BV, with a ratio BV/L_{GD} around 1-2 MV/cm [21], is far from the diamond breakdown field. Whatever, the possibility to create hybrid technologies associating 2DHG and bulk conduction, as proposed below, is probably the most promising way to create future efficient diamond devices.

However, a severe drawback of this bulk conduction design is caused by the high ionization energy of boron acceptors in $p-$type diamond (380 meV), at the origin of a large negative temperature coefficient above room temperature of the device resistance. To modulate the conductivity of the device and observe the transistor field effect, a

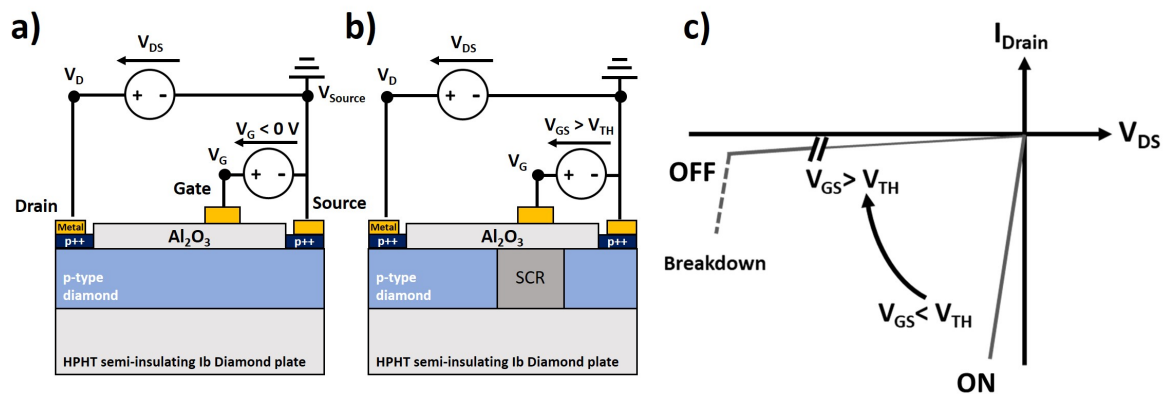

Figure 3. Schematic cross section of the p-type diamond deep depletion MOSFET device in a) on-state and b) off-state, with c) the corresponding schematic current voltage characteristics.

Metal-Oxide-Semiconductor (MOS) gate stack is used. When biased, the electric field repels or accumulates majority carriers below the gate in an area called Space Charge Region (SCR) of thickness W_{SCR}. The device is typically normally-on. The off-state is reached in deep depletion regime with a gate bias equal or higher than the threshold voltage V_{TH}, at which W_{SCR} is equal to the channel thickness (fig. 3 b)). The drain current I_D is effectively modulated by the gate to source bias V_{GS} (fig. 3 c)). For intermediate gate bias, a pinch-off of the channel is observed for drain source voltage determined by the geometrical and physical parameters of the channel. Thanks to the deep depletion concept in wide band gap semiconductors, W_{SCR} can be designed much larger than when using a lower band gap material such as silicon. This permits to minimize the losses in the device by designing a low on-state resistance R_{ON}.

3. Design of diamond deep depletion MOSFET

In this section, the basic considerations concerning the design of the D3MOSFET will be given. The first part will be dedicated to the physical parameters (doping and thickness) of diamond channel and oxide and their influence on the electrical properties of the FET. The second part consists in a discussion about the prospective design and improvements to implement in D3MOSFET.

3.1. From physical key parameters (doping, thickness, oxide) to electrical properties (R_{ON}, V_{BD}, V_{TH})

3.1.1. R_{ON} versus temperature A bulk channel conduction is used in the D3MOSFET. Also, the resistance of the device is directly dependent on the bulk mobility and carrier concentration dependence versus temperature. In most of the semiconductors, a temperature increase over room temperature is degrading the resistance, due to the

decreasing mobility induced by carrier-phonon interaction. However, diamond possesses deep dopants: 380 meV ionization energy for boron acceptors and 570 meV ionization energy for phosphorus donors. Consequently, the resistivity of diamond is limited by the incomplete ionization of dopants. It results in a negative temperature coefficient up to an optimum in the range of 500 K - 700 K depending on the doping level. The 1D electrical resistivity ρ (in $\Omega.cm$) of a semiconductor is expressed as :

$$\rho(T, N_A, N_D) = \frac{1}{qp(T, N_A, N_D)\mu(T, N_A, N_D)} \tag{8}$$

where $\mu(T, N_A, N_D)$ is the hole mobility of carriers and $p(T, N_A, N_D)$ is the free hole density which are estimated as function of doping level and temperature using the empirical model developed in ref. [22]. Detailed values of $\mu(T, N_A, N_D)$, $p(T, N_A, N_D)$ and $\rho(T, N_A, N_D)$ have been reported in ref.[23] for doping and compensation ranging between 10^{14} cm$^{-3} < N_A < 3 \times 10^{20}$ cm^{-3} at 300 and 500 K. A focus will be done here for doping and compensation densities and temperature in the range of interest for the D3MOSFET.

Before considering temperature dependence of hole concentration p, the acceptor ionization energy versus doping level is reported because of its strong impact on p. This dependence is fitted by the Pearson and Bardeen model [24] with adjusted parameters to obtain the reported 0.38 eV boron ionization energy [25], shown in Fig. 4.

$$E_A = E_{A,0} - \alpha \times N_A^{\frac{1}{3}} \tag{9}$$

where $E_{A,0} = 0.38$ eV is the ionization energy at low doping level, $\alpha = 5.5 \times 10^{-8}$ eV.cm is a fitting parameter to obtain the metal-insulator transition at the critical density 3×10^{20} cm^{-3} [26] and N_A is the doping level in cm^{-3}.

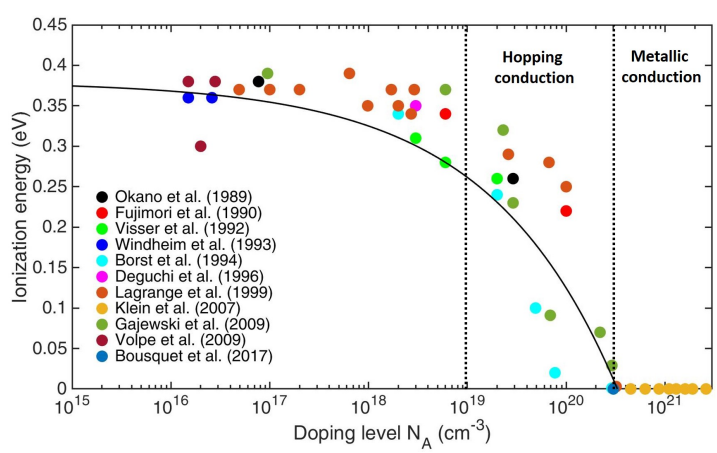

Figure 4. Ionization energy of boron in diamond as function of doping level. Symbols are experimental points extracted from [22, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35] and the full line is a fit using the Pearson and Bardeen model [24] adjusted to obtain the metal-insulator transition at 3×10^{20} cm^{-3} and a ionization energy of 380 meV at low impurity concentration.

As shown in fig. 4, for doping levels below 10^{19} cm^{-3} the experimental values of ionization energy of boron are stable at an approximate value of 380 meV, which corresponds to the energy difference of the boron acceptor level and the maximum of the valence band. For higher doping level values, 10^{19} cm$^{-3} < N_A < 3 \times 10^{20}$ cm^{-3}, E_A is decreasing due broadening and then overlapping of the acceptor wave functions. Moreover, the distance between dopant is small enough to allow carriers to hop from one site to another, with various hopping mechanisms depending on temperature, doping and compensation, decreasing the resistivity as function of dopant concentration. For a doping level above the metal-insulator transition, $N_A > 3 \times 10^{20}$ cm^{-3}, E_A is lowered down to zero as the boron impurity band conduction merges with the valence band, analogous to the conduction in a metal with $p = N_A - N_D \simeq N_A$. In this metallic conduction regime, the resistivity is orders of magnitude lower than below the transition and almost no temperature dependence is observed. This is well suited to perform low resistivity ohmic contacts at the drain and source of diamond FET devices.

The typical range of doping levels used in the active regions of power FETs is below 10^{18} cm^{-3} since high doping levels lead to lower breakdown voltages as discussed below. Therefore, only the case of a non degenerate semiconductor is considered here, with a constant ionization energy equal to the low impurity concentration value, $E_A = E_{A,0} = 380$ meV, and no hopping conduction mechanisms. Then, the free hole concentration can be expressed by [22]:

$$p(T) = 0.5(\phi_A + N_D)\left(\left[1 + \frac{4\phi_A(N_A - N_D)}{(\phi_A + N_D)^2}\right]^{0.5} - 1\right) \tag{10}$$

Where

$$\phi_A = 0.25 N_V(T) T^{1.5} e^{\frac{E_A}{k_B T}} \tag{11}$$

From this equation, the dramatic effect of compensation can be evaluated as shown in Fig. 5 a) for a doping level of 2×10^{17} cm^{-3}. Hole concentrations with compensation ratios ranging between 0% and 10% are calculated, which corresponds to common reported values for various doping levels [23]. As only few acceptors are ionized around room temperature, part of the carriers are trapped by donor atoms and the free hole density is drastically decreased. For example, the hole concentration at room temperature with no compensation is calculated to be $p(300K)_{0\%} = 1.15 \times 10^{15}$ cm^{-3}, corresponding to an ionization ratio of 0.58%. With a 6% compensation ratio, this value drops by an order of magnitude to $p(300K)_{6\%} = 1 \times 10^{14}$ cm^{-3}, corresponding to an ionization ratio of 0.05%. The carrier concentration increases versus temperature and the detrimental compensation effect tends to be reduced. Using the previous examples at 600K, one can estimate that $p(600K)_{0\%} = 5 \times 10^{16}$ cm^{-3} (25% ionization ratio) and $p(600K)_{6\%} = 4.4 \times 10^{16}$ cm^{-3} (22% ionization ratio). The negative temperature coefficient in diamond is then greatly dependent on the compensation ratio, even for low compensation concentration values, but this dependence is strongly lowered at higher temperature.

Hole mobility is a temperature and doping level dependent parameter which greatly influences the resistivity of the material. In a bulk conduction device, where surface effects are negligible, only phonon and impurities scattering are considered, as explained in more details in Ref. [7]. The empirical model developed in ref. [22] provides a reliable approach to evaluate the mobility in order to calculate the on-state resistance of the final device.

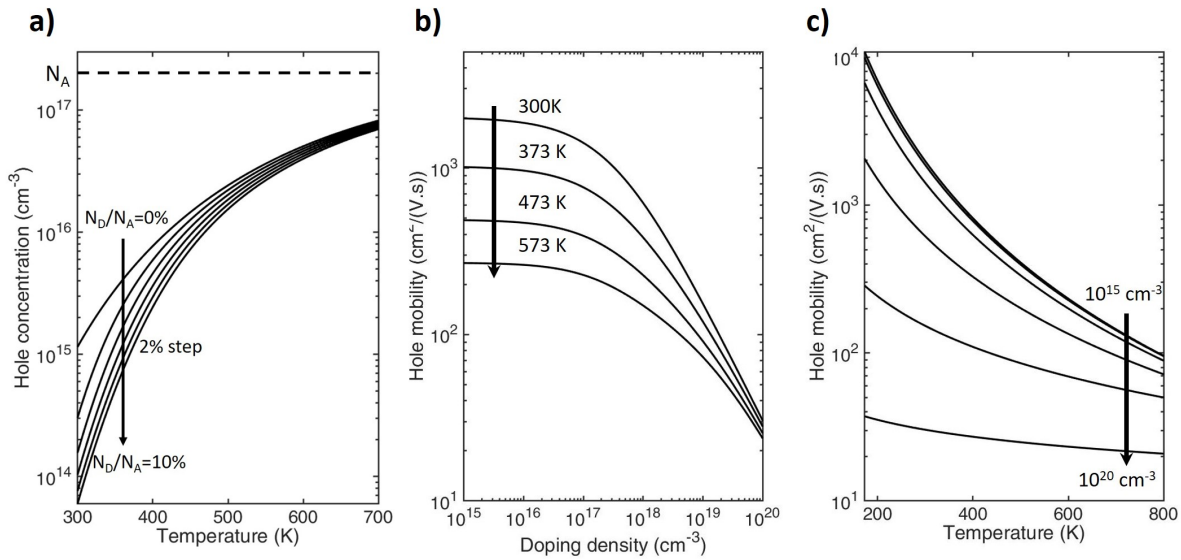

Figure 5. a) Calculated free hole concentration of p-type diamond as function of temperature for different compensation ratios on a layer doped at 2×10^{17} cm^{-3}. b) Calculated hole mobility as function of the doping density for different temperatures. c) Calculated hole mobility as function of the temperature for different doping densities between 10^{15} cm^{-3} and 10^{20} cm^{-3} with one decade step.

As shown in Fig. 5 b), the weak mobility dependence versus doping level for $N_A < 10^{17}$ cm^{-3} is due to the dominance of the intrinsic scattering by phonons. The mobility at 300K in a boron doped diamond at 10^{15} cm^{-3} is around 2000 cm^2/(V.s) compared to 1400 cm^2/(V.s) at 10^{17} cm^{-3}. Above this value, a steeper decrease of the mobility is observed due to the impurities scattering mechanisms being dominant, dropping to 150 cm^2/(V.s) at 10^{19} cm^{-3}. Fig. 5 c) shows that for temperatures above room temperature, all scattering mechanisms (phonons and impurities) have a strong negative temperature coefficient. The mobility of a layer doped at 10^{17} cm^{-3} decreases from 1400 cm^2/(V.s) at room temperature to 400 cm^2/(V.s) at 200 °C.

Using the models to calculate μ and p, the resistivity can be estimated as function of temperature, doping level and compensation with Equ. 8, shown in Fig. 6 a), b) and c) respectively. Around room temperature and below, the ionization of dopants dominates the resistivity variation versus temperature, causing the negative temperature coefficient. Eventually when increasing temperature, the higher ionization ratio is hindered by the decrease of the mobility due to optical phonon scattering, inducing

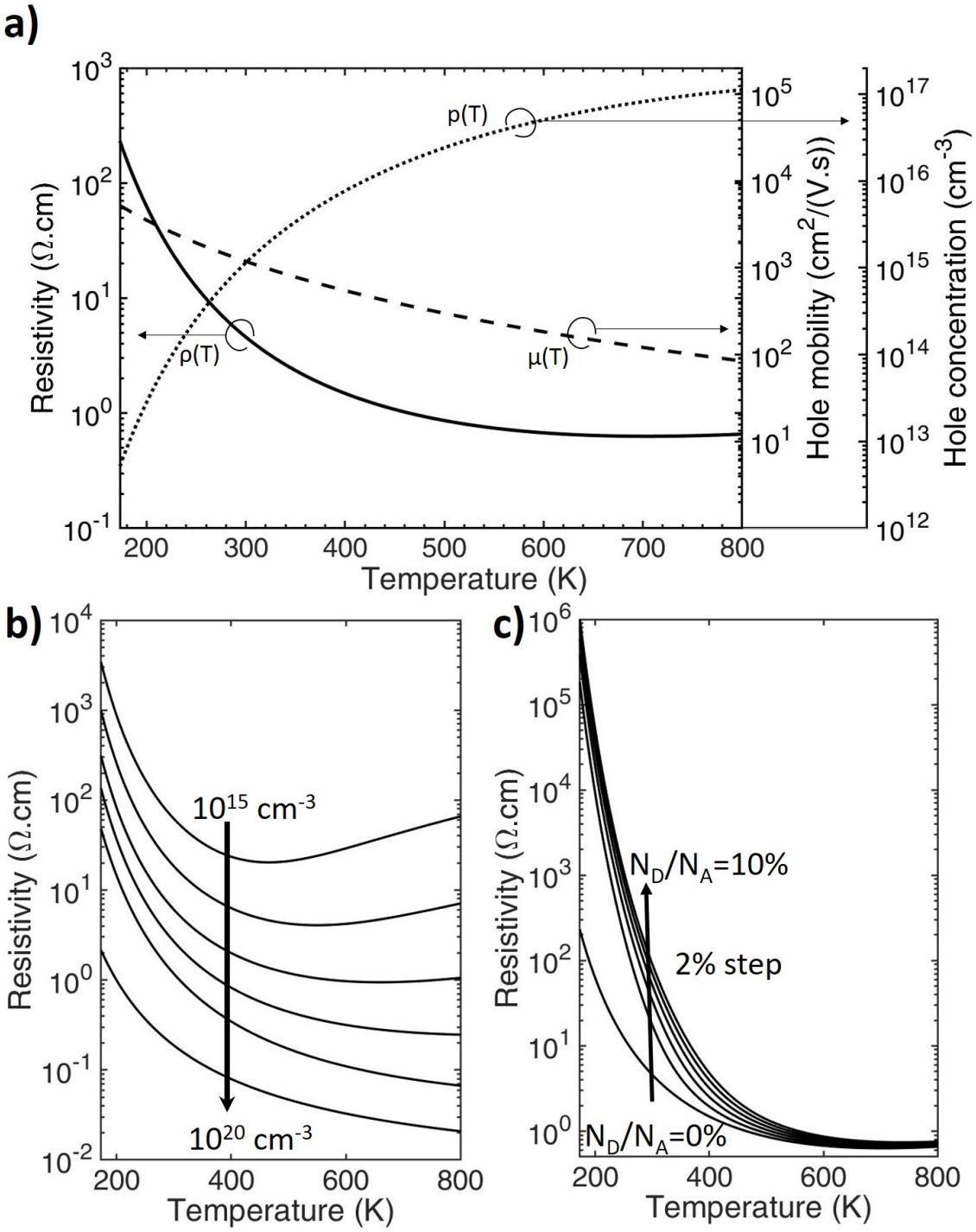

Figure 6. a) Resistivity, hole concentration and hole mobility as function of temperature for a doping level of 2×10^{17} cm^{-3} and no compensation. b) Resistivity as function of temperature for doping levels ranging between 10^{15} cm^{-3} and 10^{20} cm^{-3} with a decade step, compensation is set to 0. c) Resistivity as function of temperature for a doping level of 2×10^{17} cm^{-3} and a varying compensation ratio between 0% and 10%.

an increase of resistivity with temperature. The minimum of the resistivity is doping level dependent, around 450 K for 10^{15} cm^{-3}, but this value is strongly increasing as function of the doping level, to non practical temperatures for a device (550 K at 10^{16} cm^{-3} and 660 K at 10^{17} cm^{-3}). Then, except for very low doping level values, the negative temperature coefficient is expected in the full working temperature range of the diamond devices based on bulk conduction.

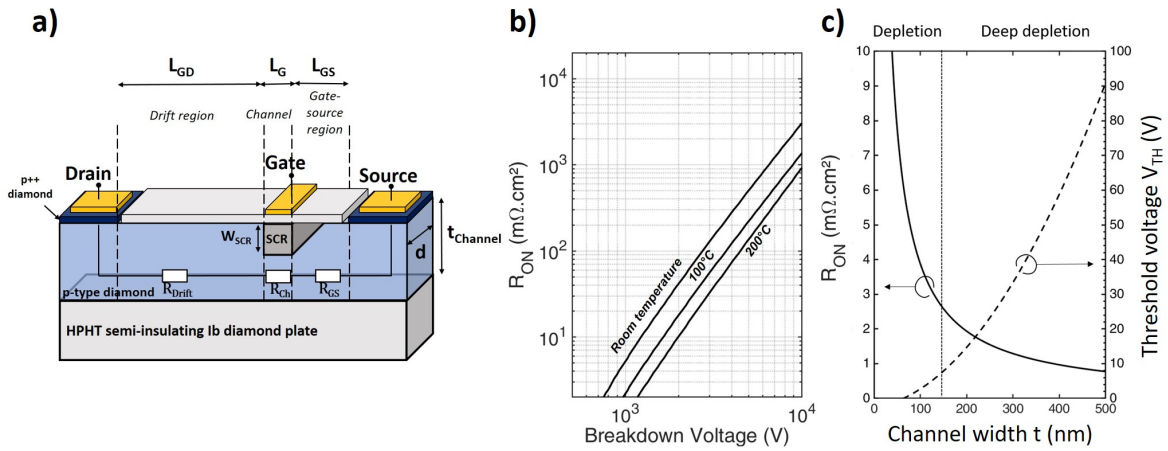

Figure 7. a) Schematic cross section of the D3MOSFET. b) Calculated R_{ON} vs V_{BD} trade-off for the lateral D3MOSFET at room temperature, 100 °C and 200 °C. An ideal structure is considered (no parasitic effects, no compensation) and the p-type layer thickness is calculated to obtain a threshold voltage of 15 V with an oxide thickness of 50 nm. The $R_{ON} \approx R_{Drift}$ approximation is used. c) R_{ON} (full line) and V_{TH} (dashed line) trade-off as function of the channel thickness for a lateral device at 200 °C and a doping level $N_A = 2 \times 10^{17}$cm^{-3}. Oxide thickness is set at 50 nm and the flatband voltage at -2.6 V.

3.1.2. R_{ON} versus V_{BD} When considering the case of a non depleted conducting channel ($W_{SCR} = 0$), with no contact resistances ($R_{C,D}$ and $R_{C,S} = 0$) as shown in Fig. 7 a), R_{ON} can be expressed by:

$$R_{ON} = \rho \times \frac{L_{Drift} + L_{Ch} + L_{GS}}{d \times t_{Channel}} \tag{12}$$

where ρ is the resistivity of boron doped diamond given by Equ. 8. It is useful to define and use a normalized resistance, the specific on-resistance $R_{ON,S}$, defined by: $R_{ON,S} = R_{ON} \times d \times (L_{Drift} + L_{Ch} + L_{GS})$ generally given in mΩ.cm^2. As $R_{ON,S}$ is normalized by the active surface area of the device, it can be used as a comparison between devices with varying designs and dimensions. $R_{ON,S}$ writes:

$$R_{ON,S} = \rho \times \frac{(L_{Drift} + L_{Ch} + L_{GS})^2}{t_{Channel}} \tag{13}$$

A trade-off exists between the on-state resistance R_{ON} and the maximum blocking voltage in off-state V_{BD} of a device. Minimization of R_{ON} requires to minimize the drift

region length L_{GD} and maximize the doping level N_A in order to decrease the resistivity. At the opposite, the maximization of V_{BD} requires to decrease the doping level. For the sake of simplicity, we only consider the resistance of the drift layer in on-state, which is generally much larger than the channel and gate-source region resistances. Also, one can write $R_{ON} \approx R_{Drift}$. This optimization of N_A and L_{GD} has been performed using a 1D model including impact ionization coefficients determined by Hiraiwa et al.[5, 36] for different temperatures. The results are plotted in Fig. 7 b).

3.1.3. R_{ON} versus V_{TH} Thanks to the deep depletion concept in wide band gap semiconductors, it is possible to use thick epilayers as channel to reduce the resistance. This is however at the cost of an increasing threshold voltage V_{TH} to reach the off-state as the SCR extension W_{SCR} is square root dependent on the applied bias:

$$W_{SCR} = \sqrt{\frac{2\epsilon_{Diamond}(V_G - V_{FB} - V_{OX})}{qN_A}} \tag{14}$$

where V_{OX} is the potential drop across the oxide layer, V_G the applied bias on the gate metal, V_{FB} the flat-band potential (-2.6 V in case of a titanium metal contact).

The threshold V_{TH} can be tuned by selecting the epilayer thickness, i.e. the channel thickness, the doping level N_A and the nature of the metal and the oxide relative dielectric constant and thickness. N_A is generally fixed by the targeted device breakdown voltage depending the application. For a given doping level N_A, a low V_{TH} transistor needs a thin channel, corresponding to a high R_{ON}, and a thin gate dielectric layer thickness t_{OX} and high relative dielectric constant ϵ_{OX}. An example of V_{TH} versus channel thickness and its corresponding R_{ON} is shown in Fig. 7 c) for a lateral device at 200 °C having a doping level $N_A = 2 \times 10^{17}\text{cm}^{-3}$, an oxide thickness of 50 nm and a flatband voltage of -2.6 V.

As implied in Equ. 14 and illustrated in Fig. 8 a) the thickness of the SCR is dependent on the potential drop across the oxide, given by: $V_{OX} = Q_M/C_{OX}$ with $C_{OX} = \epsilon_0\epsilon_{OX}/t_{OX}$ the surfacic capacitance of the oxide layer (F/cm^2) and Q_M the surfacic charge of the gate metal (C/cm^2). ϵ_0 is the vacuum permittivity. V_{OX} being linearly dependent on the oxide thickness, an increase of t_{OX} necessitates to apply a higher gate bias to reach the same surface potential. The threshold voltage V_{TH} versus t_{OX} dependence is shown in Fig. 8 b) for Al_2O_3, SiO_2 and h-BN‡ with relative dielectric constants of respectively $\epsilon_{Al_2O_3}$ =8.8 §, ϵ_{SiO_2} =3.9 and ϵ_{h-BN} =3 [37]. In this work, Al_2O_3 has been chosen, as in most of other diamond MOSFETs, because of the simplicity and availability of Atomic Layer Deposition (ALD) and because its high dielectric constant is beneficial to reduce the threshold voltage as shown in fig. 8 b). The oxide deposition conditions have been previously optimized [38]. SiO_2 has also been used occasionally, as well as h-BN which has recently shown promising results as a gate dielectric [39], with a breakdown field of 6.6 MV/cm. The deposition method used so

‡ h-BN is an insulator and not an oxide but for sake of simplicity we will keep the same notation.
§ Measurements done on metal insulator metal structures reported below in this work.

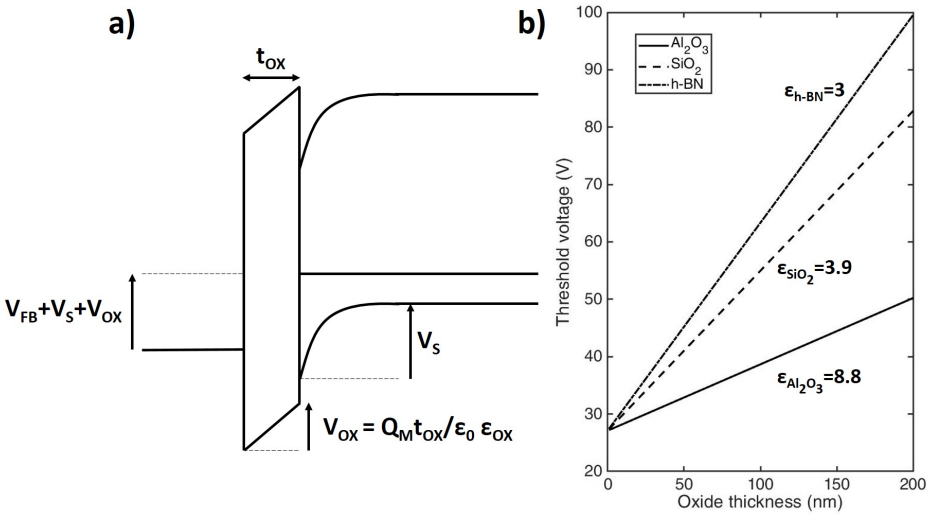

Figure 8. a) Schematic band diagram of MOSCap structure in depletion, the potential drop in the oxide is illustrated. b) Calculated threshold voltage V_{TH} as function of the oxide thickness t_{OX} for a doping level $N_A = 2 \times 10^{17}\text{cm}^{-3}$ and a channel thickness of 300 nm. The relative dielectric constant of the oxide ϵ_{OX} is set at 8.8 for Al_2O_3, 3.9 for SiO_2 and 3 for h-BN. [37]. The flatband voltage is set at -2.6 V.

far, the Scotch tape exfoliation technique, is however rather complex to reproduce. The choice of the oxide is however an important and more complex topic, as in addition to their physical parameters many effects are related to the deposition method and the fabrication process in general. As such bulk traps, the chemistry at the diamond/oxide interface, the stability with temperature and electrical stresses are important parameters for the device operation. Most of the literature on diamond MOS structures is focused on Al_2O_3 and steady improvements have been accomplished over the years with this material, allowing for the fabrication of MOSFETs. But it is still unclear if Al_2O_3 is the best gate oxide and achieving a sufficient control of the charge trapping effects still requires extensive efforts.

While in the ideal case considered here, the field in the oxide is independent on its thickness: $E_{OX} = Q_M/\epsilon_0\epsilon_{OX}$, large differences in oxide breakdown values are observed as function of t_{OX}. This can be due to edge effects but also to charging effects at the diamond/oxide interface as well as in the bulk of the oxide. The presence of traps can cause the electric field distribution in the oxide to not be uniform, which is exacerbated for thin layers and cause premature breakdown as well as increased leakage current. As a consequence H-terminated diamond MOSFET with thick oxide layers are reported to exhibit higher breakdown values [40, 21], a study of oxide thickness effect as yet to be realized on O-terminated MOS.

3.2. How to improve the D3MOSFET performances thanks to the design?

3.2.1. Edge terminations Thanks to the very high critical field of diamond, the reported lateral MOS devices are most likely showing a destructive breakdown of the oxide layer prior to the apparition of avalanche effect in diamond [41, 40, 4, 42, 43, 44]. Indeed, the Al_2O_3 breakdown field has been measured to be around 6 MV/cm, which is in many cases lower than diamond breakdown field. To observe avalanche breakdown in a diamond MOS structure, reduction of electric field crowding effects is expected to be even more important than with other materials. The use of edge termination structures is a well known way to improve the breakdown voltage of devices by reducing the electric field crowding effect. In diamond Schottky diodes, floating metal rings have been investigated [45] as well as field plates architectures [46]. Although their benefits are evidenced, the demonstrated breakdown electric field are still low in comparison to diamond capabilities. Additionally, a special care must be taken during the fabrication process, and more specifically lithography and metal deposition process, which could induce imperfections creating a local electric field crowding [47].

3.2.2. Recess gate The on-state resistance of the proposed D3MOSFET is dominated by the drift region resistance R_{Drift} especially at low doping density (high blocking voltage) where the drift region is much longer than the gate length and gate-source distances. It can be optimized by the use of a recess gate architecture described in Fig. 9 a) and b), which consists in the use of a thicker p-type layer with a thinned channel by etching. The structure has been described in the patent[48]. The thickness of the channel and the choice of the gate metal is designed so the 0 V gate bias SCR extension is enough to deplete the layer completely, achieving the normally-off operation (Fig. 9 a)). The MOS stack is then biased in accumulation in on-state to reduce the resistive channel region (Fig. 9 b)). One of the advantages of this structure over the standard lateral design is to obtain the normally-off characteristic, avoiding the necessary use of additional external devices needed in case of a normally-on transistor, for safety purpose. Moreover, the channel resistance R_{Ch} is greatly reduced by the hole accumulation layer and R_{Drift} and R_{GS} can be lowered by the use of a thicker p-layer as it is no more limited by the R_{ON} vs V_{TH} trade-off.

It is however, at the moment, challenging to obtain an accumulation layer in diamond MOS structures, to take the full advantage of this architecture. Previous reports based on capacitance measurements of O-terminated diamond MOS capacitors [49, 50, 38, 51] claimed to achieve accumulation regime in O-terminated MOSFET. However, no evidence of conducting accumulation gas at diamond/oxide interface were reported in these works. Accumulation layer has nonetheless been demonstrated in a diamond lateral FinFET [52] using ALD SiO_2 as gate oxide, but the authors could not extract the hole mobility of the channel as the accumulation layer may not be formed on the full channel surface. Recently, Zhang et al [53, 54] reported the accumulation regime in a (111) OH-terminated diamond MOSCap with an interface state density

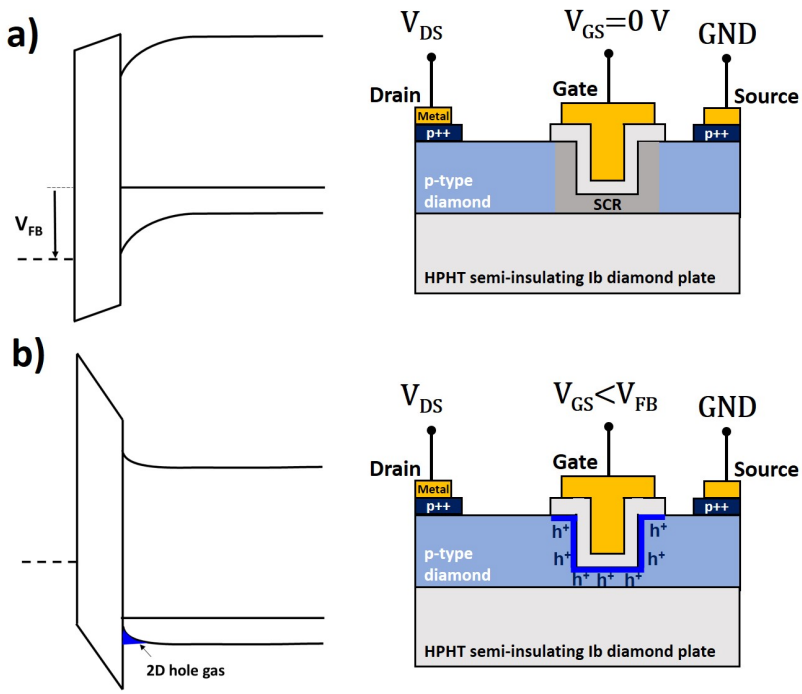

Figure 9. a) Schematic cross section of the recess gate diamond depletion MOSFET architecture and corresponding band diagrams for a) $V_{GS} = 0$ (normally-off state) and b) for $V_{GS} < V_{FB}$ (on-state)

lower than 1.5×10^{12} cm$^{-2}.eV^{-1}$. The gate insulator optimization is a key challenge to reduce parasitic capacitance coming from oxide and interface defects. Diamond MOSCap interface states densities reported in literature are usually in the range of 10^{12} cm$^{-2}.eV^{-1}$ or above, which is too high to reliably form a 2D hole gas in accumulation regime. Notably due to the strong Fermi level pinning effect. A reduction to values in the 10^{10} cm$^{-2}.eV^{-1}$ range is required to significantly increase the 2D hole gas mobility and offer the best conduction and gate control[19]. This problem is as well tied to the poor diamond MOSFET dynamic performances. Large parasitic capacitance induced by slow responding traps increase the time needed to fully open or close the channel, greatly limiting the current rating during fast switch. Hence, most reports focus on devices quasi-static characteristics. To fabricate an efficient recess gate diamond MOSFET, surface treatments, insulator material choice and its deposition method need to be investigated.

3.2.3. Vertical depletion MOSFET The lateral D3MOSFET is the most feasible architecture as for now considering the fabrication processes limitations. However, to compete with other wide band gap semiconductors devices, vertical designs need to be investigated to lower R_{ON} and to better control electric field crowding effects. A schematic example of the cross section of this kind of structure is provided in Fig. 10 a) in off-state and Fig. 10 c) in on-state. This design is similar to the vertical FinFET

designs demonstrated on GaN [55, 56, 57] and Ga_2O_3 [58, 59, 60]. Thanks to the vertical drift region, the surface area of the chip is much smaller than a lateral drift design for equivalent performances. To give an estimated benefit on the conduction capabilities, lateral and vertical R_{ON} versus BV characteristics are compared in Fig. 10 c) at 200 °C. As a first approximation, only the drift resistance is considered to compare the specific on-state resistances with a 1D current distribution:

$$R_{ON,S}^{Lateral} = \rho \times \frac{L_{Drift}^2}{t_{Channel}} \tag{15}$$

$$R_{ON,S}^{Vertical} = \rho \times L_{Drift} \tag{16}$$

Then, the ratio of the vertical resistance over the lateral one can be approximated:

$$\frac{R_{ON,S}^{Vertical}}{R_{ON,S}^{Lateral}} = \frac{t_{Channel}}{L_{Drift}} \tag{17}$$

To have a benefit in using the lateral architecture, $t_{Channel}$ has to be larger than L_{Drift}. Considering L_{Drift} is designed as the SCR extension at breakdown, it is impossible to obtain off-state by using a thicker channel than L_{Drift}. With this simple approximation, not taking into account the 2D and 3D effects of the distribution of the current, an improvement of at least one order of magnitude is expected.

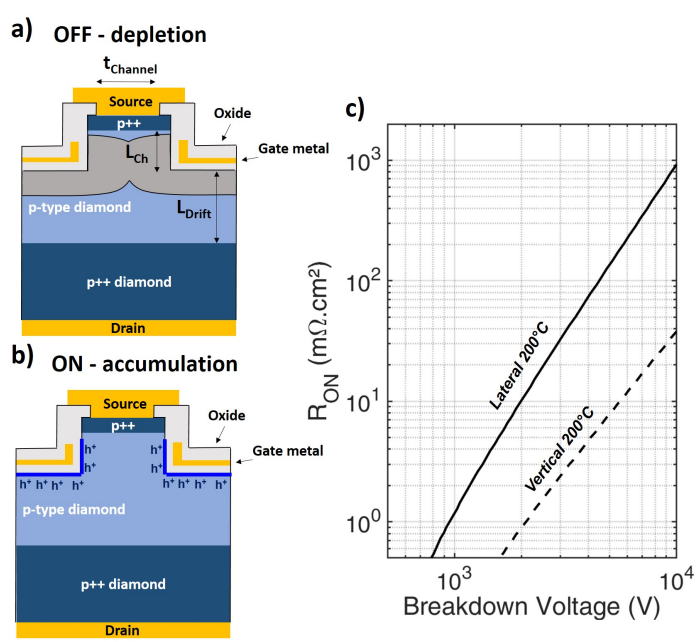

Figure 10. Schematic cross section of the vertical diamond depletion MOSFET a) in on-state and b) in off-state. c) Calculated R_{ON} vs V_{BD} trade-off for the proposed vertical architecture compared to the lateral architecture at 200 °C with $t_{ox} = 50$ nm and $V_{TH} = 15$ V.

However, numerous difficulties make challenging the fabrication of this vertical architecture with diamond: (i) The growth of a few micrometers thick and defect free

$p^{++}/p/p^{++}$ stack , as vertical designs are more susceptible to defects such as hillocks, for most of them expand vertically during growth. Threading dislocations are reported to be at the origin of leakage current [61] and could be at the origin of premature breakdown in vertical design. (ii) The need for a reliable etching technique with smooth side walls and a process to remove etch pits. (iii) The control of the MOS interface, especially on the side walls of an etched diamond surface. The large trap density at the oxide diamond interface is especially prohibitive in the case of a normally-off FinFET design.

	Short term			**Long term**	
	Recess gate	**Edge termination**	**Gate insulator optimization**	**mm² sized device**	**Vertical design**
Advantages	• Reduce the on-state resistance R_{ON} of the lateral design. • Normally-off operation.	• Increase the breakdown voltage V_{BD} by reducing the electric field crowding effect.	• Reduce parasitic capacitances thanks to lower interface state density. • Suppress the Fermi level pinning effect and reach accumulation regime.	• Increase the current rating of devices to several Amps • Open the way to demonstrate power applications with diamond based devices.	• Further reduction of R_{ON} and possibly higher V_{BD} as well. • Expected performances better than SiC and other wide band gap devices. • Normally-off design.
Key limitations	• Oxide/Diamond interface on etched area.	• Only moderate gains obtained up to now, far from the diamond potential: the process complexity is limited by the small substrate area. • Oxide breakdown field lower or close to diamond.	• Reach low diamond surface defects and dangling bonds prior to insulator deposition. • Limited choice of insulators due to band alignement compatibility with diamond.	• Lack of high quality homo and hetero-epitaxy monocristalline diamond, grown on large area substrate. • Process yield must be improved.	• Small substrate area: overall fabrication process challenging at the moment. • Need for thick, low defect density epilayers. • Oxide/Diamond interface on etched trenches.

Table 1. Key improvements to diamond MOSFETs devices and their limitations.

3.2.4. Summary and additional perspectives The Table 1 summarizes the key improvements proposed in terms of design, for the short and long terms. On the short term, the lateral design can be optimized to decrease its on-state resistance and increase its voltage rating, through the use of the recess gate design and edge terminations respectively. One of the main challenge is to achieve a reliable, predictable control of the electric field in the device, to limit electric field crowding effects and suppress interface parasitic capacitance. This translates in the reduction of the defect density, in the insulator and at the interface. More so in the recess gate design where the insulator is deposited on a damaged etched area. Moreover, these interface defects are neutral and charged impurities, which can cause a substantial reduction of the 2D hole gas mobility in accumulation regime, impacting the on-state resistance of the recess gate device. On the long term, the demonstration of a mm^2 sized device with several Amps current rating would be a break-through. It would allow the demonstration of a diamond based, or

partially diamond based, power converter. However, at the moment the defect density of both substrates and epilayers is too high to reliably fabricate large devices. This was well demonstrated by Umezawa et al.[62] for the fabrication of Schottky diodes. Increasing the substrate size with homo or hetero-epitaxy will be necessary as well to improve the yield of mm^2 sized devices, since currently only one or a few devices can be fabricated on the same substrate. The only availability of cm^2 sized substrates at most exacerbates this problematic, most of the microelectronic processing machines are not compatible and not optimized for these substrates area. This leads to extensive manual sample manipulation and out of specifications use of these machines. The contamination control throughout the fabrication process is then greatly limited.

Finally a vertical design would bring the diamond MOSFET's performances higher than other wide band gap devices, both in terms of current and voltage ratings. This however sums up all the upper mentioned challenges regarding the substrate, epitaxy, gate insulator and fabrication process.

4. Fabrication and characterization of lateral diamond deep depletion MOSFET

4.1. Fabrication process

The diamond deep depletion MOSFET was first demonstrated in [2, 3, 4]. In these previous works, two samples were fabricated (MOS1 and MOS2, described in more details by T. T. Pham [63]) with a boron doped p-type diamond layer grown by plasma assisted CVD (PA-CVD) as channel, on top of a semi-insulating 1b diamond plate. Ti/Pt/Au stacks were used for source and drain ohmic contacts because Ti creates a good adherence on diamond thanks to carbide formation, the Pt layer is acting as a diffusion barrier between Au and Ti and Au is preventing the oxidation of Ti. After an UV ozone treatment, an alumina layer was deposited by ALD at 380 °C (the upper limit of our ALD setup), followed by a post annealing at 500 °C. This process has been reported to form a crystalline alumina layer [38] with a reduced leakage current and lower interface states density, compared to a lower temperature deposition [49, 64]. Other diamond FETs analysis are reported to use a 450 °C temperature deposition to reduce leakage current [21, 40, 65, 66].

MOS1 and MOS2 transistors are exhibiting a clear transistor effect with a maximum blocking voltage at $V_{BD} = -200\,V$ on MOS1. Transistors of MOS2 could not be switched off due to an excessive threshold voltage and so, breakdown was not characterized. These devices suffered from a much higher than expected on-state resistance, with a barrier effect for low drain bias, partly due to a high contact resistance. Indeed, an ohmic behaviour by metal deposition on lightly doped p-diamond is challenging to obtain. To improve the contact resistance, a selective growth technique has been developed to produce reliable source and drain ohmic contacts, in addition to the MOS1 and MOS2 sample process flow, as shown in fig. 11. Using a metallic mask deposited by

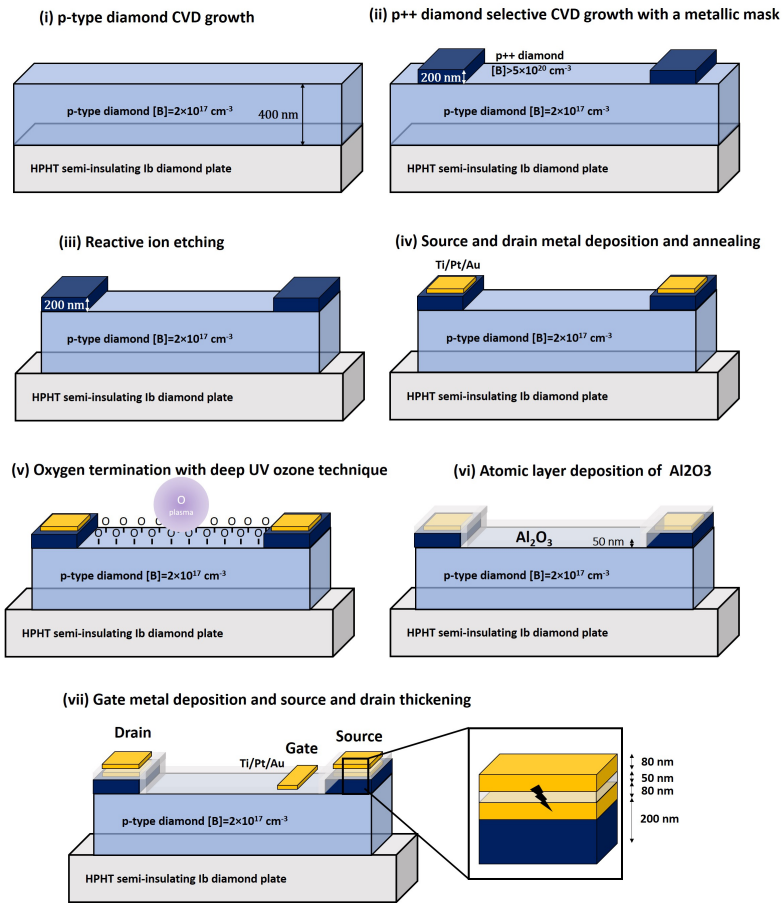

Figure 11. Schematic cross section of a D3MOSFET on MOS8 sample at the main fabrication steps.

lithography, a highly doped p-type diamond ($[B] > 5\times10^{20}$ cm^{-3}) is selectively grown at source and drain contact areas, which will be shown to result in low contact resistances, negligible with respect to the diamond p-layer resistance. Mesa structures were also fabricated by selective etching of diamond, down to the semi-insulating substrate, to obtain electrically insulated MOSFETs on the same sample with the idea to parallelize them. Moreover, large area gate contacts can be shifted on the insulating etched surface, to be connected safely by probe tips and reduce the leakage current. This process flow is however not straightforward considering the non-standard dimension of the diamond substrates ($4\times4\times0.5$ mm^3), requiring to adapt the equipment to this unusual shape and dimension. As shown in Fig. 11, the source and drain metal contacts deposited on step (iv) are covered by an alumina layer. This has been an issue to perform measurements in samples MOS1 and MOS2 as the oxide layer had to be mechanically broken with the probe tip each time a measurement was performed. Instead, it was decided to use the gate metal deposition step (vii) to deposit an additional layer on top of the source and drain contacts. The metal-oxide-metal stack formed is then electrically broken at the first measurement by applying a high bias voltage. Subsequent measurements are then

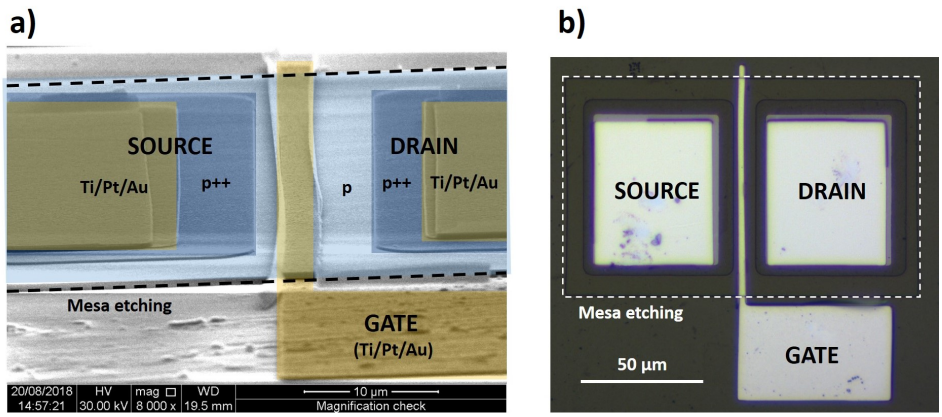

Figure 12. a) SEM image of a fabricated transistor on MOS8 with a tilt angle close to 90°. b) Optical top view of the transistor.

easy to perform. This process, while not ideal, leads to a negligible contact resistance in comparison to the p-type diamond layer resistance. An etching of the oxide on the source and drain contact would ideally be preferable, but requires an additional lithography step. SEM view of a singular device is shown in Fig. 12 a) with a tilt angle close to 90° to clearly observe the mesa. While the substrate's surface seems relatively rough after the etching and mask removal, the p-type layer remains smooth. Fig. 12 b) shows the device optical top view.

4.2. Quasi-static transistor characteristics (I_{DS} versus V_{DS}, I_{DS} versus V_{GS})

The successful operation of the D3MOSFET at room temperature and 523 K is shown in Fig. 13 a) and b) respectively. A clear on and off-states with $V_{TH} \approx 35$ V are obtained. The measured transistor dimensions are $d = 110$ μm, $L_{GS} = 4$ μm, $L_G = 2$ μm and $L_{GD} = 10$ μm. At room temperature, the sample is exposed to a white light irradiance of 11 mW/cm^2 and the source and substrate were short-circuit ($V_{Sub} = V_{Source}$) in order to modulate the back PN junction formed by the $p-$type layer and the insulating $n-$type substrate. The room temperature drain-source saturation current at $V_{DS} = -40$ V and $V_{GS} = -10$ V is 0.12 mA/mm, corresponding to more than 5 order of magnitude higher in off-state, which is below the detection limit of 1 nA/mm for $V_{GS} = +40$ V. The gate leakage current also remained below detection limit, $I_{GS} < 1$ nA/mm, in the range of V_{DS} (0 to -40 V) and V_{GS} (-10 to +40 V) measured.

A weak increase of gate leakage current was observed when heating the sample up to 250 °C, i.e. $V_{DS} = -40$ V and $V_{GS} = 40$ V, $I_G = 15$ nA/mm. The D3MOSFET exhibits a high on-state over off-state drain current ratio $\mathrm{I}_D^{ON}/\mathrm{I}_D^{OFF} \approx 5 \times 10^5$ at 250 °C. This is of importance as diamond is the best semiconductor candidate for high temperature applications. The transistor characteristic does not seems to suffer from such elevated temperatures. For this specific MOSFET device, the sample suffered several thermal cycles, i.e. heated up to 250 °C and cooled down to room temperature without any

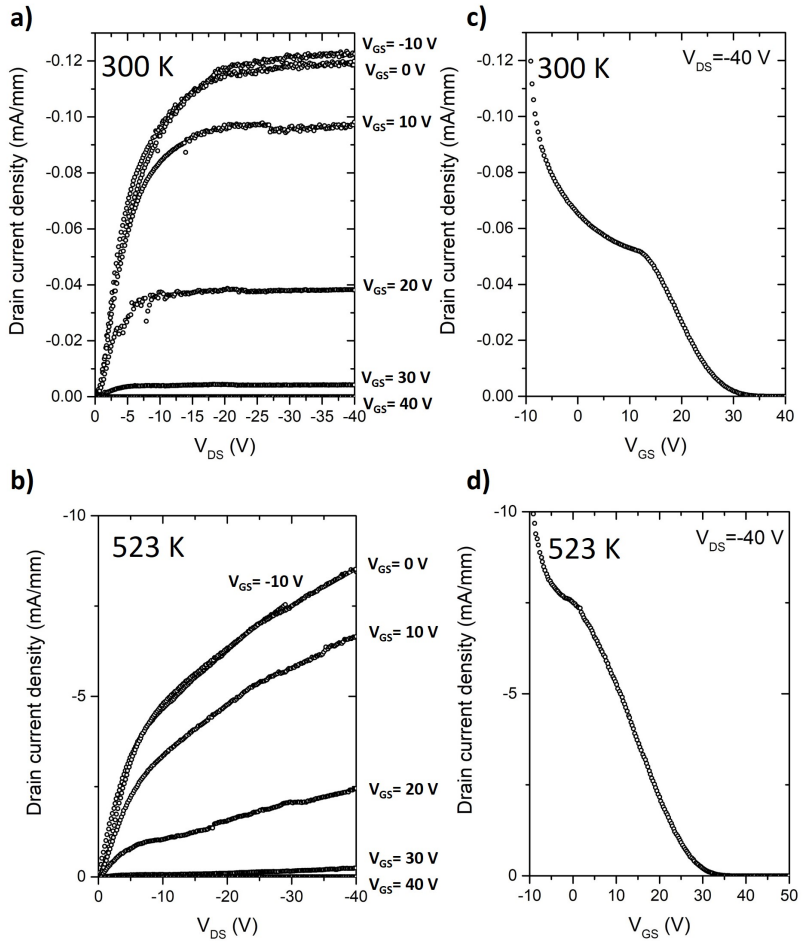

Figure 13. I_{DS} vs V_{DS} for V_{GS} from -10 V to +40 V with a 10 V step at a) room temperature and b) 523 K. Transfer characteristic I_{DS} vs V_{GS} at $V_{DS} = -40$ V at c) room temperature and d) 523 K. The configuration $V_{Sub} = V_{Source}$ is used and the measurement was performed under a white light 11 mW/cm^2 irradiance.

noticeable modification of the characteristics. No particular features could be identified between the first measurements, on the newly fabricated sample, and the ones months later.

Typical n-type Silicon and SiC inversion-mode MOSFETS have a body diode, which is coming from the structural bipolar PN junction between source (p-type) and drain (n-type). This body diode withstand the drain to source positive bias in off-state (Ist quadrant), when the MOSFET's inversion channel is not formed. Consequently to this PN body diode, such MOSFETs are not able to reach a off-state in the IIIrd quadrant, where a reverse current is flowing either through the forward biased PN junction or the inversion channel, or a combination of both, as a function of the gate to source biasing condition (above or below threshold). This can be clearly observed in SiC MOSFET [67], GaN HEMT [68] and other low voltage and high voltage silicon MOSFET.

The reverse conduction in the IIIrd quadrant is quite useful for power converters,

where MOSFETs can be used as freewheeling diodes [69]. However, the body diode typically has large on-state voltage drop, especially for low load current and close or lower than room temperature. Therefore, the channel conduction in preferred in the IIIrd quadrant, since it typically exhibits lower conduction losses than the intrinsic body diode. Using the reverse conduction of MOSFETs through the inversion channel has been extensively used in low voltage synchronous DC/DC converters ($\leq$ 48 V) with silicon MOSFETs, and is now considered for higher voltages with SiC MOSFETs (>400 V). However, there is a strong risk of "shoot through" in the power commutation cell, where both high side and low side power MOSFETS can be in on-state at the same time, leading to catastrophic failure. Hence, the body diode is used during the dead time.

For all these reasons, it is important to check the ability of the D3MOSFET to operate in reverse conduction (IIIrd quadrant), with a body-diode like behaviour, and the channel characteristics. Similarly to GaN n-type HEMTs which do not have any PN junction between drain and source, the p-type D3MOSFET can have a body-diode like characteristics. For the normally-on D3MOSFET in the dark or with a controlled substrate bias, so the back SCR is constant, the Ist quadrant is biased in off-state at $V_{GS} > V_{TH}$. A current can still flow in the IIIrd quadrant for $V_{DS} > V_{GS} - V_{TH}$, as the channel is opened. When increasing V_{DS}, the SCR reduces and the channel resistance decreases until it becomes negligible in comparison to the drift resistance. The IIIrd quadrant characteristics is shown in Fig. 14, the diode-like conduction is clearly measured. This constitutes the first demonstration of the IIIrd quadrant conduction in a bulk conduction FET.

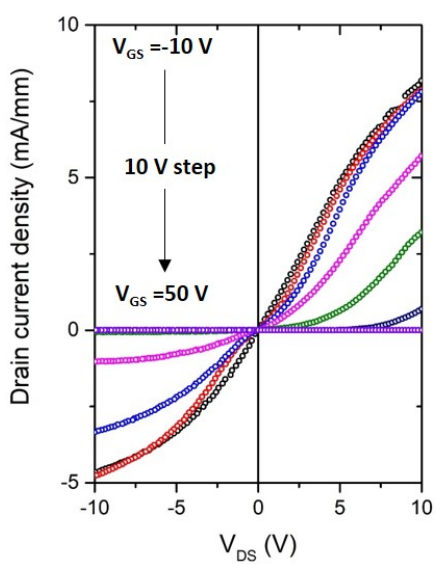

Figure 14. Ist and IIIrd quadrants characteristic of the D3MOSFET at 250 °C with a substrate bias $V_{Sub} = V_{Source}$.

However, for some other applications (matrix converters, multi-level converters, AC/AC converters) bidirectional power transistors are preferred. These devices have symmetrical Ist and IIIrd quadrants, e.g. there is no reverse conduction in off state (reverse blocking device) and both quadrants are conducting in on state (reverse conduction). An experimental demonstration of a bidirectional diamond power FET based on the D3MOSFET was recently published [70]. This device possesses only one drift region and two distinct gates, achieving low on state resistance compared to the use of two separate transistors.

4.3. Off-state blocking capabilities

4.3.1. Experimental I_{DS} versus V_{DS} in off-state The blocking voltage of the device is of particular importance for power devices and is a major advantage of wide and ultra wide band gap semiconductors over silicon. This is however a very challenging parameter to optimize, as the reduction of the electric field crowding effect requires specific architectures such as field plates in lateral devices. Due to the complexity of the fabrication process, the choice has been done to not to use them and thus a peak electric field is suspected to be present at the gate edge, in the oxide and at the oxide/diamond interface.

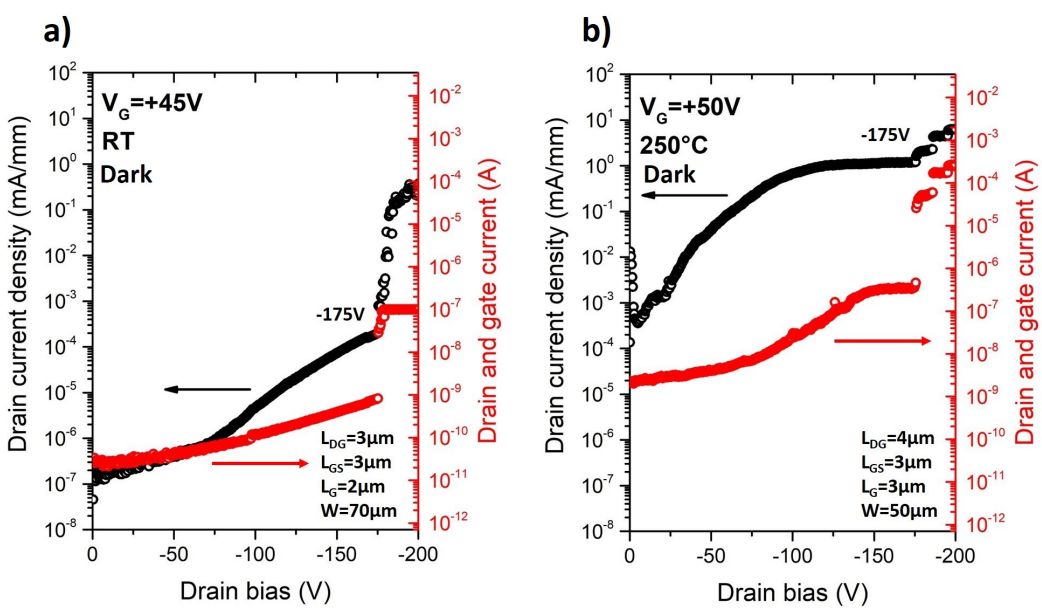

Figure 15. Breakdown characteristics of two different D3MOSFETs with a rectangular shape a) at room temperature and b) at 250 °C in the dark. Due to the destructive nature of the breakdown, the same transistor could not be measured several time with different conditions. The drain current density is plotted on left axis and the absolute value of the gate and drain current are plotted on right axis.

The highest drain to source breakdown voltage was measured to be $V_{BD} = -175$

V ($V_{DG,max} = -220$ V) at room temperature and $V_{BD} = -175$ V ($V_{DG,max} = -225$ V) at 250 °C in the dark, with the current-voltage characteristics shown in Fig. 15 a) and b). According to the model described in 3.1.2, this device would be able to withstand a 1 kV drain to source bias in off state, assuming no electric field crowding effect.

The strong increase of the gate current and the destructive nature of the breakdown indicate that it occurs in the oxide, as such the avalanche breakdown could not be observed in diamond and the gate is destroyed after the measurement. No modulation of the MOS stack is possible afterwards. At 250 °C, the control of the off-state is less efficient, with a gradual reopening of the channel. Nonetheless, the oxide induced breakdown voltage is clearly identified and these values are close to the one measured on MOS1 sample at $V_{BD} = -200$ V ($V_{DG,max} = -212$ V) for the same doping level value.

Improving the blocking characteristic would require specific architectures to reduce the electric field crowding in the oxide, which was not the focus of this work. Due to the nature of the breakdown, the V_{BD} value is dependent on local defects in the oxide, or gate metal lithography imperfections, and thus dispersed between −50 V and −175 V. No correlation was found between L_{DG}, L_G and V_{BD}, in contrast to MESFETs [71] and H-terminated MOSFETs [21], due to the relatively high doping level used here. The electric field in the drift region never extends further than L_{GD}.

4.3.2. Simulation of the maximum electric field In spite of the relatively low breakdown voltage demonstrated here in comparison to other diamond FETs, the maximum electric field in the structure is still high, due to the relatively elevated doping level of the p-type layer. Estimations of this peak electric field value at breakdown voltage had been performed using a 2D finite element simulation tool (SILVACO) (Fig. 16 a)), and compared with a simple 1D analytical model (Fig. 16 c)). The later is evaluated to give an underestimation of the peak electric field as it omits to take into account edge effects. The physical models discussed in this paper have been implemented in the software except for the diamond avalanche effect which is not considered here, as the breakdown occurs prematurely. This simulation relies on solving the Poisson equation in the quasi-static case for each point of a defined grid. It has been performed assuming no fixed or mobile charges in the oxide, or at the diamond/oxide interface, and the substrate is treated as an insulator which is valid in the case of the room temperature measurement in the dark. Implementing these additional effects has been tried, but optimizing the software parameters to an ultra wide band gap material was found to be particularly challenging and the simulation did not converge.

Fig. 16 b) shows the electric field extracted from 2D simulation at the oxide top surface where it is maximum. A peak electric field value of 6.3 MV/cm at breakdown is obtained, in good agreement with the experimental values measured in MIMCap fabricated on the same sample, shown in Fig. 17 b). A simplified structure schematized in Fig. 17 a) with no oxide/diamond interfaces has been used to only probe the alumina layer. The 4 measured MIMCaps exhibit breakdown fields between 5.7 MV/cm and 6.3 MV/cm assuming a constant electric field in the oxide, with a reproducible leakage

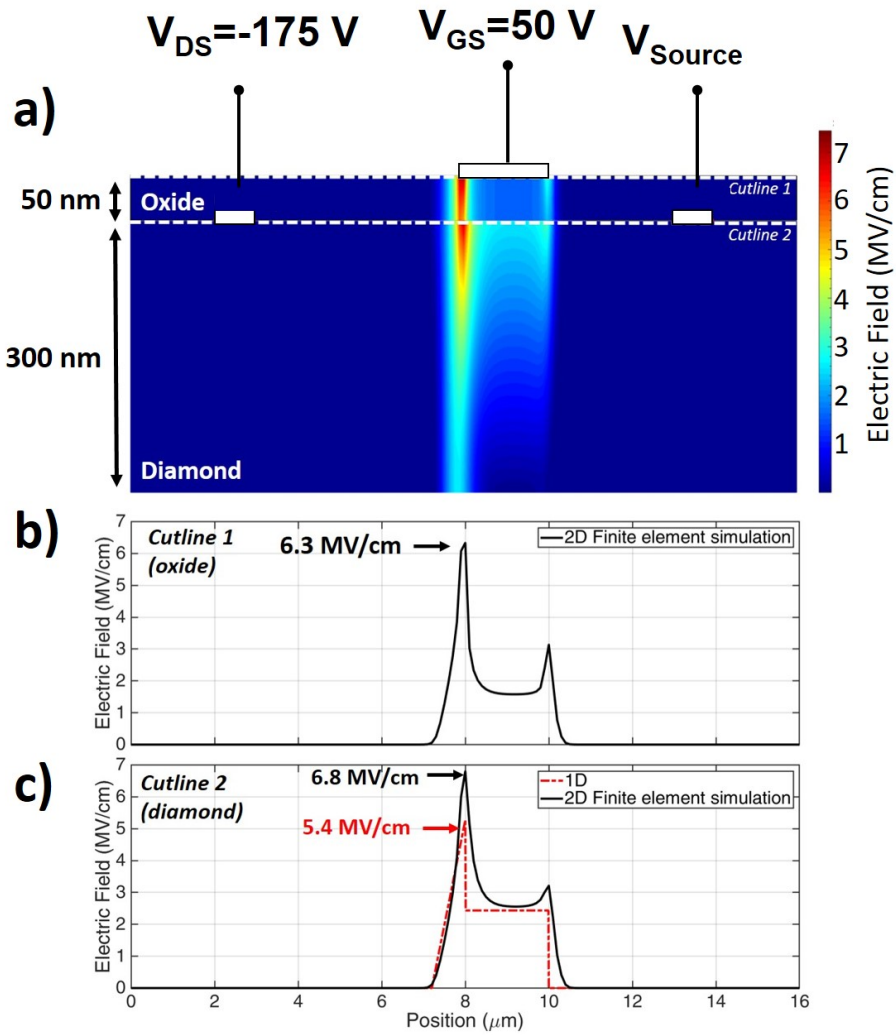

Figure 16. a) Finite element simulation of the electric field distribution in off-state with a drain bias of -175 V and a gate bias of +50 V. Without a specific field plate edge termination, the electric field crowding effect causes a very high electric field peak under the gate, which reduces the maximum voltage breakdown capability. The lateral electric field profiles on b) the oxide surface and c) the top surface of diamond are extracted from the simulation (black) and calculated using 1D electrostatic analysis (red).

current at first measurement. Successive measurements on the same MIMCap at high field tends to degrade the alumina layer and the leakage can increase by few orders of magnitude. A maximum electric field of 6.8 MV/cm is calculated in diamond, which is amongst the highest reported in diamond FETs. Yet, it is not enough to observe the avalanche breakdown in diamond. Estimation based on impact ionization rates reported by Hiraiwa et al. [36] suggests that the critical field is about 10 MV/cm, leading to an ideal breakdown voltage of 1 kV by neglecting the edge effects. As for any other semiconductors power devices, improving the breakdown voltage requires the use

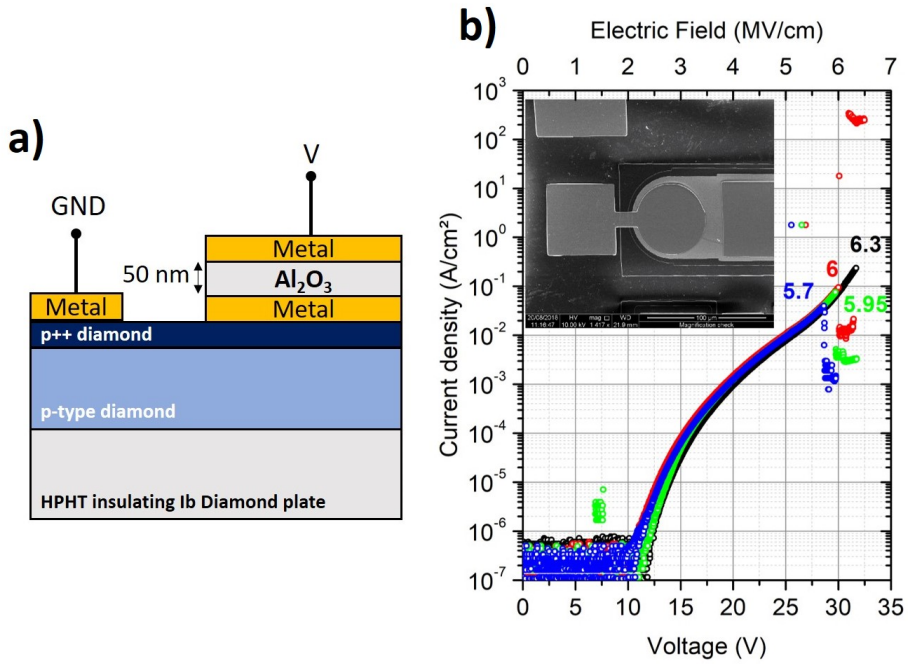

Figure 17. a) Schematic cross section of the MIMCaps. b) Current-voltage breakdown characteristic at room temperature of 4 MIMCaps, exhibiting a high destructive breakdown field between 5.7 MV/cm and 6.3 MV/cm.

of specific features such as field plate to reduce edge effects, as discussed previously.

5. Summary and perspectives

The deep depletion regime has been evaluated to be a steady state in wide band gap semiconductors, allowing to use it in a depletion MOSFET design with a thick channel layer. Based on the physics of the MOS capacitors, the expected performances in terms of conductivity and blocking voltage capabilities of the simplest lateral design have been deduced, as well as the predicted transistor characteristic, thanks to the existing literature providing most of the needed models and parameters. Given the inherent difficulty of processing small sized diamond samples, the lateral architecture is preferred over a vertical design, limiting the number of technological steps. Some more advanced designs are however shown to achieve in principle higher performances and bring this deep depletion MOSFET concept toward the best it can achieve, yet needing more development in process fabrication and diamond growth control. The discussion developed in this paper assumed an ideal MOS, i.e. no parasitic charges are present in the device and only 1D equations are used. The 2D geometry effects have a dramatic impact on the device's performance, as edges are not considered in the model used here. These considerations are difficult to predict and are intrinsically tied to the fabrication process.

The successful operation of the D3MOSFET with diamond selective growth and

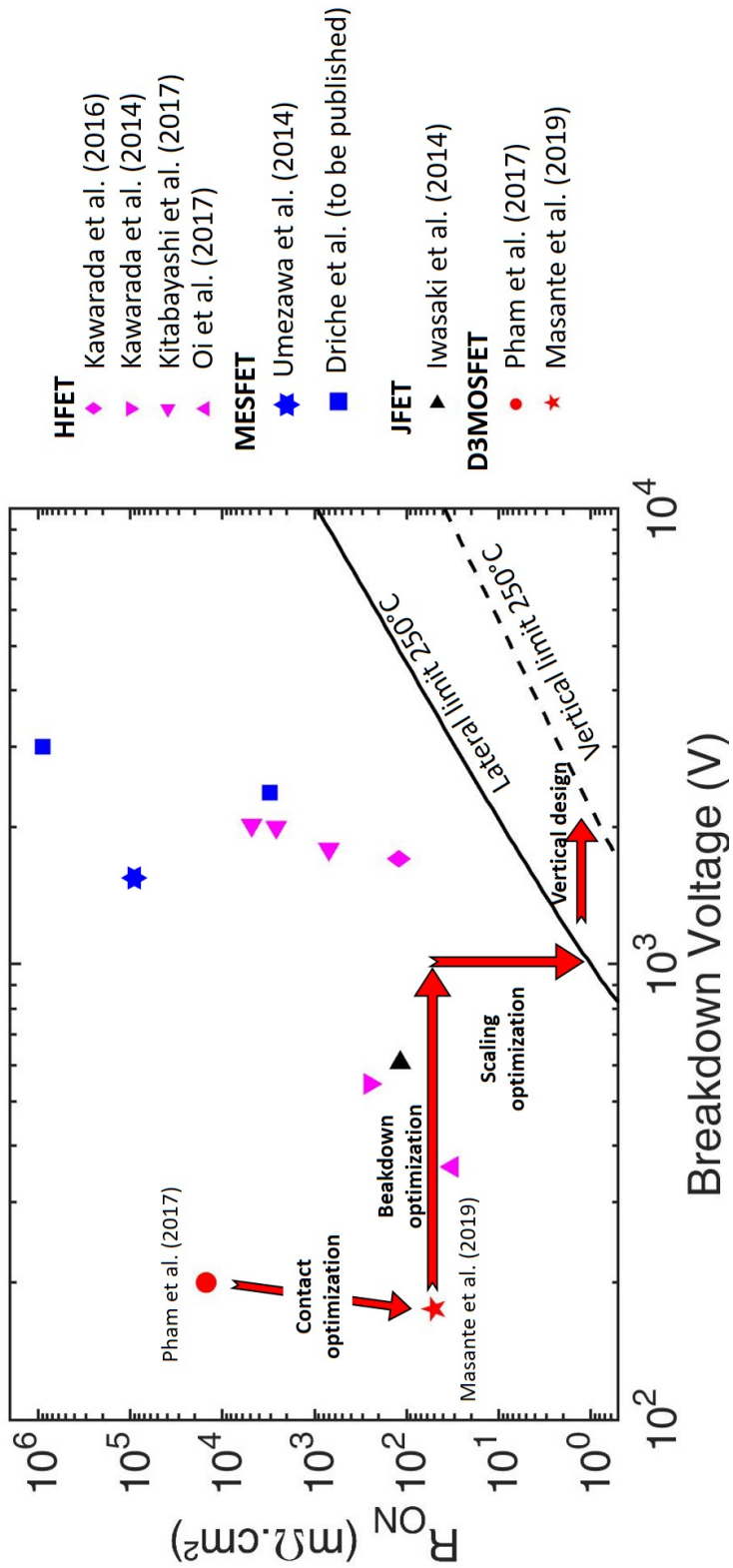

Figure 18. $R_{ON,S}$ vs V_{BD} performances of reported power diamond FETs in the literature, compared to the expected performances of the optimized lateral and vertical design of the D3MOSFET at 250 °C. Improvements from the previous work of T. T. Pham et al. thanks to the contacts optimization is shown, along further performance gains that can be achieved with an improved sizing, electric field crowding management and a change to the vertical design. Experimental points are taken from ref. [21, 40, 65, 66, 71, 72, 42, 43].

mesa etching has been achieved. The transistor characteristics of the fabricated D3MOSFETs have been measured in the Ist and IIIrd, from room temperature to 250 °C, exhibiting a transistor effect. The lowest specific on-state resistance was measured at $R_{ON,S} = 50$ mΩ.cm^2 at 250 °C [43] while ensuring an off-state. The maximum breakdown voltage was measured to be $V_{BD} = -175$ V [43], corresponding to a peak electric field superior to 5.4 MV/cm (estimated at 6.8 MV/cm by 2D finite element simulation) in the diamond. The breakdown most probably occurred in the oxide layer due to its lower breakdown field, measured to be 6.3 MV/cm without considering edge effects, and the lack of edge termination features. Nonetheless, this value is much larger than in silicon (0.2 to 0.8 MV/cm), SiC and GaN (≈ 3 MV/cm). Thanks to gate oxide control, in most of the devices tested the gate leakage current remained below 1 nA/mm at room temperature and in the order of 10 nA/mm at 250 °C. Large variations from one device to an other are however observed, with values that can vary by several orders of magnitude due to local defects in the oxide.

The performances of the D3MOSFET were compared to the other demonstrated diamond power FETs in terms of the R_{ON} vs V_{BD} trade-off in Fig. 18. All of these devices have a lateral design, due to the constraints of the fabrication process or due to the use of a 2D hole gas as channel. The estimated optimal performances of the lateral and vertical design are based on the 1D models of the first part with a 50 nm oxide layer and a threshold voltage $V_{TH} = 15$ V. It has been assumed that the drift layer resistance is much higher than the channel resistance and that $L_{SD} \approx L_{GD}$. For the vertical design, only the bulk conduction is considered and the R_{ON} could be further decreased by operating it in enhancement mode. As it can been seen, all shown devices require optimizations to fully take advantage of the diamond capabilities. The next key step toward demonstrating outstanding performances is a better electric field crowding effect management by the use of edge terminations. Indeed, its detrimental effect is evidenced by the measured D3MOSFET breakdown at 175 V, more than a factor 5 below the calculated 1D diamond breakdown of 1 kV. On the longer term, the vertical design is well known to be more suited than the lateral one to reduce the electric field crowding. The maximum current per chip surface area is also much higher than in the lateral design.

Aside from design improvements, the high thermal conductivity of diamond and its effect in terms of device performance should be more deeply studied. It is one of the most significant advantage comparatively to other semiconductors: diamond in its various forms (monocrystalline, polycrystalline or nano particles, as a bulk material, coating material or in composites) has been proposed for the last decades as an efficient heat spreader which can reduce the total thermal resistances of electronic devices and their packaging[73, 74, 75, 76, 77, 78, 79]. Consequently, higher total current levels are allowed for the same maximum device junction temperature[80, 81], or lower device temperatures under the same operating conditions. At the device level, moving from Silicon or other WBG materials to diamond will offer a better heat spreading at the closest of heat generation sources (i.e. the channel and drift regions in each elementary

transistor cell), with a reduction of hot spots, lower temperatures and a more uniform temperature profile, accordingly to Fourier's law. As an example, a study similar to [82] must be conducted with diamond devices, to solve the conduction heat transfer in 3D, associated with realistic diamond device architectures and physical parameters. Another solution to maximize the heat exchange at the closest to the heat sources of electronic devices is to create micro cooled channels in the active region of the semiconducting device[83], which can be seen as more complex technologies than diamond to reach lower total thermal resistances.

Moreover, diamond FETs based on a bulk diamond current conduction such as the D3MOSFET have the peculiar behavior of a Negative Temperature Coefficient (NTC) for the ON-state resistance (in the linear/ohmic regime). This specificity adds paralleling issues (hot spots, unevenly current sharing) and thermal instability[84, 85]. Hence, paralleling diamond transistors at the power module level can lead to a large current imbalance between paralleled devices when dispersions or poor thermal coupling of paralleled diamond devices are considered[86, 87]. However, this should be mitigated when paralleling FET cells on the same diamond die, due to its large thermal conductivity and a high thermal coupling between elementary transistors. Nonetheless, a careful design must be done for the next-to-be-developed diamond power modules, similarly to Si, GaN, SiC modules[88, 89, 90, 91] but with the physical parameters of diamond devices such as the NTC behavior.

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