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New monolithic multi-terminal Si-chips integrating a power converter phase-leg for specific applications

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Abstract— The paper deals with the monolithic integration of a power converter phase leg. It focuses on the integration of a power phase leg consisting of a VDMOS and an IGBT. This association is suitable for monolithic power integration in silicon. Different monolithic chips integrating phase legs were proposed and discussed in this paper. Interesting advantages can be brought by the monolithic integration of the converter phase leg. These advantages include power chips realization simplification, control of gate transistors with respect to constant voltages (DC-link or ground-0V).

Keywords—P-IGBT; N-VDMOS; monolithic integration; power conversion; switching cells.

I. INTRODUCTION

Currently commercialized conventional power modules are generally realized using 2D hybrid packaging technology in which two-terminal power dies such as IGBT and PiN-diode are soldered on their backside and interconnected using wire bonds. A power module is made of a great number of two-terminal dies that are interconnected by wire bonds. Power modules are therefore bulky and their mass fabrication is limited in productivity. Wire bonds require an expensive wiring operation and are a source of reliability problems [1]-[3]. Moreover, they are a source of stray inductance [4] that limits the operation frequency of the power modules.

In order to overcome these shortcomings, a significant breakthrough can be achieved by an optimized mixed hybrid/monolithic integration of the multi-phase power converters. Different monolithic integration approaches were proposed in literature [5][6]. However, they are either limited in performance due to lateral integration with vertical insulation trenches through the die [5] or require a complex technological process for their realization due to molecular bonding of two silicon wafers [6]. Within the same context, the authors have proposed a vertical quasi-monolithic integration of a multiphase converter called dual-chip approach as well as an ultra-compact single chip approach [7]. From the technology process realization point of view, the proposed multi-terminal chips require the realization of through silicon deep trenches and therefore their realization is complex.

For power conversion applications, the use of P-type power devices is very rare as compared to N-type power devices. This

is mainly due to the poor on-state characteristics of P-type power devices as compared to their N-type counterparts. However, the association of P-type and N-type transistors, for specific applications, can make easier the monolithic integration in one chip of the phase leg.

In this paper, new multi-terminal power chips were proposed for monolithic phase leg integration. The integrated phase legs are illustrated in Figure 1. The converter of Figure 1.a is a current reversible DC/DC buck converter while the converter of Figure 1.b is a current reversible DC/DC boost. In the case of Figure 1.a, the phase leg consists of a high side P-IGBT and a low side N-VDMOS. In the case of Figure 1.b, the phase leg consists of a high side N-VDMOS and a low side P-IGBT. In this paper, only on the buck configuration (Figure 1.a) was studied..

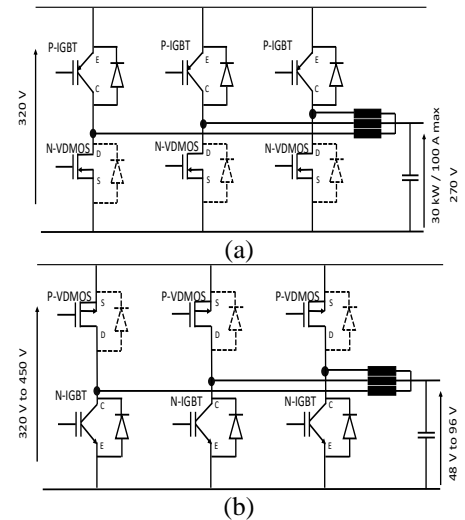


Figure 1 : Converter leg typical applications for the DC/DC buck converter (a) and the DC/DC boost converter (b)

The converters components are placed (high-side or low-side) according to their type (unipolar or bipolar), so that the power losses would be always minimum for a given duty cycle. More specifically, the configurations exploit the conductivity modulation principle of bipolar components to reduce the power losses. For instance, for a 0.8 duty cycle, in order to optimize the power losses in the buck configuration (Figure

1.a), the bipolar transistor will be conducting 80 % of the time and the N-VDMOS the complement (20 %). The same principle applies for the boost configuration (Figure 1.b). This time, in order to reduce the power losses, a 0.2 duty cycle will be affected to the high-side unipolar transistor (P-VDMOS), while the low-side N-IGBT will be conducting 80 % of the time.

The monolithic architectures and the operating modes of the multi-terminal chips were validated through mixed-mode Sentaurus™ 2D-numerical simulations.

II. PRINCIPLE OF THE APPROACH

The 2D cross sectional views of a P-IGBT, N-IGBT, P-VDMOS and N-VDMOS are summarized in Figure 2. In the proposed buck converter topology (Figure 1.a), one can notice that the N^+ back-side region is the same in the high side P-IGBT and in the low-side N-VDMOS. By mutualizing this backside N^+ regions, the monolithic chip of Figure 3.a is proposed. It consists of a vertical N-VDMOS and a vertical P-IGBT separated by deep but not through silicon trenches [7]. This latter can be filled by an insulator [8]-[9].

The same principle applies for the proposed boost converter topology (Figure 1.b). Noticing the same P^+ backside regions for the high side P-VDMOS and the low side N-IGBT, these could be associated. By mutualizing this backside P^+ regions, the monolithic chip of Figure 3.b is proposed. It consists of a vertical P-VDMOS and a vertical N-IGBT separated by deep but not through silicon trenches that can be filled by an insulator.

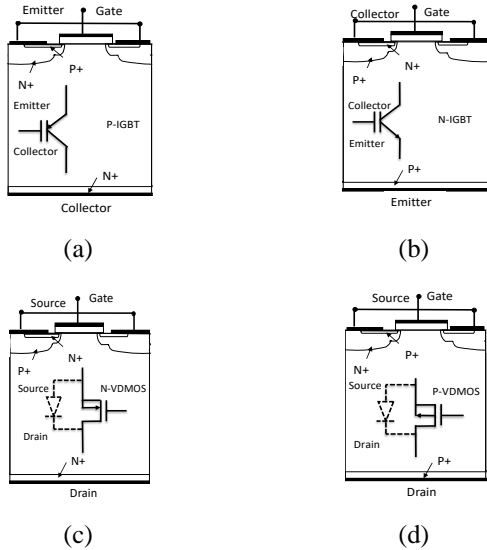


Figure 2 : P-IGBT (a), N-IGBT (b), P-VDMOS (c) and N-VDMOS (d) topologies.

III. CHIPS DESIGN

For the sake of illustration, the monolithic chip integrating a phase leg of Figure 4 is designed to support a blocking voltage of 100 V and carry out a nominal current of 48A. The chosen rated voltage (100 V) is a design example. Designs at higher

voltages are possible by following the procedure described here after.

The design starts first by estimating the drift regions doping concentration and thickness of each device separately (P-IGBT and N-VDMOS) that allow to withstand the rated (100 V) voltage. The on-state static I(V) characteristics of each device is used to determine the on-state current density J_{VDMOS} and J_{IGBT} and voltage drop that limits power losses to 50 W.cm⁻².

Assuming a monolithic chip area of 1cm², and knowing each transistor's current density, the total rated current I_{tot} is determined using equation (1).

$$I_{tot} = \frac{S_{tot}}{\frac{1-\alpha}{J_{VDMOS}} + \frac{\alpha}{J_{IGBT}}} \quad (1)$$

Where α represents the duty cycle, S_{tot} the chip surface (1 cm²) and J_{VDMOS} , J_{IGBT} the N-VDMOS and P-IGBT current densities. Once the rated current is determined, each transistor occupied surface is then calculated using (2) and (3).

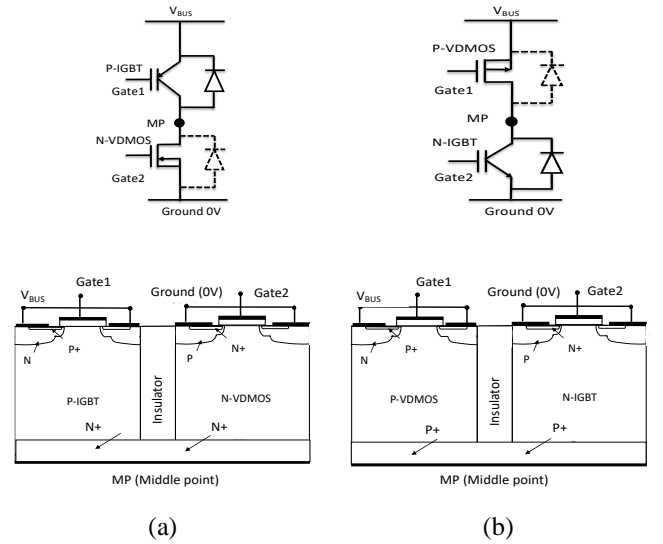


Figure 3 : Cross-sectional view of the proposed monolithic chip integrating the phase leg P-IGBT (high side) and N-VDMOS (low side) (a), N-IGBT (low side) and P-VDMOS (high side) (b).

$$J_{VDMOS} \times S_{VDMOS} = I_{tot} (1-\alpha) \quad (2)$$

$$J_{IGBT} \times S_{IGBT} = I_{tot} (\alpha) \quad (3)$$

As a design application, Figure 4 shows a P-IGBT and N-VDMOS monolithic structure integration, where a 0.8 duty cycle (α) is used. The 2D mixed mode simulation of the monolithically integrated structure requires the use of the same components depth (area factor). Consequently, four IGBT cells and one VDMOS cell are used to reach the required devices areas at the designed rated current density, with respect to power losses constraint. This monolithic integration increases the on-state voltage of the N-VDMOS due to the required P-IGBT thickness to support the applied voltage (100 V),.

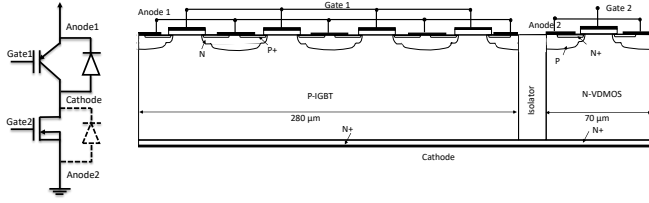
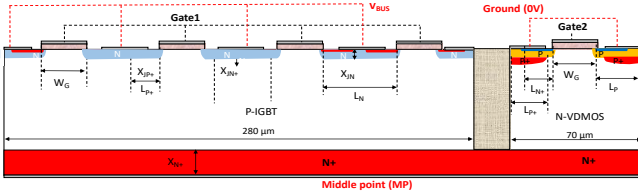


Figure 4 : Designed P-IGBT and N-VDMOS phase leg with duty cycle 0.8, 100 V bus voltage and 48A rated current

IV. SENTAUROS™ MIXED-MODE SIMULATIONS RESULTS

The main physical and geometrical parameters of the diffused regions used in the IGBT and VDMOS sections are those set by the IGBT process-flow of the micro and nanotechnology platform at LAAS-CNRS (Table 1). The drift regions thickness and concentration are chosen so the devices are able to withstand 100 V. The simulation conditions correspond to a static state, when one diagonal section of the half H-bridge is in on-state, the other is in off-state. A current source of 48 A simulates an inductive load. Both presented architectures (Figure 3) are simulated using the circuits configurations shown in Figure 5.

Table 1 :Main Physical and geometrical parameters of the LAAS-CNRS IGBT-Technology process [10].



Symbol	Parameter	Value	Doping concentration
W_G	Gate width	30 μm	
e_{ox}	Gate oxide thickness	55 μm	
$L_{N(P)}$	N diffusion width	40 μm	$2.5 \times 10^{17} \text{cm}^{-3}$
$X_{JN(P)}$	N diffusion depth	5 μm	
$L_{N+(P+)}$	N diffusion width	26 μm	$5 \times 10^{19} \text{cm}^{-3}$
$X_{JN+(P+)}$	N diffusion depth	7 μm	
$L_{P+(N+)}$	P diffusion width	14 μm	10^{20}cm^{-3}
$X_{JP+(N+)}$	P diffusion depth	1 μm	

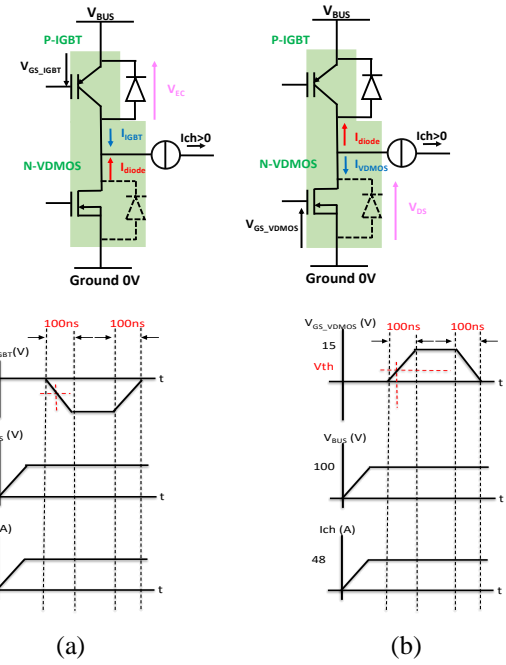
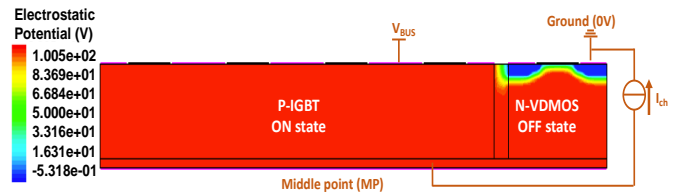


Figure 5 : Simulated architectures and control signals used for simulations.

Mixed-mode 2D simulations using Sentaurus™ were carried out to validate the architecture in boost converter circuit. The results of the simulated structure under short switching time (100 ns) are presented below.

A. P-IGBT switching

Figure 6 and Figure 7 show simulation results on the P-IGBT conduction and blocking capabilities. During P-IGBT conduction (Figure 6.a and Figure 6.b), N-VDMOS reverse biased junction P/N- supports the applied voltage. When the P-IGBT's threshold voltage is reached through V_{GS_IGBT} (green curve) increasing voltage, its current starts to increase (Figure 7.a), until the forward recovery phenomenon is completed. Subsequently, the voltage across the component (V_{EC} , purple curve) decreases to reach the on-state drop voltage (0.91 V). During this time, the voltage across the N-VDMOS increases to withstand the DC-bus voltage.



(a) equipotential lines distribution in the multiterminal chip

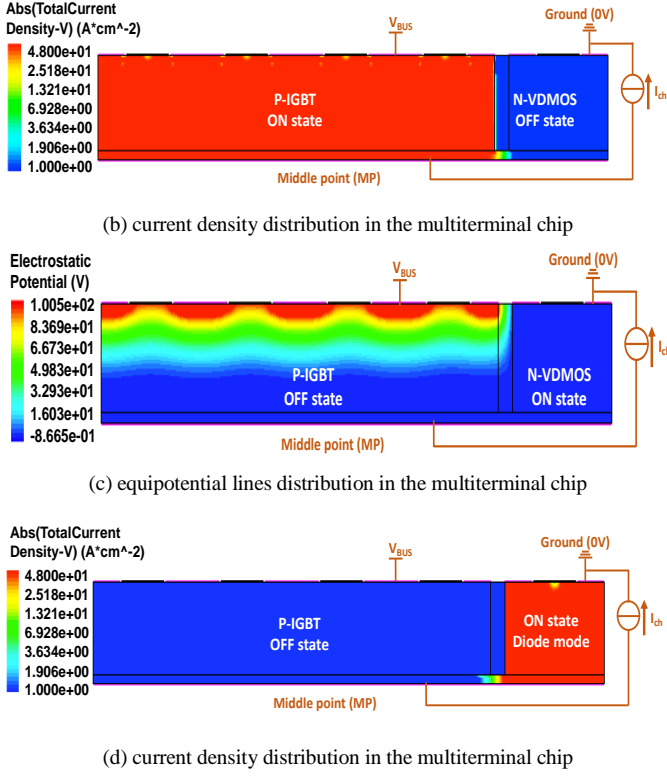


Figure 6: Equipotential lines distribution and current density distribution in the multi-terminal chip: P-IGBT on-state and NVDMOS in off-state (Leakage current: 0.2 μ A) (a-b); and NVDMOS on-state and P-IGBT in off-state (Leakage current: 94 μ A) (c-d).

The P-IGBT turn-off phase (Figure 7.b) begins with a voltage switching across the component (V_{EC} , purple curve), to reach to DC-bus voltage where the component withstands the rated voltage (100 V) thanks to the reverse biased N/P- junction (Figure 6.c). Then, the P-IGBT current decreases to zero. Simultaneously, the current through the N-VDMOS increases, meaning the component's body diode is in on-state (Figure 6.d).

B. N-VDMOS switching

During N-VDMOS conduction (Figure 9.a), the P-IGBT reverse biased junction N/P- withstands the DC-bus (Figure 8.a) voltage. Once the threshold voltage is reached, the current starts to increase in the VDMOS structure, until the forward recovery phenomenon is complete (Figure 8.b). Then voltage across the drain source (V_{DS}) decreases to reach an on-state voltage of 2.1 V. At the same time, the P-IGBT anti-parallel freewheeling diode voltage increases and supports the applied DC-bus voltage.

Once the N-VDMOS turn-off phase begins (Figure 9.b), the voltage across drain source rises (V_{DS}), until the reverse recovery phenomenon is complete. When the component turn-off is completed, the freewheeling diode is in on-state, where the VDMOS supports the DC-bus voltage (Figure 8.c).

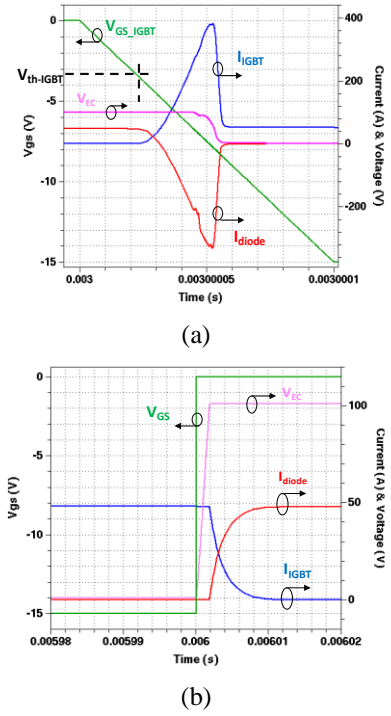


Figure 7 :P-IGBT turn-on (a) and turn-off (b) switching waveforms.

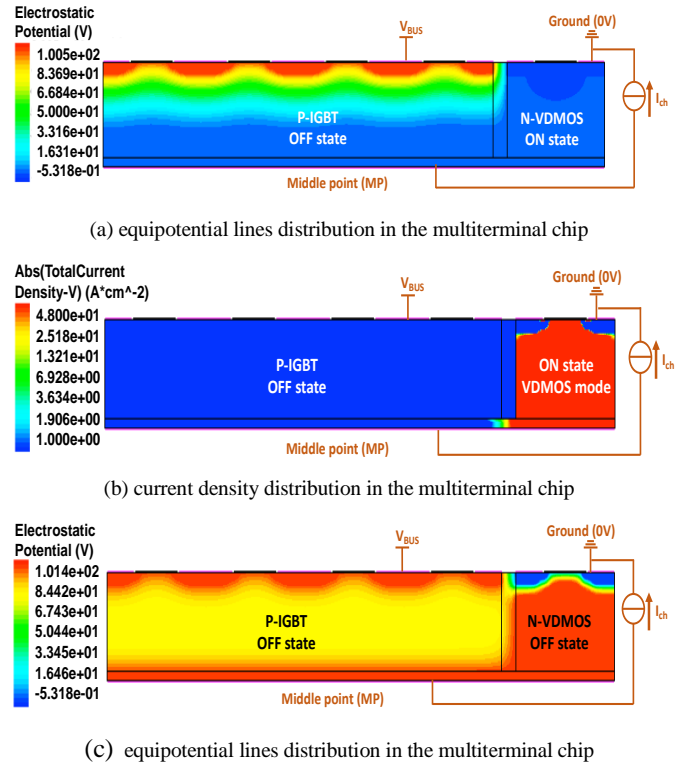


Figure 8 :Equipotential lines distribution and current density distribution in the multi-terminal chip: NVDMOS on-state and P-IGBT in off-state (Leakage current: 0.3 μ A) (a-b); and P-IGBT freewheeling diode on-state and NVDMOS in off-state (Leakage current: 0.2 μ A) (c).

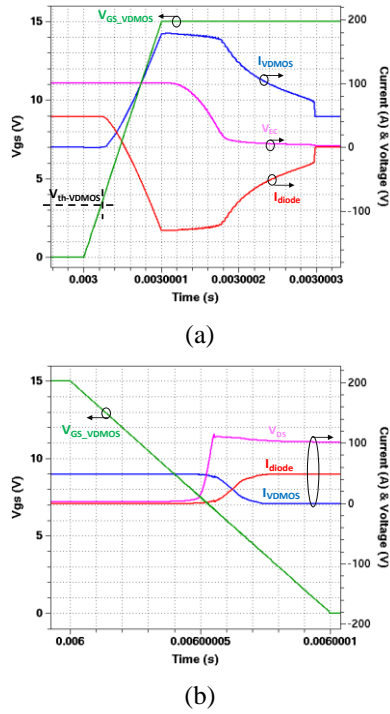
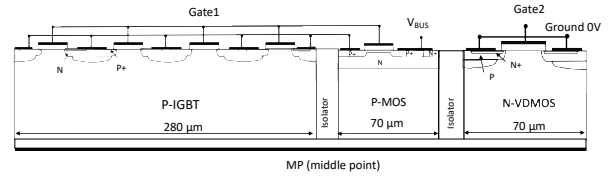
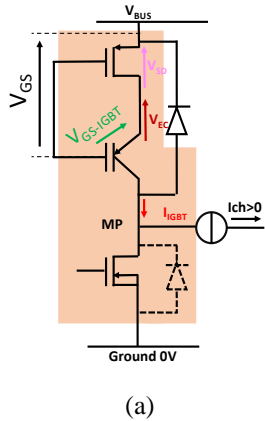


Figure 9: N-VDMOS turn-on (a) and turn-off (b) switching waveforms.

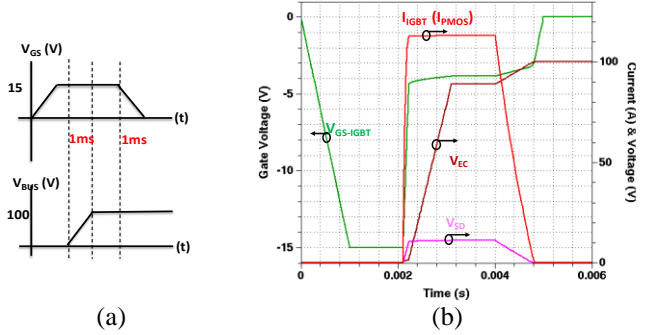
C. P-IGBT current limitation

To limit the P-IGBT current under short circuit occurrence, a low voltage depletion mode P-channel-MOS transistor is added in series with the vertical P-IGBT as shown in Figure 10. This transistor limits the current through the P-IGBT and provides P-IGBT's gate-depolarization, its desaturation current limitation and then prevents the component's latch-up under short-circuit conditions. Sentaurus™ simulation results illustrate the impact of the addition of the P-MOS transistor on the I(V) characteristics of the high-side part of the phase leg.



(b)

Figure 10 : Improved P-IGBT structure against latch-up phenomena during short-circuit using a depletion mode P-MOS transistor



(a)

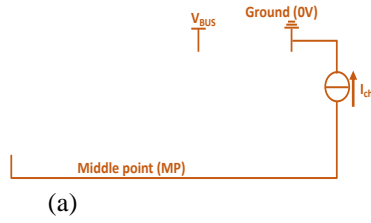
(b)

Figure 11: A combined P-IGBT/P-MOS structure switching waveforms obtained using mixed mode simulation in a short-circuit case.

When the short-circuit is initiated (Figure 11, green zone), both current and voltages across the transistors rise until saturation of the P-MOS is reached, according to the designed saturation current of the P-MOS. During the short-circuit (Figure 11, orange zone), the components support the DC-bus voltage ($V_{BUS}=100$ V). The IGBT withstands 90 V and the P-MOS supports the difference. The on-state voltage drop across the P-MOS increases, which leads to a decrease in the P-IGBT gate-emitter voltage ($V_{GS-IGBT}$, green curve). As a result, the current through the P-IGBT is maintained at the P-MOS saturation current (~ 115 A), which is lower than latch-up current and higher than rated current (48 A). When the transistors gates control signal (V_{GS}) is decreased to zero (Figure 11, blue zone), the current through the components decreases. Once the transistors switch off, the P-IGBT supports the DC-bus voltage (100 V). Equipotential and current density lines distribution in the integrated monolithic structure comprising the three components (IGBT, VDMOS and P-MOS) during IGBT on-state are shown in Figure 12. During IGBT conduction (Figure 12.a), the VDMOS reverse biased junction P⁺/N⁻ withstands (Figure 12.b) the DC bus voltage (100 V). The IGBT on-state voltage drop remains the same (0,91 V).

Abs(TotalCurrent
Density-V) (A*cm⁻²)

4.800e+01
2.518e+01
1.321e+01
6.928e+00
3.634e+00
1.906e+00
1.000e+00



Electrostatic
Potential (V)

1.000e+02
8.350e+01
6.700e+01
5.050e+01
3.400e+01
1.750e+01
1.000e+00

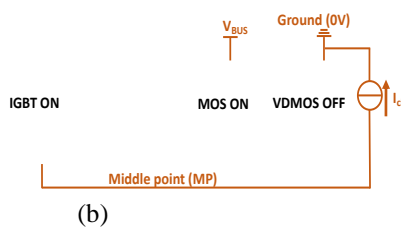


Figure 12 : Current density distribution (a) and equipotential lines distribution (b) in the multi-terminal chip: P-IGBT & P-MOS on-state and N-VDMOS in off-state.

V. CONCLUSION

In this paper, original monolithic chips integrating converter phase legs were proposed. From the technology process realization point of view, these multi-terminal chips do not require the realization of through silicon deep trenches [6] and therefore their realization is not complex. The operating modes of the chips were validated in a buck converter application using 2D Sentaurus™ mixed-mode simulations. The design approaches were illustrated and validated in an a 100V, 48A application. An improved version of the multi-terminal chip was proposed. It uses a depletion mode P-MOS transistor in series with the P-IGBT in order to limit the current through this latter mainly in the case of a short-circuit condition and therefore prevents P-IGBT latch-up.

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