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# InAs/Al<sub>0.4</sub>Ga<sub>0.6</sub>Sb side gated vertical TFET on GaAs substrate

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**Abstract**— We report on the fabrication of a side gated vertical tunnel field effect transistor (TFET) with a 570  $\mu\text{A}/\mu\text{m}$  ON current at  $V_{\text{ds}}=V_{\text{gs}}=0.5$  V. The device is based on a near broken gap AlGaSb/InAs heterostructure grown on a GaAs substrate thanks to a GaSb accommodation layer. The electrostatic control of the 80 nm InAs channel is obtained by lateral side gates. The trade-off between mesa width and ON/OFF ratio is evidenced.

**Keywords**—TFET; AlGaSb/InAs; near broken gap;

## I. INTRODUCTION

The Tunnel field effect transistors (TFETs) have been recognized as a potential candidate to replace complementary metal oxide field effect transistors (CMOS) for ultra-low power logic applications. Among various architectural configurations [1-3], vertical TFETs with side gated architecture is attractive to effectively control the tunnel current in the channel because of good gate electrostatics. III-V based AlGaSb/InAs is a promising system for TFET logic application to achieve high ON current densities at a very low supply voltage due to the low effective mass of carriers and small tunneling barrier width [4]. In this work, a top-down approach is proposed to fabricate a side gated tunnel FET device based on an InAs/Al<sub>0.4</sub>Ga<sub>0.6</sub>Sb heterojunction grown on a GaAs substrate.

## II. FABRICATION & CHARACTERIZATION

The proposed material system is grown using molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. The epitaxial layers comprised of 600 nm p+ GaSb layer ( $\text{Si} \sim 1 \times 10^{19} \text{ cm}^{-3}$ ), 50 nm p+ Al<sub>0.4</sub>Ga<sub>0.6</sub>Sb ( $\text{Si} \sim 1 \times 10^{19} \text{ cm}^{-3}$ ) followed by 80 nm InAs (i) and 50 nm n+ InAs ( $\text{Si} \sim 1 \times 10^{19} \text{ cm}^{-3}$ ) respectively. The type-II (highly staggered) heterojunction is formed at the interface between p+ Al<sub>0.4</sub>Ga<sub>0.6</sub>Sb and InAs.

Devices are fabricated using a self-aligned E-beam lithography process. Drain electrodes from  $2 \times 0.25 \mu\text{m}^2$  to  $2 \times 1 \mu\text{m}^2$  oriented in the two crystallographic orientations of the substrate are first defined. These contacts are used as a mask for the anisotropic and selective wet etching of the InAs layer with respect to AlGaSb. After a dilute HCl treatment, a 4 nm thick alumina oxide is deposited by Atomic Layer Deposition (ALD) followed by a self-aligned evaporation of gate metal. Contacts to the source and device isolation are performed after dry etching of alumina and buffer layer down to the GaAs substrate. Finally, air bridges are formed to contact drain, gate and source to large pads for characterization. Figure 1 shows SEM and FIB-STEM cross sectional images of the fabricated side gated vertical TFET with a  $2 \times 0.25 \mu\text{m}$  drain contact. The different profiles of the devices oriented in [1-10] and [110] direction are due to anisotropic wet etching and result in different width at the InAs/AlGaSb junction. For the smallest device, this leads to a width of 40 nm and 250 nm for the [1-10] and [110] orientation respectively. The current-voltage (I-V) output characteristics of the two devices measured at room temperature are shown in figure 2 & figure 3. In both cases, a negative differential resistance in reverse bias characteristic of a band-to-band tunnel injection mechanism is observed. As can be seen on the  $I_{\text{DS}}-V_{\text{DS}}$  forward characteristics, the gate command efficiency is clearly improved with the reduction of the mesa width. This behavior has also been evidenced by comparing devices oriented in the same direction but with different drain contact width.

For the smallest device of figure 1.c, a 570  $\mu\text{A}/\mu\text{m}$  ON current is measured at  $V_{\text{ds}}=V_{\text{gs}}=0.5$  V. Although further reduction of the mesa width together with an improvement of the InAs/oxide interface quality is required to completely pinch-off the device, this result is very promising for the realization of an efficient TFET with a large ON current.

## REFERENCES

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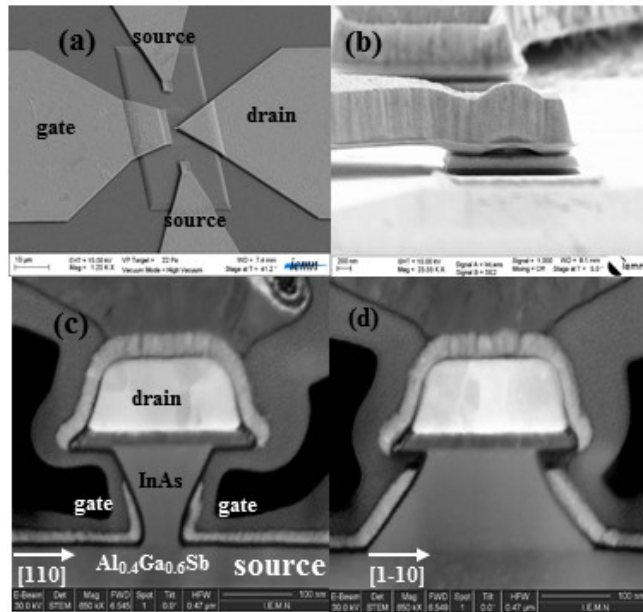


Figure 1. – SEM images of the fabricated TFETs: (a) large view showing the configuration of the vertical TFET, (b) zoom on the air-bridge drain contact, FIB-STEM images on the smallest devices oriented in [1-10] (c) and [110] direction (d).

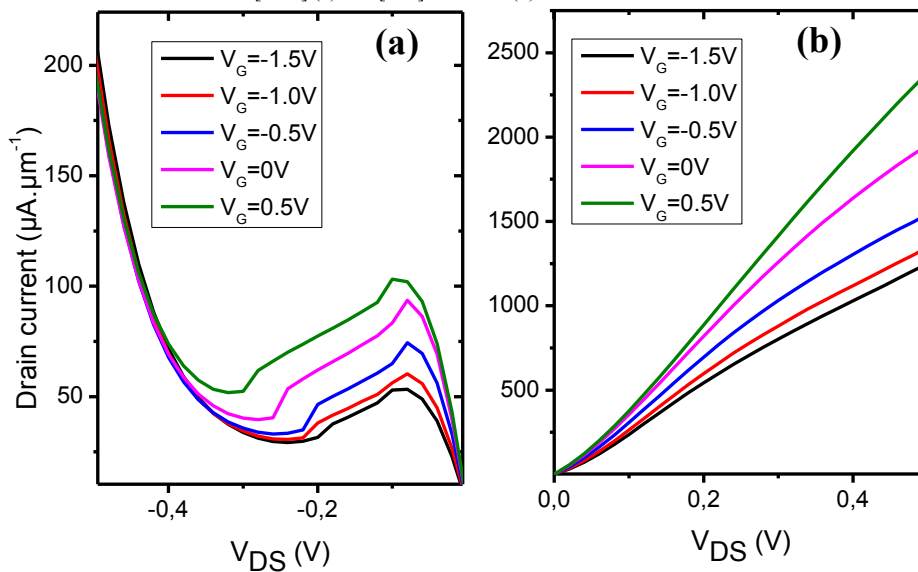


Figure 2. – Tunnel junction forward I-V characteristics (left) and ID-VDS characteristics (right) of the  $0.25 \times 2 \mu\text{m}^2$  TFET oriented in [110]

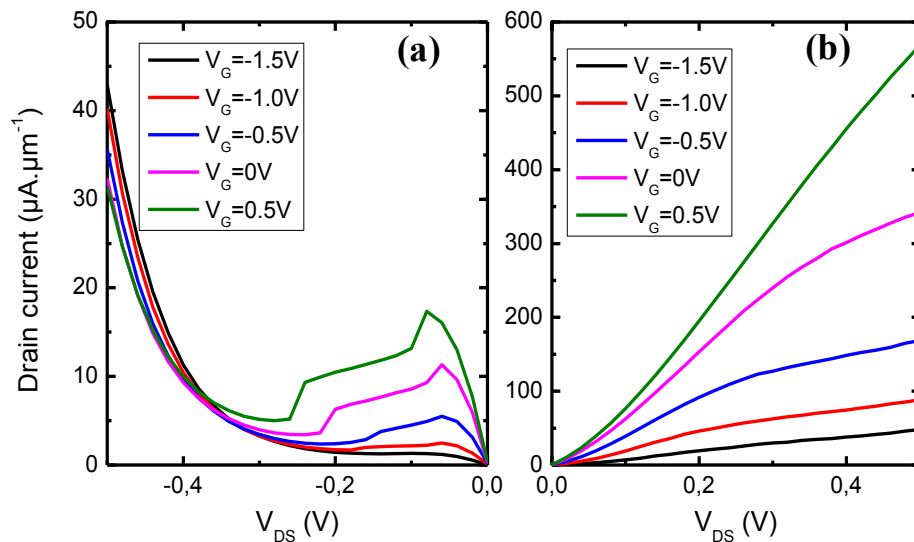


Figure 3. – Tunnel junction forward I-V characteristics (left) and ID-VDS characteristics (right) of the  $0.25 \times 2 \mu\text{m}^2$  TFET oriented in [1-10]