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HEMT GaN Normally Off Reliability comparison

Tanguy PHULPIN, Thy bich Hop DINH

Université Paris-Saclay, CentraleSupélec, CNRS, Laboratoire de Génie Electrique et Electronique de Paris, 91192, Gif-sur-Yvette, France.

Sorbonne Université, CNRS, Laboratoire de Génie Electrique et Electronique de Paris, 75252, Paris, France

ABSTRACT - Recently, new HEMT GaN Normally Off with a buried P-layer have been developed by the LAAS Laboratory to propose a device adapted to embedded power electronics. In this article, several Normally Off HEMT GaN architectures are compared using TCAD Sentaurus simulation: Gate Recess, P-GaN, and Buried P-GaN. Main failure mechanisms are compared to determine the most robust topology. The new structure with P-GaN Buried shows promising properties with a higher threshold voltage stability.

Index Terms— HEMT GaN Normally Off, failure mechanism, TCAD Sentaurus, V_{th} stability, Gate-lag, Buffer trap, Temperature impact

1. INTRODUCTION

GaN transistors on the market are typically HEMT devices. This Normally On structure is used for RF application and demonstrates high performances [1]: a fast switching frequency, with low losses in commutation and in conduction, and high robustness against radiation or temperature variation. In power electronics, however, a Normally Off device is required. Several studies have therefore been defined to obtain the best Normally Off HEMT GaN device, without using a solution such as another Si-transistor in cascode. While this ubiquitous solution is convenient, it maintains the Si limitation, thus the HEMT GaN development.

This article presents three different Normally Off HEMT GaN: one reference and two topologies thanks to their possible realization for power electronic devices in harsh environments. After a note on standard characterization, we focus on the comparison of main failure mechanisms such as gate leakage, buffer traps, temperature effect, or gate degradation. Reliability issues are indeed fundamental to the development of new power electronic devices.

2. PRESENTATION OF THE STUDIED DEVICES: SEVERAL HEMT NORMALLY OFF

We will focus on three devices: one Recess gate device, used as a reference, one commonly used P-GaN HEMT, called E-mode [2], and one Buried P-GaN HEMT [3], as a new device in development [4].

2.1. Gate recess structure and thin barrier layer

The Gate recess structure and thin barrier layer structure have nearly the same principle [5]. They bring the gate Schottky

contact closer to the channel. The goal is that the depletion region reach the channel when a polarization is applied. The current flow will then be pinched off at the zero gate voltage.

2.2. P-GaN Gate HEMT

In this structure, a GaN layer doped P with Silicon doping is introduced below the gate contact region and over the 2DEG. The P-GaN layer lifts up the band diagram, resulting in the depletion of the 2DEG channel, even without external applied bias ($V_G = 0$). The consequence is the possibility of easily modifying the threshold voltage, setting the P doping concentration. This technology is, albeit, rather challenging to realize, and the device behavior is significantly influenced by several layouts and processing conditions [2] limiting the device reproducibility.

2.3. Buried P-region

The cross-sectional structure of this new HEMT Normally-Off is shown in Fig.1. A P-GaN layer, doped with Si, is inserted below instead of above the 2DEG as in the precedent device. If the doping concentration is high enough, conduction bands are sufficiently elevated beyond the Fermi level. As a result, the 2DEG channel is deserted and the HEMT becomes Normally-Off. A positive voltage should be applied to the gate for the current conduction between drain and source. Furthermore, the N-GaN regions should be implanted below the 2DEG to restore the channel regardless of the gate voltage value [3]. As described in the figure, the P-doping is localized at gate level.

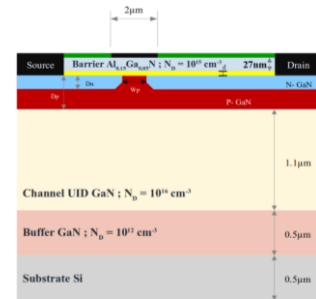


Fig.1. Cross-section structure of Buried p-region HEMT

The first experimental demonstrations of this new structure was presented in [4], which concludes that the appearance of the P-GaN layer (doping about $2 \times 10^{18} \text{cm}^{-3}$) allows the conventional HEMT to shift the threshold voltage to more than 6V, from -5.5V to 0.8V. Moreover, the optimization in processing, as well

as new technology is necessary to achieve a reliable working component.

3. SIMULATION RESULT

3.1. Static characterization

First we simulate the drain current versus gate voltage characteristic for the three devices (**Erreur ! Source du renvoi introuvable.**3). The Recess threshold voltage is lower in comparison with others. A trade-off between AlGaIn width layer and the threshold voltage can be found but a high V_{th} value can't be obtained with this topology as it is demonstrated in the simulation with $V_{th_max}=0,2V$. That's why P-GaN devices were developed. Indeed, increasing the doping concentration below the gate electrode is easier for obtaining a Normally Off state device. However, the technology is not mature enough and a high P doping is laborious, inducing a maximum threshold voltage value that may be rapidly reached. For adjusting this parameter, the best solution appears to be the Buried P-GaN device. P doping area dimensions are adjustable in addition to the doping concentration. In this work, we set the threshold voltage at 1V for the P-GaN device and 2V for the Buried device. We observe the saturation current is largely higher for the Recess device but is almost similar for the others devices. The reason is linked to the polarization effect, with a smaller AlGaIn layer for the Recess device in comparison with others.

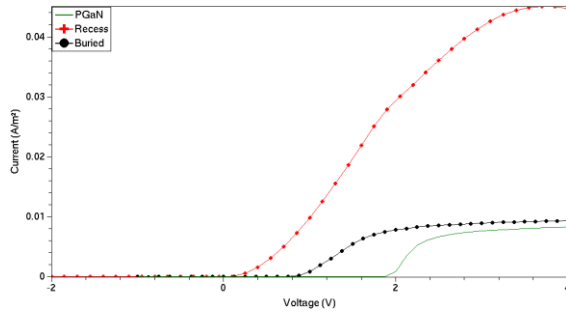


Fig.3. IdVg simulation for Recess HEMT, PGaN HEMT and Buried PGaN HEMT

The second standard characterization is the drain current versus the drain voltage (Fig.4). The simulation was carried out until failure for $V_{gs}=0V$ and $V_{gs}=4V$. For each case, the transistors are logically Off at 0V. The P-GaN and Buried device have the same behavior with a current increase at 1000V whereas the Recess device can bear more than 2500V. When $V_{gs}=4V$, the devices are On and they all conduct until more than 1000V, before the simulation stopped for the buried device at 1200V and before current increase for the P-GaN at 1300V and 2500V for the Recess device.

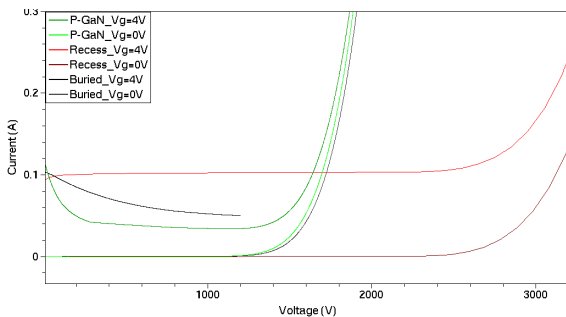


Fig.4. IdVd with $V_{gs}=0V$ and $V_{gs}=4V$ simulation for Recess HEMT, PGaN HEMT and Buried PGaN HEMT

Buried GaN device should logically have a higher robustness to the punch through effect than Recess because of its larger AlGaIn layer. The maximum voltage is yet to be determined.

3.2. Contact degradation results

The contact degradation is simulated in Fig.55. This failure mechanism is represented by the gate size reduction. Therefore several gate size has been evaluated and the electrical impact is minimal on the Recess and on the PGaN devices. Indeed, even with a variation of 25% of the width (from 2 μm to 1,5 μm), the threshold voltage stay identical. Only the Buried GaN device is modified, with the threshold voltage passing from 1,1V to 0,7V. The PGaN device looks more stable than the buried configuration device.

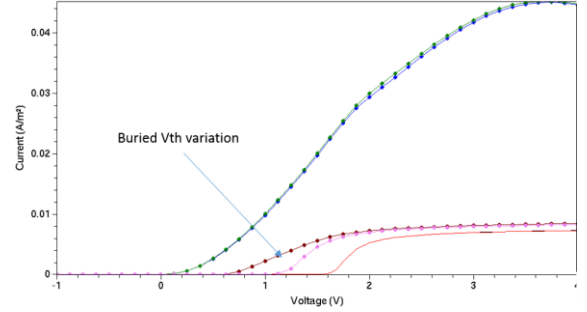


Fig.5: Gate width variation from 2um to 1,5um for Recess HEMT, PGaN HEMT and Buried PGaN HEMT

Further informations are provided in the global article, with the electrical behavior in both case. Several stresses are also evaluated and some explanations are given for proposing the more robust HEMT GaN device.

4. CONCLUSIONS

Two main architectures of Normally Off HEMT GaN devices are compared by simulation in this article. The realization process aside, the Buried P-GaN below the 2DEG device looks considerably more reliable than the P-GaN device even if the latter is one solution currently used by industrials with the cascode device.

The solution presented is less sensitive to temperature variation, with less leakage current, less impact of the gate degradation and less impact of buffer traps concentration. Furthermore, the threshold voltage setting is much easier to fix and can facilitate the corresponding driver.

Even if fabrication processes are not taken into account, the solution proposed by S. Hamady should be the solution used for future power HEMT GaN device development.

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