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Thermal stability of 5 nm barrier InAlN/GaN HEMTs

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InAlN/GaN is a new alternative heterostructure to AlGaIn/GaN promising even higher power densities and high temperature operation [1,2]. Due to the high spontaneous polarization discontinuity maximum drain current densities of more than 2 A/mm and barrier thicknesses down to 5 nm have been demonstrated with semi-enhancement performance [3]. First RF power results have become available with 7.5 nm barrier [4]. However no hints of the stability of these sub-10 nm barrier devices has been given.

In this paper, the properties of 5 nm barrier HEMT devices has been investigated in a temperature ramping experiment as used for AlGaIn/GaN devices [5] and InAlN/GaN devices with 13 nm barrier [2] previously.

The devices have been tested up to 1000 °C in vacuum in an experiment, where the temperature had been ramped in 100 °C steps, keeping the device 20 min at each temperature and cooled to R. T. between each step. As shown in fig. 1 after cycling the maximum FET output current density is not degraded. This means that the polarization discontinuity is fully preserved and no interfacial diffusion has occurred. The pinch-off voltage remains identical and the Schottky diode leakage only marginally increased. No gate sinking, even on the nm-scale of the Ni metallization and no reduction in Schottky barrier height are observed (Fig. 2). The ohmic contacts, which have been alloyed at 850 °C by RTA show also exceptional stability. The initial alloying cycle still kept the alloy front just out of reach for high tunnelling probability. It has been moved within this distance in a very controlled way, however without degrading the contact resistance by the 1000 °C post alloying cycle.

High current densities in combination with thin barriers are only possible for low surface potentials and not possible for unpassivated AlGaIn/GaN devices, where the surface potential is pinned at approx 1.65 eV (and only unpinned by the passivation process) [6]. In the case of the InAlN barrier the surface potential is located approx. 0.4 eV below the conduction band even in the unpassivated case. (see Fig. 3). Due to this low value a high current density of 1.1 A/mm can still be obtained in planar 5 nm barrier devices with a pinch-off voltage of -2 V and a maximum forward gate bias of +2 V resulting in semi-enhancement operation.

In conclusion, the InAlN/GaN heterojunction is exceptionally stable even for barrier thicknesses below 10 nm. Experiments for barrier thicknesses of approx. 2.5 nm (verified by a pinch-off voltage of -0.8 V) are presently performed and results will be reported. Room temperature characteristics are shown in Fig. 4.

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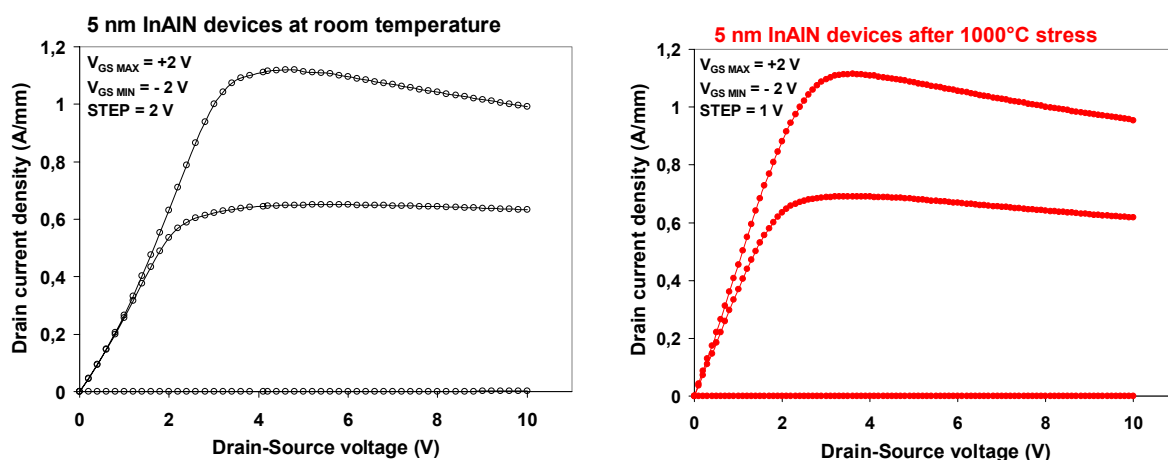


Fig. 1: $0.25 \times 50\ \mu m$ DC output characteristics at room temperature and after 1000°C stress of 5 nm barrier thickness InAlN/GaN HEMTs

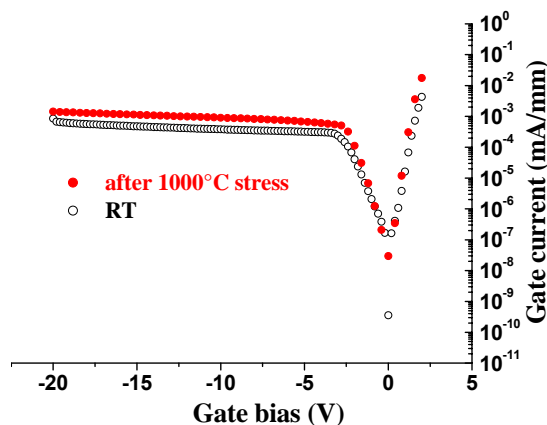


Fig. 2: $0.25 \times 50\ \mu m$ Schottky diode characteristics at room temperature and after 1000°C stress of 5 nm barrier thickness InAlN/GaN HEMTs

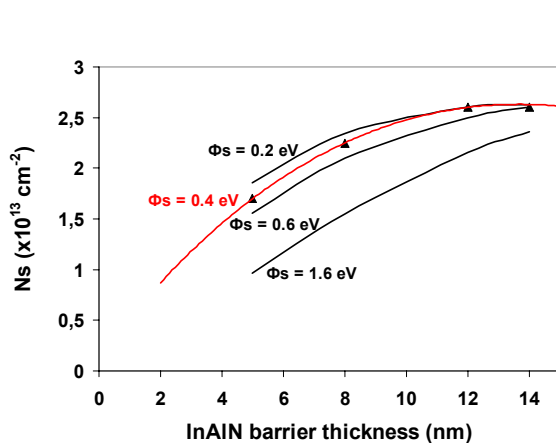


Fig. 3: Simulated N_s as a function of the barrier thickness. Simulations fit with experiment for a $\Phi_s = 0.4\ eV$

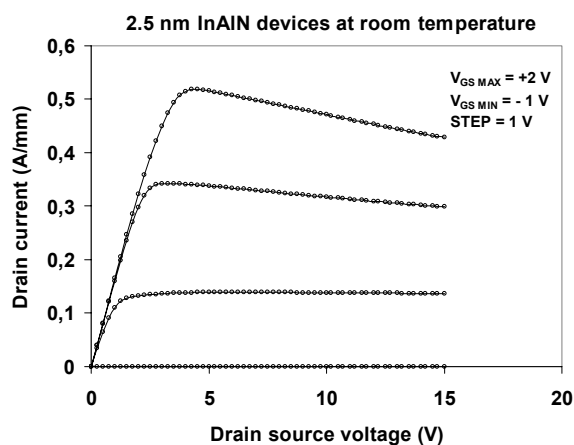


Fig. 4: $0.25 \times 50\ \mu m$ DC output characteristics at room temperature and after 1000°C stress of 2.5 nm barrier thickness InAlN/GaN HEMTs