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Hans Hoffmann Sathler, Lucas Nagano, Bernardo Cougo, François Costa, Denis Labrousse. Impact of multilevel converters on EMC filter weight of a 70 kVA power drive system for More Electrical Aircraft. CIPS 2020 - 11th International Conference on Integrated Power Electronics Systems, Mar 2020, Berlin, Germany. hal-03279931

HAL Id: hal-03279931

<https://hal.science/hal-03279931v1>

Submitted on 6 Jul 2021

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Impact of multilevel converters on EMC filter weight of a 70 kVA power drive system for More Electrical Aircraft

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Abstract

This paper presents the design of a 70 kVA GaN-based multilevel power converter (EMC filters comprised) with a power density and efficiency superior to 10 kW/kg and 98.5% for future More Electrical Aircraft (MEA) power drive systems. The order of magnitude of these parameters, not verified in other papers for a converter of this power, were reached thanks to the precise optimization of each component, such as input/output filters and forced-air heat sink. In addition, PCBs, drivers and current sensor weights were also taken into account in the final converter weight analysis.

1 Introduction

In the last decade, the air traffic has increased by over 60%, being responsible by 2% of the CO₂ emissions worldwide [1]. In order to prevent the impact that this increase in the air traffic will have in the environment, the Europeans authorities imposed new limits for the CO₂ emissions. Reduction of about 1% on the weight of the aircraft represents a fuel economy of about 0.5% to 1.5% [1].

In the actual aircraft, the variety of existing energy vectors is not optimal from performance and weight point of view. However, with a MEA (More Electrical Aircraft) the idea is to replace pneumatic and hydraulic systems by electrical systems to improve aircraft overall weight and reliability. Many of these applications are power drive systems composed by a three-phase inverter, cables and a motor, as well as the EMC filters as shown in Fig. 1.

The setup studied in this paper is composed by a ± 270 V DC to a 70kVA three-phase inverter; a 10m-long, 3AWG, non-shielded cable; and a 50kW electrical machine as presented in Fig. 1. This power drive system is representative of diverse types of loads on an aircraft, such as the Air Conditioning System or Environmental Control System (ECS) and the ventilation of the air conditioning system. DO-160 standard used in aircraft applications imposes limits to conducted emissions (150kHz–152MHz), basically composed by common-mode (CM) currents. To respect these limits, CM input/output filters are used to attenuate the CM currents flowing through parasite capacitances of the inverter, cables and motor to the ground plane (which represents the aircraft chassis). In this power drive system, the heat sink is directly connected to aircraft chassis. Besides, for HVDC networks in aircraft such as the one studied here, there are limits for low frequency harmonics, from 0-150kHz, regarding power quality network due differential-mode (DM) current.

Finally, DM output filter is used to limit maximum overvoltage level at motor terminals and phase current THDi (related to motor magnetic and copper losses). With that in mind, the objective of this work is to analyse the impact of different multilevel inverter topologies and semiconductor technologies on the overall weight and losses of this power drive system inverter.

The goal of this study is to identify power inverter solutions (filters included) with power density superior to 8kW/kg and efficiency higher than 98.5% for the 50kW MEA power drive system application. Inverter solutions must comprise design criteria listed below and highlighted with red marks in Fig. 1.

- Airbus HVDC Power Quality Standard (0 – 150kHz);
- Conducted Emissions DO-160 Standard (150kHz – 152MHz) - Category L, M and H;
- Maximum overvoltage on motor terminals: 750V;
- Output current THDi: 7%;
- Inverter Input Voltage Ripple = 5% of nominal DC bus voltage = 540V;
- CM capacitance maximum value of 150nF (WF5A - impedance 100Ω/10kHz);
- Forced Air cooling;
- Fixed aeronautic cable setup - 3AWG EN4681-006-AZA (10m-long unshielded);
- 50kW three-phase permanent magnet synchronous motor;
- Motor operation point: 3600rpm/132N.m/50kW/130Arms;
- Passive filters only.

Different power inverter topologies and semiconductors technologies are evaluated in Section 2, while the chosen topologies to be evaluated with the respective number of semiconductors in parallel are presented in Section 3.

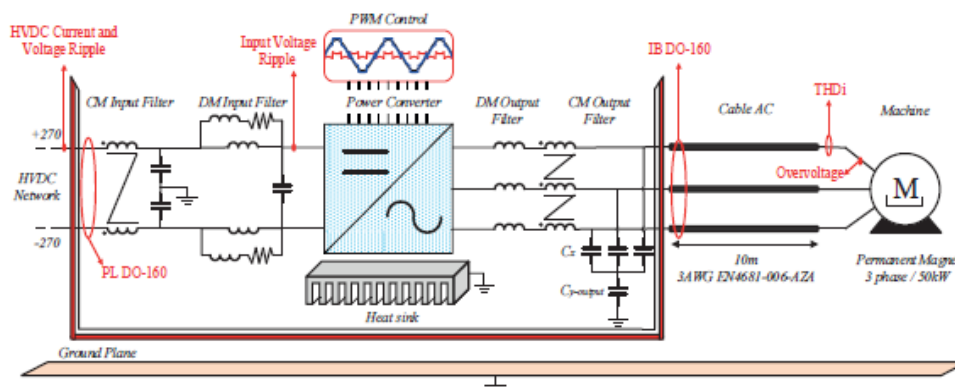


Figure 1 Power drive system

Complete optimization results are presented in Section 4, as well as the impact of switching frequency on power inverter overall weight and efficiency. Finally, the conclusions of the present study are presented in Section 5.

2 Power Inverter Topologies and semi-conductors

When a high performance inverter is desired, a trade-off between losses and weight must be done in detail. In aircraft application, weight criteria remain the most challenging one [2]. Not only semiconductor losses and cooling system weight should be taken into account, but also losses and weight of filters connected to this inverter, which can represent about 70% of the overall inverter weight as presented in [3] for a MEA 45kW bi-directional inverter.

2.1 Semiconductor technologies

With the aim of increasing power drive system efficiency and power density, semiconductors must be chosen considering their respective losses. One method to limit the choice of a semiconductors is to consider a given share on conduction and switching losses, and from the current level, estimate the conduction losses based on semiconductor on-state resistance (for Si or SiC MOSFETs or HEMT GaN) R_{DSon} . Fig. 2 shows the R_{DSon} of different transistor technologies (Si, SiC and GaN) and different breakdown voltages.

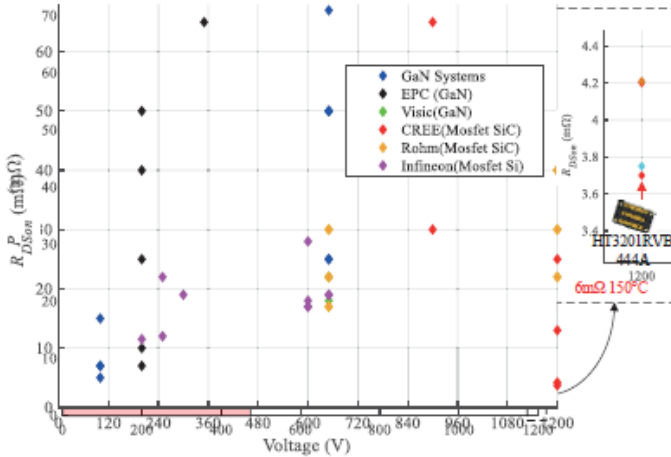


Figure 2 Semiconductors trade-off: Four components were chosen to be compared one from each technology.

Semiconductor series connection is inherently necessary for FC and NPC inverters. However, it is also possible to use low voltage (200V for example) components connected in series to hold the 540V bus voltage. The number of transistors in series N_s to hold bus voltage V_{bus} is given by:

$$N_s = \left\lceil \frac{V_{bus} + \text{margin}}{V_{DS-max}} \right\rceil,$$

where V_{DS-max} is the transistor breakdown voltage. If a maximum value of on-resistance, $R_{DSon-desired}$, is desired, the number of transistors in parallel N_p can be expressed from transistor on-resistance R_{DSon} as

$$N_p = N_s \cdot \left\lceil \frac{R_{DSon}}{R_{DSon-desired}} \right\rceil.$$

Thereby, the total number of transistors N_t is given by:

$$N_t = N_p \cdot N_s.$$

Only components with blocking voltage higher than 600V were considered. In the case that 200V components are used, in 3-level NPC topology for example, at least 6 transistors must be used in series (top of inverter leg). By considering each one with

10mΩ, and $R_{DSon-desired}$ of 10mΩ, 6 transistors are needed in parallel. Totalizing 216 transistors for a three phase 3-level NPC inverter. Assuming an inverter efficiency of 99%, there would be approximately 700W of transistor losses for the current 70kVA power converter. In a hypothetical case that the conduction losses represent 70% (490W) of total losses, the transistor should have a maximum resistance of approximately 9.66mΩ (140W per phase and a current of 130A_{rms}) in the current path. Tab. 1 summarizes total number of transistors in parallel considering the selection in Fig. 2.

Table 1 Number of transistors in parallel to reach of 9.66mΩ based on the components selected in Fig. 3.

Part Number	V_b	R_{DSon}	N_p	T_j
HT3201RVB	1200 V	6mΩ	1	150°C
GS66516T	650 V	56mΩ	6	135°C
IPZ60R017C7	650 V	30mΩ	3	135°C
SCT3017AL	650 V	22mΩ	2	150°C

A 1200V IGBT transistor (SKM600GA12E4) was also considered in a 2-level topology as a traditional reference inverter. This component was chosen since it presents conducted losses relatively close to the 1200V SiC MOSFET HT3201RVB, for the same topology. Tab. 2 presents the semiconductors that were considered for the efficiency trade-off between different multilevel topologies. Different semiconductor technologies were considered to verify the impact of the technology on inverter overall efficiency and power density which will be presented on Section 4.

Regarding power diodes for NPC topologies, SiC Diode C5D50065D was selected among others due low conduction losses.

Table 2 Power semiconductors selected based on the components presented in Fig. 2.

Part Number	V_b	R_{DSon}	Technology
SKM600GA12E4	1200 V	-	IGBT
HT3201RVB	1200 V	3.7 mΩ	SiC Mosfet
GS66516T	650 V	25mΩ	GaN
IPZ60R017C7	650 V	17mΩ	Si Mosfet
SCT3017AL	650 V	17mΩ	SiC Mosfet

2.2 Multilevel power inverter topologies

The traditional 2-level inverter is widely used because of its simplicity and low cost. It usually uses semiconductors with larger blocking voltage 50 to 100% larger than the DC bus voltage. In most semiconductor technologies, the higher the blocking voltage, the higher the switching losses for given switched voltage and current. For that reason, a lower switching frequency should be used to balance conduction and switching losses and increase the inverter overall efficiency. However, low switching frequencies may increase size of passive devices. This deadlock is solved by the use of multilevel inverters. They reduce voltage steps in inverter output voltage, reducing filtering needs. Moreover, some multilevel inverters may increase the effective switching frequency of the output voltage, which further reduces filter size [4] [5]. Another advantage is the use of lower blocking voltage semiconductors, which present lower intrinsic capacitances that is directly related to semiconductor losses [6]. During transistor switching process, semiconductor input capacitance C_{iss} is charged faster (for the same gate resistance) if compared to higher voltage semiconductors, leading to lower

switching losses. The relation between parasitic capacitance and switching energies is exemplified in [7], where 4 GaN transistors are paralleled with the same gate driver, and turn-on and turn-off energies are higher than 2 devices in parallel for the same current level.

The impact of multilevel inverters is also verified when considering DM input filters, as well as EMC filters. In [3], it is shown that replacing a traditional 2-level inverter with a 3-level inverter can achieve values of up to 33% reduction in the overall inverter weight in addition to increased efficiency.

In this study, series multilevel legs are associated in parallel (parallel multilevel – the number of legs in parallel per phase are limited from 1 to 4) and a pre selection of topologies, from a trade-off between inverter efficiency and the number of semiconductors, will be evaluated on filter design to meet the criteria determined in Section 1. Among different inverter topologies, five were selected: regular 2-level cell (FB), Flying Capacitor (FC 3 levels and 5 levels) and Neutral Point Clamped (NPC 3 levels and 5 levels). The Cascaded Half Bridge (CHB) topology was not considered since it needs individual voltage sources for each half-bridge (the setup is fixed to one input voltage source). Modular Multilevel Converter (MMC) topology is commonly used for applications with some kV and MVA [8] [9], no applications for MEA applications were found and it was discarded for this study. ANPC and T-Type need to directly associate transistors in series (at least 2), and this can be a strong issue with the use 650V GaN devices. Direct series connection of power transistors reduces switching speed and it can increase switching losses [10], due to the augmentation of stray inductance in the commutation cell (especially for discrete components as TO-247 packaging). Another problem is that a simultaneous switching is necessary for series connected semiconductors, since even a small delay in switching could cause major damage to the circuit through setting all the bus voltage across a single switch is usually higher than the switches breakdown voltage.

3 Multilevel topologies trade-off: Efficiency x Number of Semiconductors

A study for a pre-selection of inverter topologies was made from loss calculation, by considering datasheet information, of semiconductors listed in Tab. 2. Parameters that were varied and operating conditions are listed below:

- Nominal power = 70kVA (130A_{rms} per phase);
- Switching frequency = 20kHz
- Input Voltage = 540V;
- Modulation Index = 0.96;
- Legs connected in parallel = 1 to 4;
- Inverter output voltage levels = 2, 3 and 5;
- Inverter topologies: 2-level, NPC and FC;
- # of semiconductors in parallel (transistors and diodes) = 1 to 4;

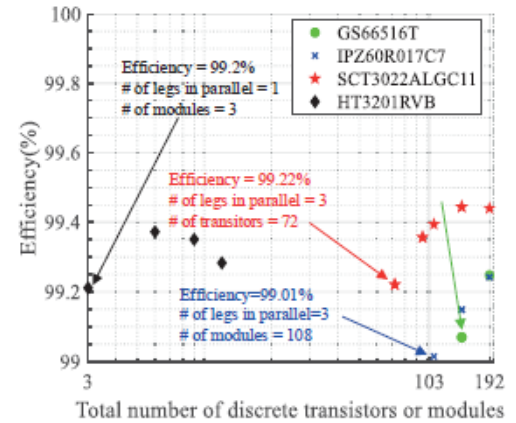
Inverter control was performed using DPWM1 technique [11]. With this technique, semiconductors are not switched during a period when the current reaches its highest value (highest value of the switching energy), thus reducing switching losses, and consequently the overall inverter losses.

Transistors losses were calculated from datasheet information for T_{j-max} -15°C. The choice for high temperature operation is to reduce cooling system weight. An increment of 15%

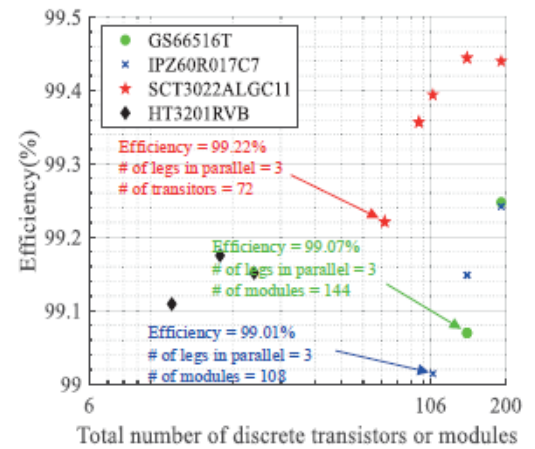
was considered in the inverter losses to roughly estimate the filter losses, which will be precisely calculated during optimization process in Section 4.

Almost 288 transistors are required to make 5-level FC inverter with an efficiency of over 99% with 650V SiC transistors, whereas 192 transistors and 216 diodes are required for a 5-level NPC inverter. For virtually all solutions with efficiency levels above 99%, four legs in parallel per phase are required. The large number of transistors in series, added to the paralleled legs, further complicates the inverter control and integration. Therefore, these topologies will not be considered for future analysis.

Fig. 3a) presents the solutions for the 2-level topology with the 1200V SiC module (HT3201RVB), in which we also considered the series association of 650V components, while the Fig. 3b) presents the solutions for 3-level FC topology. In both figures, solutions are identical regarding the efficiency, number of transistors and parallel legs. This is because, in the first case, the 2-level inverter, with 650V components, is controlled like a traditional 3-level FC, but the floating capacitor is replaced by a small one in order to allow the connection of the transistors in series, and thus to operate as an inverter a 2-level named Quasi Flying Capacitor [12]. Solutions that meet the efficiency criteria of over 99% with 650V transistors (see Tab. 3) have at least 3 paralleled legs, 2 SiC MOSFETs in parallel, 3 Si MOSFETs and 4 GaNs.



(a)



(b)

Figure 3 Calculated efficiency for different number of transistors used in (a) 2-level and (b) 3-level FC inverters.

Solutions for 3-level NPC were considered and the total number of transistors for the 3-level NPC topologies is equal to

the number of transistor 3-level FC topology solutions. However, in addition to using a considerable number of diodes (at least 36), the efficiency of NPC solutions is slightly lower than the 3-level FC solutions. This is because in the NPC topologies topology presents higher conduction losses of the inner switches.

Table 3 Inverter topologies characteristics

Topology	Technology	Legs p/ phase	# of Modules or Transistors	# of Diodes
2Lvl	IGBT	1	3	-
2 Lvl	SiC Module	1	3	-
Quasi FC	GaN	3	144	-
FC 3Lvl	GaN	3	108	-
FC 3Lvl	Mosfet Si	3	72	-
FC 3Lvl	Mosfet SiC	3	72	-
NPC 3Lvl	GaN	4	144	72
NPC 3Lvl	GaN	3	72	36
NPC 3Lvl	Mosfet Si	4	96	72
NPC 3Lvl	Mosfet SiC	3	72	72

Calculation results for different inverter topologies and semiconductors resulted in 709 different combinations. Ten topologies were selected based on the number of components and efficiency; they are summarized in Tab. 3. From datasheet information, the 1200V SiC 2-level inverter presents a calculated efficiency of 99.21% while the 1200V IGBT 2-Level, 97%. Due to the challenges in using and the integration of GaN transistors, as well as the possibility of inverter compression due to the size

of this transistor, four topologies were initially selected: one Quasi FC, one 3-level FC and two 3-level NPC.

Topologies selected in this section were used for global inverter optimization (with filters included) in the following section. In this way, it is possible to verify not only the impact of multilevel topologies on inverter overall efficiency and power density, but also the influence of the different transistor technologies.

Reliability and fault management on power inverter are important subjects and they characterize research subjects themselves. Many authors have already worked on these subjects related to multilevel inverters [13]. However, these themes are outside the scope of the proposed work, whose main goal is to compare power inverters efficiency and power density for aircraft applications.

Finally, after preliminary calculation, NPC topologies were discarded because the heat sink and the DC bus capacitor are considerably heavier for this topology. This happens because of the high number of diodes that need to go on the heat sink and due to the presence of a third harmonic of the fundamental current that is reinjected by the neutral point diode that significantly increases the weight of the DC bus capacitor. Thereby, only the 2-level, Quasi FC and FC topologies were considered for the analysis in Section 4.

4 Optimization results

This section presents the optimization results of inverter topologies, listed in the previous section. Weight and losses of the different elements, individually optimized, that compose the

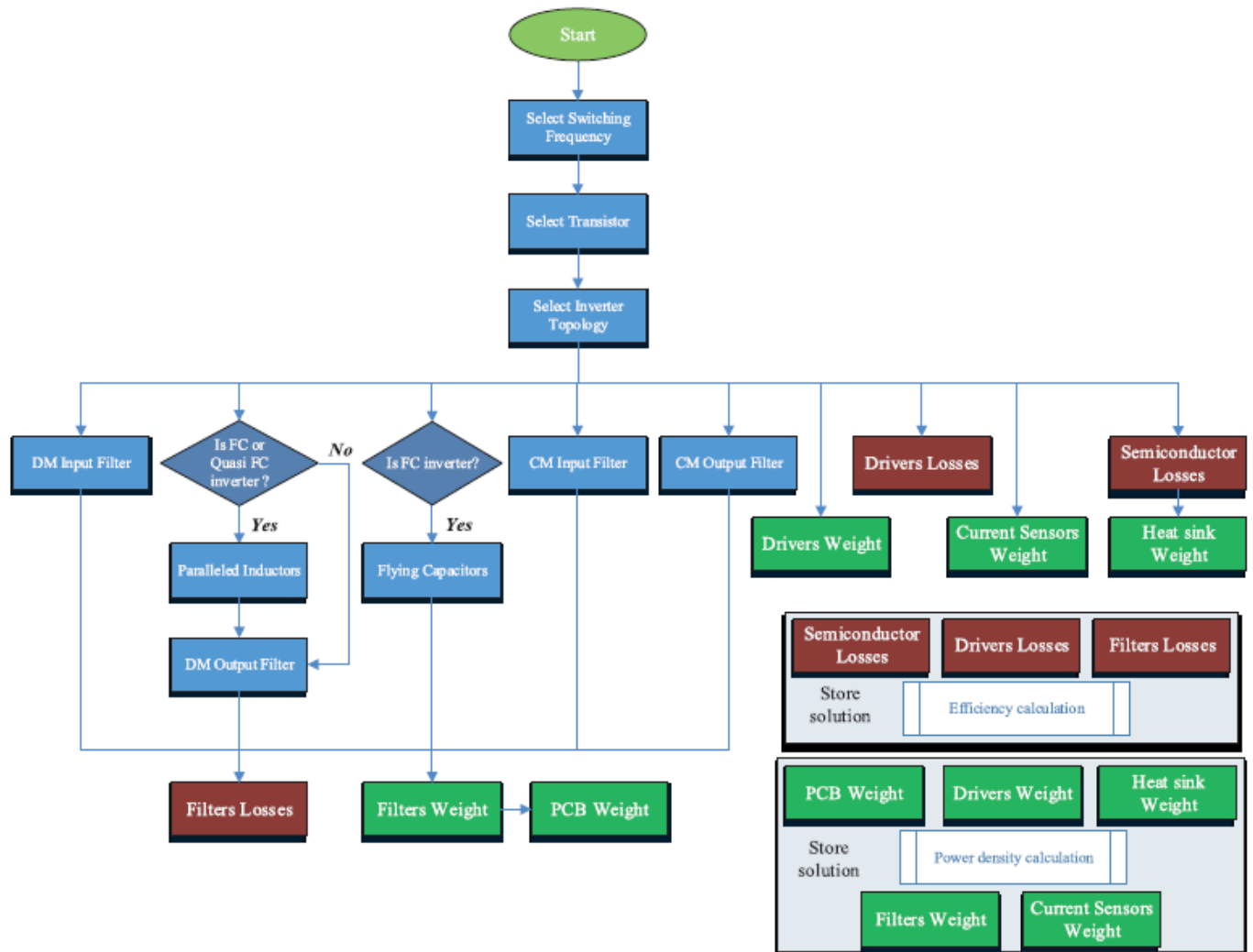


Figure 5 Optimization Flowchart with all devices considered for weight and losses estimation.

inverter are used to draw the efficiency and power density trade-off curves for different switching frequencies (10kHz - 70kHz). Inverters are composed of heat sink, PCBs, current sensors, drivers, input and output filters, and they must meet the criteria described in the Section 1, besides having an efficiency and power density greater than 98.5% and 8kW/kg, respectively.

Each component was individually optimized and no coupling was considered between filters. Fig.5 show a generic flowchart to illustrate all devices considered in the optimization. Finally, two topologies will be analysed, in detail, from the weight and loss distribution of each element that composes the inverter.

4.1 Filter design

To comply with the design criteria presented in the previous section, only passive filters were considered due to the wide range of existing works on EMC filtering [14], power drive system CM current modeling [15] and overvoltage mitigation [16]. Filter design optimization was based on magnetic cores and capacitors datasheet information to have a more accurate estimation of filter weight and volume, regarding design constraints such as core saturation and winding factor for inductors, as well as voltage and current levels for series and parallel combination of capacitors of the filter. Parasitic elements of passive components have a great influence on the frequency response, therefore, estimation of these parasitic elements (mainly the winding capacitance and leakage inductance) were considered according to works at [17][18], as well as frequency response of core permeability and conductor skin and proximity effects.

Different magnetic materials were used according to filter application. For DM filters the Magnetics Powder Cores (High Flux/Kool M μ /MPP) were used, while for the CM filters the VAC nanocrystallin VITROPERM cores were considered, where high impedances are achieved for a small number of turns, reducing minor parasitic effects. The capacitive elements considered are: EPCOS MKP Film (450V to 1100V) family for the DC bus capacitors; EMI Suppression capacitors (MKP Film) Y2/300VAC for the CM filters; CeraLink R/Flex Assembly series for flying capacitors (on FC topologies) and EMI Suppression capacitors (MKP Film) X2/305VAC for DM output filter.

For the sake of simplicity, this paper will not present in detail the optimization routines. Each filter was individually optimized, so possible couplings between the filters were not considered. Only second order LC filters were used, highlighting the addition of a parallel RL damping circuit [19] for the DM input filter. Concerning the CM output filter, it was designed to have a quasi-sinusoidal output current in order to respect THD criteria. Thus, it avoids high losses in damping resistors in the case a high cut-off frequency was chosen to filter dV/dt only.

CM output filter is usually composed of only one inductor, and the use of second order filters is limited due the DM current flowing through the small values of C_y connected between inverter output phases. The hybrid topology presented in [3] uses the common point of capacitors C_x connection of sinusoidal filter to connect CM capacitor C_y . Thus allowing the use of a second order CM output filter and reducing CM output inductance and consequently its weight.

A large number of design variables and design constraints were considered in such a way that the system specifications described in Section 1 are fulfilled. Beyond inverter topology, switching frequency is also seen as design variable, and it influences a large number of internal characteristics of design, such

as cross-section of the magnetic core, core saturation and winding losses as well as semiconductor losses.

4.2 Efficiency x Power Density

Fig. 6 shows the efficiency curves as a function of power density and switching frequency for the different topologies chosen from the optimization of losses and number of semiconductors in Section 3. The traditional 2-level topology based on 1200V IGBT (light blue curve) despite being sized to meet the functional criteria described in Section 1, does not reach the minimum values of efficiency and power density. At 10kHz this inverter has 19.9kg and 1742W of losses, which requires results with power density and efficiency of 3.51kW/kg and 97.5% respectively. The filters sized for this inverter are practically identical to those designed for the 1200V SiC 2-level, so the weight difference between these two solutions is basically due to the cooling system.

The cooling system for the IGBT solution presents 1.3kg while the 1200V SiC solution has half the weight for 10kHz. The major difference, which is the vertical distance of the curves, is due to semiconductor losses: 1516W and 412W for the solutions with IGBT and 1200V SiC, in that order. At the switching frequency of 20kHz, there is a large weight reduction in the DM output filter (13.78kg to 3.86kg) for 2-level inverter solutions, while semiconductor losses increase from 1516W to 2485W (IGBT-based inverter). Semiconductor losses increase proportionally to the switching frequency. Since 1200V IGBT inverter does not satisfy efficiency criteria even for 10kHz, switching frequency was limited to 20kHz for this solution.

The curves with names starting with "FC" present the same multilevel topology, formed by nine legs of a three-level FC inverter, connected three by three via uncoupled inductors. The difference between the curves is the semiconductor technology: 650V SiC MOSFET (red curve), 650V GaN (black curve) and 650V Si MOSFET (pink). This implies that filters weight, PCBs and drivers for these topologies have very similar values, and the difference between the curves are directly related to the semiconductor losses and the cooling system weight.

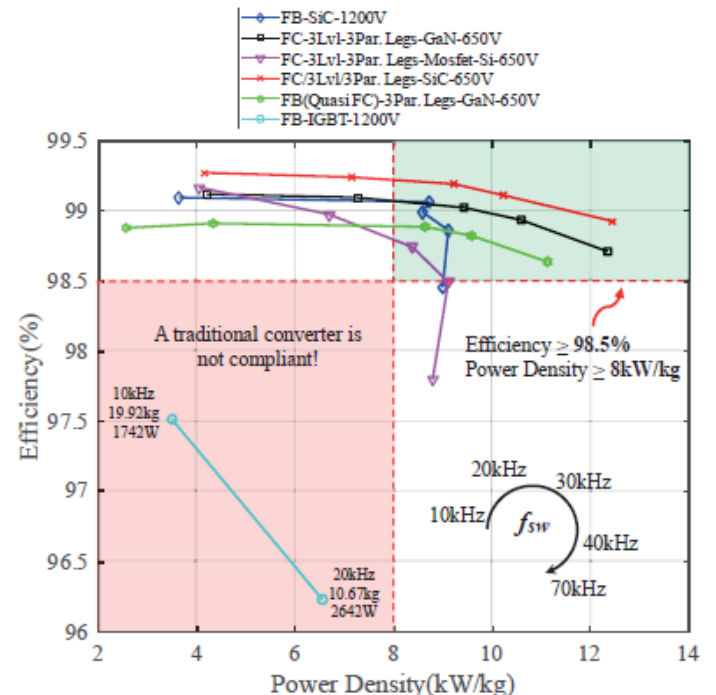


Figure 6 Optimization results of different inverters topologies (3-level FC, Quasi-FC and 2-level) with different semiconductor technologies (IGBT, Si and SiC MOSFETs and GaN) for switching frequency

from 10kHz to 70kHz. Note that IGBT 2-level inverter does not comply to any of power density and efficiency criteria.

The impact of transistor technologies on filters weight is caused by dV/dt and overvoltage at inverter output. Nevertheless, this will only change behavior for frequencies above 30MHz [20] and it is strongly related to inverter integration. Since this study does not take into account PCB routing and inverter integration, filters for these topologies were considered equal. The solution with 650V SiC MOSFET has lower losses than GaN solution, 432W against 525W at 10kHz and 566W against 690W at 40kHz. According to datasheet of the SCT3017ALHR (650V SiC MOSFET), the tests carried out for switching energies considered a gate resistance equal to 0. Low values of gate resistance increases dV/dt and overshoots in inverter output connections [20]. Very fast switching (high dV/dt) can increase EMI problems [15] and overvoltage in machine input connectors [20].

Characterization of this component is required with gate resistance values used in a real application to estimate more reliable values of switching energies. Another important factor is that this 650V SiC has TO-247 packaging, which has parasitic inductance in the terminals of approximately 7nH [22], and it does not have a Kelvin connection. These characteristics can also increase switching energies as presented in [23].

Si MOSFET solution (pink curve) has higher losses than the other multilevel solutions for switching frequencies higher than 20kHz (660W versus 576W - solution with GaN transistor - at 30kHz). Therefore, it presents lower efficiency and consequently higher heat sink weight than the others (1455g versus 913g - solution with GaN transistor - at 30kHz). It is noteworthy that the difference on heat sink weight is not only related to semiconductor losses, but also to thermal exchange surface area of all semiconductors. The solution with 650V Si MOSFET is composed by 108 transistors with 20.70mm x 15.87mm each, while the solution with GaN transistors has 144 components, each one with 9mm x 7.6mm. Finally, 650V Si MOSFET solution is only compliant at 30kHz, where efficiency is 98.7% and power density is 8.38kW/kg. Si and SiC MOSFET solutions both presents a large number of semiconductor with TO-247 packaging, which indicates a greater difficulty in integrating these components and reducing parasitic inductances that can considerably increase switching losses in these components in the real inverter.

The solution represented by the green curve, a Quasi FC, is a variation of the black curve FC topology. Both have the same number of transistors and losses (considering phase shifted triangular carriers - PS PWM). However, the value of the floating capacitor is reduced to allow only the series connection of GaN transistors (synchronize their commutations), but no longer provides the same number of voltage levels at the inverter output. The Quasi FC inverter operates as a FB inverter (same number of output voltage levels). However, in this case with three legs per phase, it results on 4 levels at the inverter output voltage. This reduction in the number of output levels (compared to the FC possibilities) strongly impacts the inductors weight of paralleled legs, which goes from 6.17kg (FC) to 20.72kg (Quasi FC) at 10kHz, and from 1.5kg (FC) to 3.5kg (Quasi FC) at 40kHz.

The FC multilevel solution still has lower overall weight, even considering the floating capacitor weight (6.48kg at 10kHz and 1.6kg at 40kHz), that does not exist in Quasi FC. The biggest difference is noticed in the inverter efficiency, as the Quasi

FC topology has higher output inductors, higher losses are present in the magnetic elements (110W to 40kHz) compared to the inductors of the FC topology (30W to 40kHz), which decreases inverter efficiency. The Quasi FC topology is compliant with design criteria for switching frequencies superior to 30kHz.

4.3 Inverter Weight and Loss distribution

For a better understanding of the weight and loss distribution on the elements that compose the power inverter, results of the 1200V SiC 2-level and the 650V GaN based three level FC with three legs in parallel per phase topologies are detailed in this section, and the impact of increasing the switching frequency on each element will be verified. It will be also evaluated the impact of the use of multilevel inverters on each filter, compared to a traditional 2-level topology. Pie charts in Fig. 7 show overall distribution of weight and losses on 1200V SiC 2-level (blue curve in Fig. 6 for 10kHz and 40kHz). Increasing the switching frequency in this inverter allows us to reduce the overall weight of different components, despite the increase on semiconductor losses and cooling system weight, as summarized below:

- Decrease of 60% on global weight;
- Decrease of 75% on DM output filter weight. DM output filter represents 45.4% of global weight for 40kHz and 71.5% for 10kHz;
- Decrease of 56% on PCB weight. PCB represents 17% of global weight for 40kHz and 16% for 10kHz;
- Increase of 37% on heat sink weight and 67% on semiconductor losses. Heat sink represents 11% of global weight for 40kHz and 3.4% for 10kHz;
- Increase of 32% on CM output filter weight. CM output filter represents 5.1% of global weight for 40kHz and 1.5% for 10kHz;
- Filter losses represents 14.2% of global losses for 40kHz and 35.5% for 10kHz.

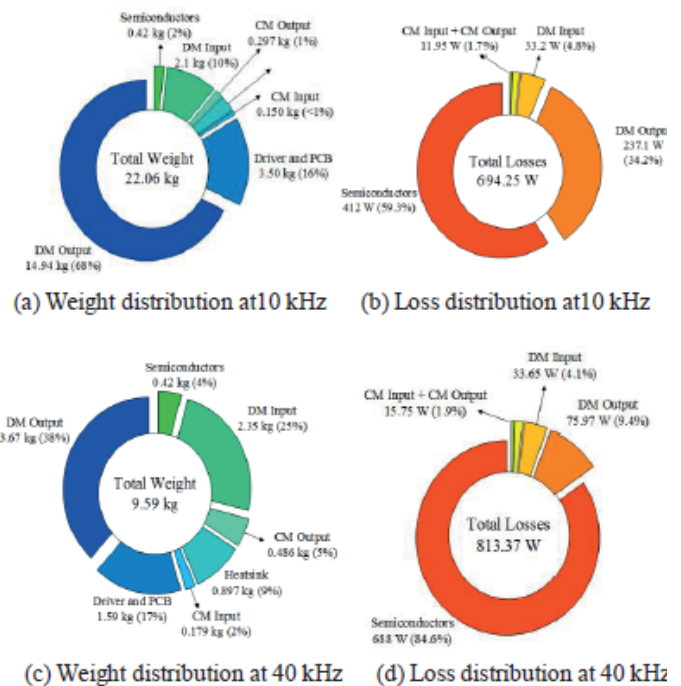


Figure 7 Weight and loss distribution for 1200V SiC 2-level topology and two switching frequencies: 10kHz and 40kHz. Nominal power = 70kVA, $V_{bus} = 540V$ and DPWM1 method.

On the other hand, Fig. 8 shows the weight and losses overall distribution of the 650V GaN based three level FC with three legs in parallel per phase (black curve in Fig. 3) for 10kHz and

40kHz, whose impact of increasing switching frequency from 10kHz to 40kHz is shown below:

- Decrease of 60% on global weight (as 2-level inverter);
- Decrease of 75.5% on Paralleled Inductors + Flying Capacitors weight. Paralleled Inductors and Flying Capacitors represent 46.8% of global weight for 40kHz and 76.18% for 10kHz;
- Decrease of 46.2% on PCB weight. PCB represents 14% of global weight for 40kHz and 10% for 10kHz;
- Increase of 10% on heat sink weight and 31.4% on semiconductors losses. Heat sink represents 15.26% of global weight for 40kHz and 5.5% for 10kHz;
- Increase of 1.3% on CM output filter weight. CM output filter represents 2.3% of global weight for 40kHz and 0.9% for 10kHz;
- Filter losses represents 7.6% of global losses for 40kHz and 15% for 10kHz.

By comparing the FB with 1200V SiC module and the FC with GaN at switching frequency of 40 kHz, the multilevel topology is 13% (almost 1.2kg) lighter than the 2-level inverter. This gain is fractionated into 150g in the cooling system, 400g in PCB, 380g in the DM output filter (in the multilevel topology the interleaved inductors and floating capacitors were considered) and 190g in the CM filters. This result can be translated into a fuel save.

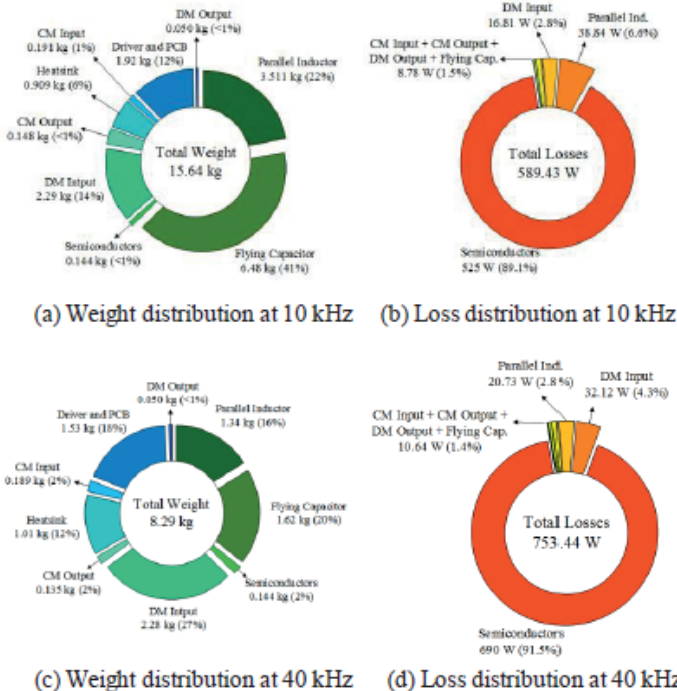


Figure 8 Weight and Loss distribution for the 650V GaN based three level FC with three legs in parallel per phase and two switching frequencies: 10kHz and 40kHz. Nominal power = 70kVA, $V_{bus} = 540V$ and DPWM1 method.

In 2007, the fuel cost per weight unit, in the life time of an aircraft, was about 1500 €/kg to 2000 €/kg [24], which means that the topology FC with GaN could represent a gain between 1800€ and 2400€, in fuel save, compared to 2-level inverter.

5 Conclusions

This paper aimed to present the impact of the use of multilevel inverter topologies and different semiconductor technologies on the weight and overall performance of a 70kVA inverter that meets the requirements of the future more electric aircraft. A precise optimization was presented for the design of filter passive elements and the heat sink, which shows a good representation of weight and losses of the devices that compose the in-

verter. In the work described in [3], it is shown that for an aircraft system with a power 45kW, an optimized three-phase bidirectional inverter with the EMC filters included has a power density of 5.3kW/kg and 99.2% of efficiency. Comparatively, this paper demonstrates for a 70kVA system, that it is possible to obtain a converter with weight optimized filter and heat sink (forced-air), with a power density and efficiency superior to 10kW/kg and 98.5%

The use of multilevel topologies has a direct impact on increasing inverter power density from 3.63kW/kg to 4.21kW/kg at 10kHz for a 2-level and 7-level topologies respectively. By passing to 70kHz this increase is even higher, it passes from 9kW/kg to 12.36kW/kg, showing that if the most important criteria is the power density, there is a considerable gain with the use of multilevel topologies, especially with the increase of switching frequency.

Switching frequency has a direct impact on the passive elements of the inverters, such as the differential-mode output inductors, the capacitors of a FC topology and the inductors to parallel inverters legs. By considering only the weight of these devices, a reduction from 14.94kg to 3.67kg has been seen with the increase from 10kHz to 40kHz for the 1200V SiC 2-level. For the GaN based three level FC with three legs in parallel per phase, the weight drops from 10kg to 3kg. Beyond the gain of power density, by using the multilevel inverter, we highlight the challenges related to parallel GaN transistors, the problems of integration WBG transistors in a power inverter, the degrees of freedom in the control of this inverter due to the number of legs in parallel, which can allow a inverter reconfiguration to operate in degraded mode, and even the operation as a Quasi FC inverter (removing a large part of the inverter floating capacitors).

6 Acknowledgments

This paper is part of the EPOWERDRIVE Project, which is sponsored by Airbus, AKKA, Apsi3D, ELVIA, Liebherr, Meggit, Nidec, Safran and the French National Research Agency (ANR).

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