Meander-Type Lines: An Innovative Design for On-Wafer TRL Calibration for mmW and sub-mmW Frequencies Measurements

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Marco Cabbia, *Student Member, IEEE,* Sébastien Fregonese, Marina Deng, *Member, IEEE,* Arnaud Curutchet, Chandan Yadav, *Member, IEEE,* Didier Céli, Magali De Matos and Thomas Zimmer, *Senior Member, IEEE*

***Abstract*—In this work we introduce novel transmission line standards for on-wafer TRL calibration employing a meandering architecture, which aims to keep the inter-probe distance constant and avoid any probe separation during the measurement process, yet establishing the required signal path length between the ports. Measurements will be performed up to 500 GHz on passive de-embedding structures and on a SiGe HBT; they will be calibrated with both a classic approach and this novel "meander-type" technique. Furthermore, measurements will be evaluated by means of electromagnetic (EM) simulation: for this purpose, we will make use of Ansys HFSS on passive test structures. Finally, a novel joint EM-SPICE co-simulation analysis will allow to provide simulated data for a transistor, thus extending our study to active devices; this will allow a complete characterization of the measurements and an insight on the physical limits of our calibration technique.**

***Index Terms*—Characterization, Transmission Lines, THz, Millimeter-Wave, On-Wafer TRL Calibration, SiGe HBT.**

I. Introduction

THE study of terahertz (THz) technologies has seen rapid growth from late 2000's due to its attractiveness to become the technology behind many of the applications that are projected to revolutionize the near future of high-speed communication technologies [1], such as 5G and beyond-5G networks [2] and IoT [3], radar control for gesture sensing [4], and new imaging techniques for health [5] and safety [6]. The existing electronic and optoelectronic THz commercial solutions are not suitable for mass deployment due to high system cost, lack of integration and reliability. To be widely-adopted, new applications have to be suitable to existing technology, performing and simple (i.e. single-chip). That is why silicon-based technologies (nanoscale MOS and SiGe HBT/BiCMOS process) seem today promising to meet those needs [7]. The design of these THz IC goes hand in hand with the improvement of design kit SPICE models, and require, for their part, accurate and trustworthy measurements of the S-parameters of the transistor and verification of the consistency of the high-frequency model. Calibration is a necessary step to deliver the active devices' S-parameters, and the TRL (thru-reflect-line) algorithm [8] has been recommended for this purpose when measuring on-wafer and at microwave frequencies [9]. This method, however, relies on measuring two standards which necessarily have their own different lengths: a line and a thru. The operator is thus forced to accommodate the RF probes on a new pad position. The calibration repeatability is therefore degraded [10] and the error terms calculation might be compromised, thus leading to discrepancies and questionable conclusions on measurements [11]–[14]. Several studies have been led with a focus on contact repeatability and discussions on measurement uncertainty in on-wafer measurement and probe positioning [13], [15]. For instance, Potereau *et al.* [16] set up an experiment to assess the impact of axial probe displacement and observed a 50% variation of the admittance on the port of the displaced probe and a related capacitance drop. They concluded that due to reduced probes' crosstalk, different cable position and other small modifications of the measurement environment, one is exposed to less accurate HF measurements.

This paper will make use of a novel architecture in which transmission lines are designed as meanders [17], i.e. the portion of the upper metal layer carrying the signal from port-1 to port-2 (and vice-versa) is rolled up in the direction perpendicular to the probe axes, as introduced in [18]. This allows to design lines with different lengths, as prescribed by the TRL algorithm, and same pad-to-pad (or port-to-port) distance. Compared to [18], this work will extend the method up to $500\,\mathrm{GHz}$ and make use of a novel layout for the design of structures that reduces both the probe-to-substrate EM coupling and coupling with neighbors, as it will be described in the following. Also, this manuscript employs EM simulation as a way to verify measurement results and interpret them. A new method, dubbed "EM-SPICE co-simulation" [19] will associate HFSS EM simulations to a SPICE model of the device, to evaluate the deviation at the transistor level.

In the next section, our on-wafer TRL calibration test structures and the layout improvements will be presented, as well as the geometrical and electrical characteristics of the meander lines (such as their shape, length, characteristic impedance, etc…). Later on, measurement and simulation procedures will be described. The core section will expose results on both passive (de-embedding standards) and active (reference HBT) test structures, with both calibration techniques (straight and meander approach). S-parameter measurements and extrapolated figures of merit of a SiGe HBT from a state-of-the-art BiCMOS technology will be juxtaposed

Marco Cabbia, Sébastien Fregonese, Marina Deng, Arnaud Curutchet, Magali De Matos and Thomas Zimmer are with IMS Laboratory, University of Bordeaux, 33405 Talence, France (e-mail: marco.cabbia@ims-bordeaux.fr, thomas.zimmer@ims-bordeaux.fr).

Chandan Yadav was with the IMS Laboratory and is now with the National Institute of Technology Calicut, Kozhikode 673601, India.

Didier Céli is with STMicroelectronics, 38920 Crolles, France.

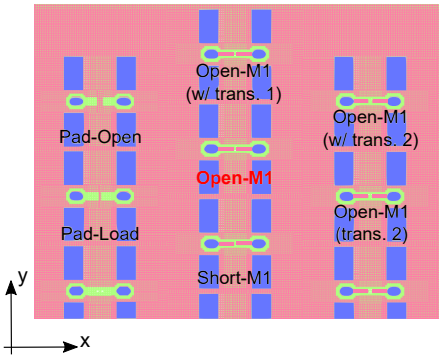


Fig. 1. Top layout view of part of the new mask with the open-M1 in the middle surrounded by its neighbors (i.e. pad-open, pad-load, three layout variations of open-M1 and short-M1). The structure are connected by a "continuous ground plane" and are in a "chessboard" configuration. Color key: pads (aluminium) in blue, M8 (copper) in pink, M1 (copper) in green.

in a similar fashion. Finally, conclusions will be drawn.

II. Test Structures and Calibration Kit Overview

All test structures of the TRL calibration kit and the HBTs are designed and fabricated with STMicroelectronics BiCMOS 55-nm (B55) technology [20] laying on a silicon substrate consisting of 8 metal layers (M1-M8) and vias in the BEOL. The pad geometry has been adapted to be compatible with 100 and $50\,\mu$m pitches for millimeter wave and sub-millimeter wave measurements. Our mask presents several structure design optimizations compared to previous implementations and has been extensively presented in [21]. In particular a "continuous ground plane", made of a M1-to-M8 volume connecting all the ground pads together, and a better isolation from adjacent structures, which is made possible thanks to a chessboard configuration, the absence of holes or slots in the ground, and a "shield" directing more effectively the signal from port to port, are the main new layout solutions (Fig. 1). The structures are in a microstrip configuration: ground is at M1 and, on top of M8, which acts as the access level, aluminum ground-signal-ground (G-S-G) contact pads are realized. The drawn HBT emitter dimensions, mounted in common emitter with CBEBC configuration, are $0.2 \times 5\,\mu\text{m}^2$.

In Fig. 2, the entire TRL calibration kit is presented:

- the novel meander-shaped lines are shown in Fig. 2a-2c;
- a load (Fig. 2d) and an open (Fig. 2e), common to both classic and meander calibration lines;
- classic straight lines are presented in Fig. 2f, 2g.

As originally described in [18], the aim of the meander-type design is to avoid pushing back and forth the probes when measuring a standard with a different probe-to-probe distance, such as the straight 500 GHz line in Fig. 2g. As a matter of fact, the port-1 to port-2 distance of this structure is $185\,\mu$m. The 110 GHz line, which is not presented in the figure since its geometry is the same of the 500 GHz line, has, for its part, a port-to-port distance of $595\,\mu$m. To characterize both of these lines, one is confronted with the need to manually withdraw the RF measurement probes and lay them back down to the pads, since the port-to-port distance of every other structure in our wafer is $65\,\mu$m. Therefore, lines creating a meander-type path for the signals have been designed. This is done in order to maintain the inter-probe distance and avoid displacing the probes. As a useful consequence, no calibration imperfection due to mechanical movement in RF cables and mmW heads is introduced and the on-wafer calibration standards' occupation is reduced (and in turn, the production costs). The thru (Fig. 2c) is made of 4 unit cells, each routed at a $45°$ angle. It has been adapted in such a way in order to show the same initial bend of the meander lines: the 110 and 500 GHz meander lines (Fig. 2a, 2b) share the same recurring quasi-octagonal pattern made of a total of 12 unit cells, repeated one and four times, respectively. The equivalent lengths must be found in order to perform the TRL calibration and they can be estimated in several ways (according to the considered path). In order to calculate the effective length, we exploited the well-known formula for the signal propagation on a line:

$$S_{21}(\equiv S_{12}) = \exp(-\gamma\, l) \implies \angle S_{21} = -\beta l, \tag{1}$$

where $\gamma = \alpha + j\beta$ is the propagation constant, α being the attenuation constant and β the phase constant; l is the length of a line; $\angle S_{21}$ represents the phase (argument) of the transmission coefficient. Since β is only frequency-dependent and identical in both straight and meander lines, we calculate the ratio between the measurement of $\angle S_{21}$ for the meander and straight line, the length of the latter being unambiguously known. Thus, we derive:

$$l_{M,eff} = \frac{\angle S_{21,M}}{\angle S_{21,S}}\, l_S, \tag{2}$$

the "$_{S,M}$" subscripts indicating the type of line.

The actual length values for the straight lines and the calculated length values for the meander lines are listed in Table I. Thus, the three lines allow a range of measurement validity from 20 GHz to 500 GHz. For implementing the on-wafer TRL calibration with an impedance correction as described in [22], [23], we have drawn two resistive

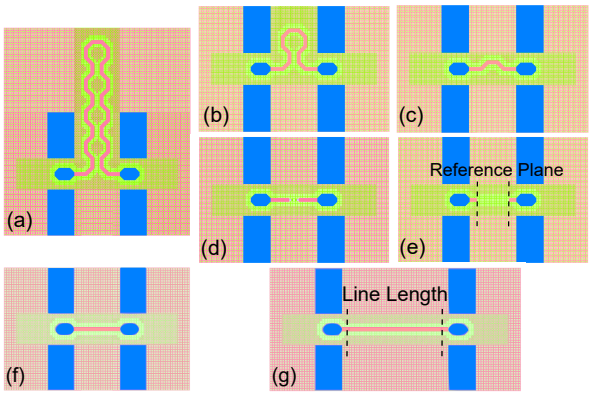
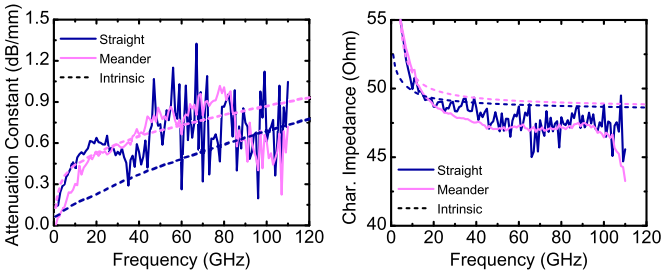


Fig. 2. Top view of the on-wafer TRL calibration kit. 110 GHz meander line (a), 500 GHz meander line (b), meander thru (c), pad-load (d), pad-open and position of reference plane after calibration (e), straight thru (f), 500 GHz straight line with its length (g). This image does not reflect the actual on-wafer structures' topology.

TABLE I. Lengths of thru and lines (in μm).

	Straight (real)	Meander (central path)	Meander (effective)
Thru	65	76	72
Line 110 GHz	595	685	660
Line 500 GHz	185	228	205



(a) α_{ohm} (b) Z_0

Fig. 3. Attenuation constant (a) and real part of the characteristic impedance (b) of the straight 500 GHz line and meander 500 GHz line.

polysilicon loads below M1, one for each port, both measuring around 50 Ω: we called this standard 'pad-load' and it is shown in Fig. 2d. To complete the set of TRL standards, an open, drawn at M8 level and shown in Fig. 2e, provides a high reflection at both ports: we called it 'pad-open'. By performing the on-wafer TRL calibration with our standards, we set the reference plane right at the pads' edge: therefore, we remove all the parasitic components due to pads and access lines. Finally, two test structures called 'open-M1' and 'short-M1' have been designed for transistor de-embedding and will be fully characterized in the next chapter. These structures present a complex BEOL dropping down to M1 where, as their names suggest, an open/short circuit below the contact plane is set. Their composite BEOL is the same as the HBT's, so that most of the parasitic contribution of the BEOL can be further eliminated from the transistor measurement. In addition to being used for short-open de-embedding, we will consider them as passive verification standards of our TRL calibrations.

An observation of the electrical characteristics –attenuation losses and the characteristic impedance– of the shortest (straight and meander) lines is plotted in Fig. 3 up to 110 GHz. The losses for the two types of lines are comparable and quite limited at low frequency (higher measurement noise can be observed in the straight line, most likely because of several repeated contacts which damaged the pads). Concerning the characteristic impedance after correction by our in-house implementation of the TRL algorithm with the pad-load, we can state that both lines' Z_0 are 50 Ω-matched over the whole considered portion of the spectrum.

III. Methodology

A. Measurement Setup

Four sets of measurements were carried out to cover the whole spectrum up to 500 GHz using a setup similar to [21]. The on-wafer TRL calibration is performed using raw measurement data provided by the VNA where the TRL calibration with impedance correction has been applied.

B. Probe and Intrinsic EM Simulation

For passive TRL calibration standards, electromagnetic (EM) simulations are also carried out to complete the measurement verification by importing the layout design in Ansoft's HFSS, as described in [21]. The 3D EM models of the meander structures are placed on a Si substrate, and RF probes models are placed on the RF pads of the device under test (DUT) and of each of the meander calibration standard models, similar to what is done in measurements. To take into account the use of different probe sets in the real world, we perform it for each probe model: 4 sets of data are therefore produced for a single DUT, spanning from 1 to 500 GHz. TRL calibration is also applied similarly to measurement, by means of our implementation of the algorithm in Keysight's IC-CAP. To complete the analysis and to understand the supposed behavior of the DUT, intrinsic simulation, an HFSS simulation of the DUT without RF probes and pads, is also included (Fig. 4).

C. SPICE+EM Simulation

For the active devices, using a compact model simulation results into an accurate description of the intrinsic transistor behavior. However, the resulting description does not take into account the measuring environment (made of probes, pads, BEOL, etc...); moreover, active structures cannot be imported to HFSS, since this software does not treat semiconductor equations such as drift-diffusion equations or any circuit description. Hence, neither way we are able to understand whether the observed measured curves present artifacts generated by the probes or rather due to other causes. To better understand, an hybrid solution has been imagined and presented in [19]: it embeds the transistor model to the HFSS environment. For this method, the open-M1 HFSS model has been modified and two extra lumped ports have been added beneath the contact pins which are normally absent in its layout (Fig. 5). This is done to output the EM signal at the position where the base and the collector should be located, bringing the HFSS model to a total of 4 ports (two probes wave ports + base lumped port + collector lumped port). The resulting 16-terms matrix representing the S-parameters of the

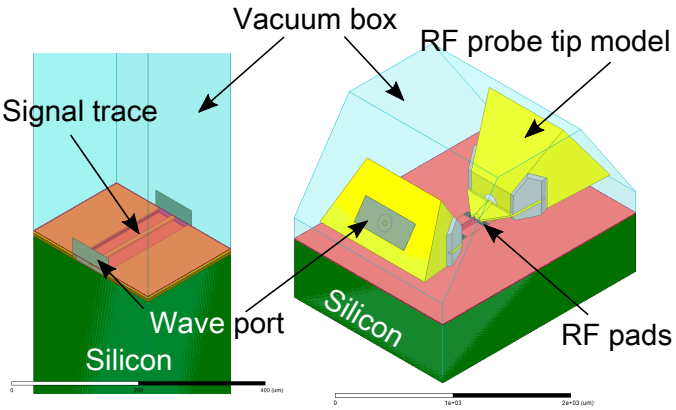


Fig. 4. Intrinsic (left) and probe (right) models for EM simulatiion of the 500 GHz straight line.

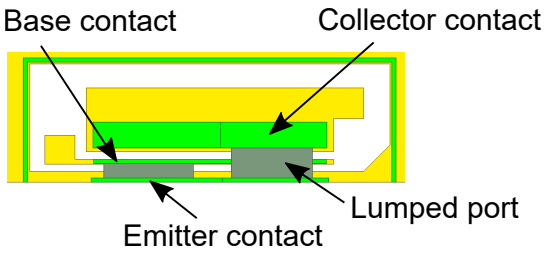
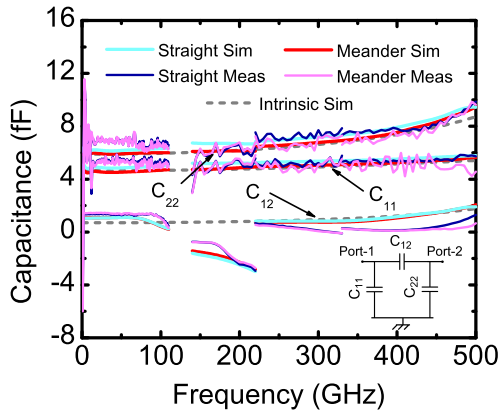
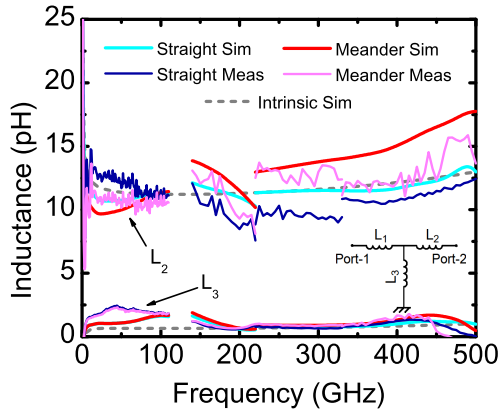


Fig. 5. Connections for the SPICE+EM simulation: lumped ports beneath contacts. Color key: bottom metal level in yellow, color pins in light green, ports in green. Only half of the layout is shown.



(a) Open-M1 capacitances



(b) Short-M1 inductances

Fig. 6. Open-M1 capacitances and short-M1 inductances measurements and probe simulations (both classic and meander TRL calibration are applied) versus intrinsic simulation. As L_1 is symmetric to L_2, it is not shown.

measuring environment is then linked to the compact model, through the well-defined base and collector ports. The joint electro-magnetic + SPICE simulation is performed in IC-CAP after that the transistor circuit model has been simulated with proper parameters (experimentally validated values of capacitance, resistance, transit time, parameters accounting for self-heating and non-quasi static effects, etc...). These data are subsequently assembled in IC-CAP and calibrated with the complete models' simulated data of each calibration standard, and yield the parameters representing the calibrated HBT, after being affected by the measuring environment.

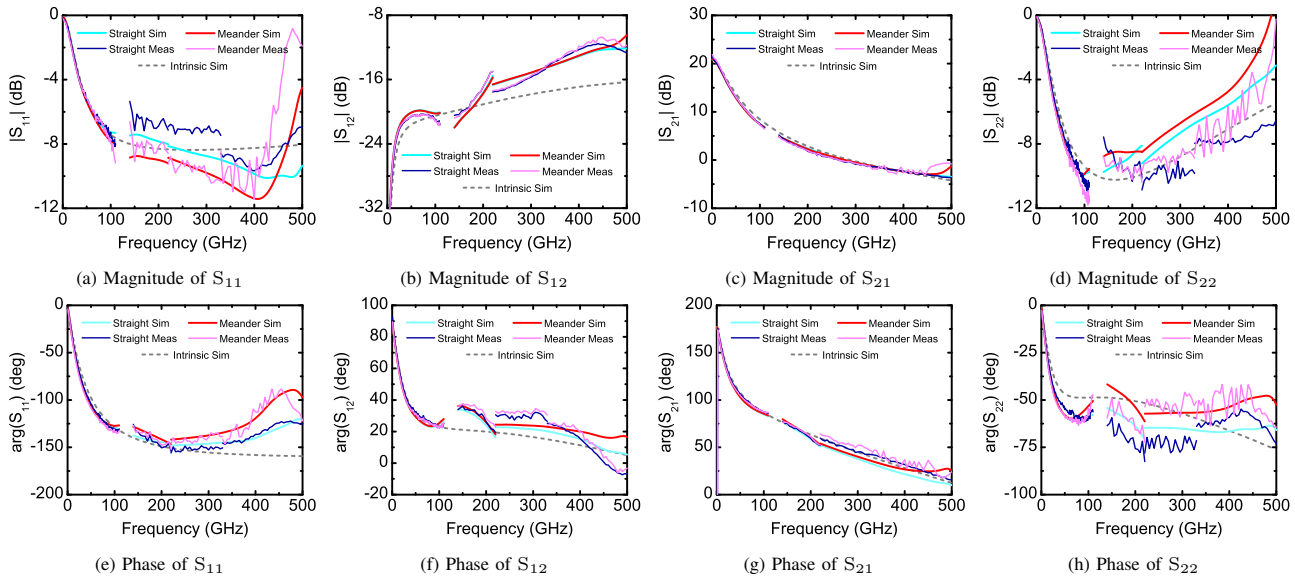
IV. Results and Discussion

A. De-embedding Standards' Characterization

Fig. 6a shows the measured and simulated capacitances of the open-M1 after TRL calibration in which classic straight and meander-type designs are compared. Note that the open-M1 is physically the same for both straight and meander cases. As previously mentioned, what is changing are just two out of four TRL calibration standards, i.e. thru and lines; since the reflect and pad-load (for impedance correction) are identical. Simulations are derived from both probe and intrinsic EM approaches (solid and dashed lines, respectively). Both measured curves show quasi-identical trends, slightly diverging in the last two frequency bands. In the 140-220 GHz frequency range, the coupling capacitance C_{12} is negative and visibly decreases. In a previous work [24], we could prove that the negative capacitance is partially due to the cross-talk between ports caused by these particular probes' design (Picoprobe probes up to 220 GHz) or to the probe-to-substrate coupling. Between these two, the former hypothesis seems to be the most likely, since the mask layout considered in this work takes into account the previous conclusions and improves the pad design to effectively reduce the substrate coupling. The port inductances of the short-M1 are symmetric and appear rather noisy, for this reason only L_2 is presented in Fig. 6b. Simulation well replicates the measured trends (slopes of the curves and small difference between the two approaches, never above 3-4 pH). At high frequency, the simulated meander L_2 anticipates a separation of the meander approach from the intrinsic curve, which is not followed by the measurement in the 330-440 GHz range.

B. Transistor's Characterization

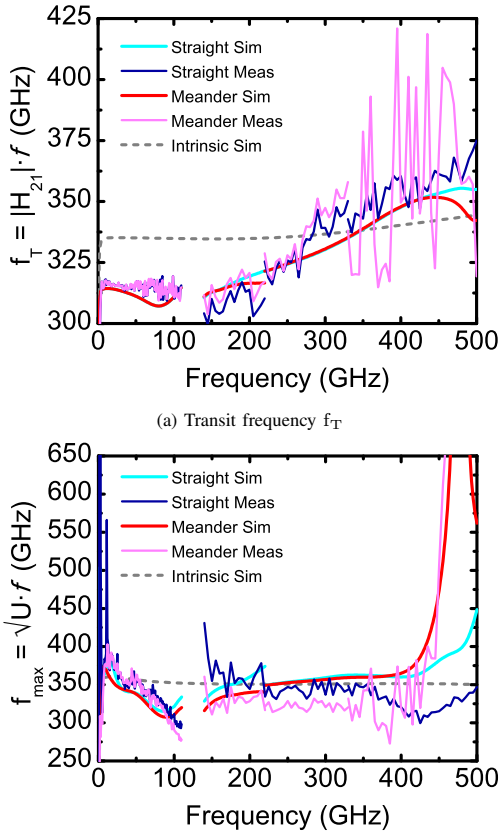
Moving on to the device analysis, in Fig. 7 the S-parameters of the HBT are depicted for the bias point where the f_T-peak is reached. Both simulated data (generated by the SPICE+EM simulation approach) and measured data have been calibrated as before and de-embedded by our short-M1/open-M1 structures. As for the previous passive devices characterization, also in this meander- vs. straight-type design comparison only the thru and line standards for calibration are changing, whilst every other device data are the same. We first consider transmission coefficients. We can observe identical $\mathrm{mag}(S_{21})/\mathrm{arg}(S_{21})$ (Fig. 7c, 7g), S_{21} being easy to characterize, but a slight deviation of both the meander curves starting from around 460 GHz can be also noticed. $\mathrm{mag}(S_{12})$ (Fig. 7b) is well reproduced by the simulation curves particularly at low frequency. Trends are very similar for meander TRL and straight TRL curves, and confirmed by simulation. The curves slightly diverge around 440 GHz, though, yet the simulation does not fully capture this change. Similar considerations can be made for $\mathrm{arg}(S_{12})$ (Fig. 7f). Surprisingly, the measurements after calibration with both meander or straight line show similar behaviors, that is different from the SPICE+EM simulation approach. Possible explanation can be physical effects inside the device that are not correctly captured by the compact model (e.g. NQS effects). Moving on to reflection coefficients, simulation



(a) Magnitude of S_{11} (b) Magnitude of S_{12} (c) Magnitude of S_{21} (d) Magnitude of S_{22}

(e) Phase of S_{11} (f) Phase of S_{12} (g) Phase of S_{21} (h) Phase of S_{22}

Fig. 7. HBT's S-parameters measurements and transistor model+probe simulations (both classic and meander TRL calibration are applied) versus transistor model simulation (intrinsic) at $V_{CB} = 0\,V$, $V_{BE} = 0.9\,V$.



(a) Transit frequency f_T

(b) Max. oscillation frequency f_{max}

Fig. 8. HBT's f_T and f_{max} measurements and transistor model+probe simulations (both classic and meander TRL calibration are applied) versus transistor model simulation (intrinsic) at $V_{CB} = 0\,V$, $V_{BE} = 0.9\,V$.

curves in $\mathrm{mag}(S_{11})$ (Fig. 7a) follow the measurement and the offset between straight and meander is reproduced. The curves crossing that leads to a peak of the meander curve around $480\,GHz$ is also replicated by simulation. However,

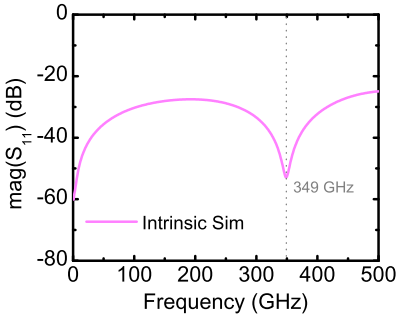
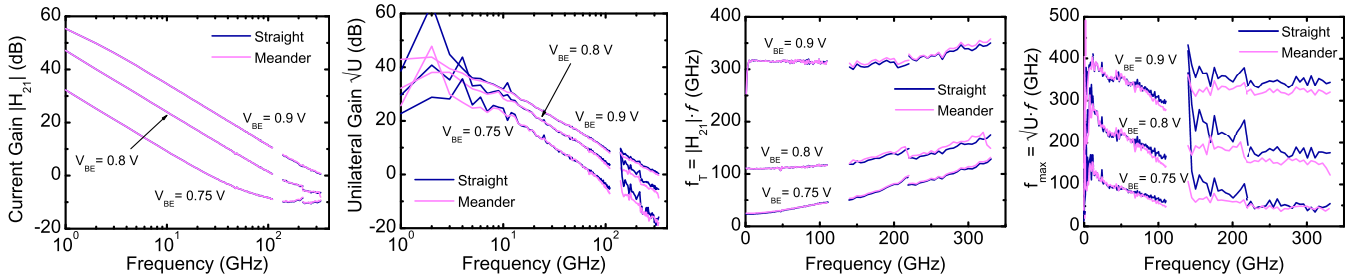


Fig. 9. Reflection coefficient magnitude of the meander 500 GHz line. At $349\,GHz$, we observe a resonance dip.

the straight TRL curve also rises starting from $420\,GHz$, suggesting that the peak does not belong to the meander structure but is reinforced by it. Moreover, we can observe a change in the monotonous decrease of $\mathrm{arg}(S_{11})$ (Fig. 7e) in both curves, again stronger for meander. Analogously to $\mathrm{mag}(S_{11})$, $\mathrm{mag}(S_{22})$ (Fig. 7d) follows the measurement with an offset and tends to a peak at high frequency (meander case, above $500\,GHz$). In the 140-220 GHz range, measurement and simulation curves have opposite trends (for the classic case only). The change in the slope of both straight and meander is also visible by simulation between 100 and $110\,GHz$. Similarly to $\mathrm{mag}(S_{22})$, $\mathrm{arg}(S_{22})$ (Fig. 7h) presents a simulation-measurement offset and a growing trend at high frequency (meander case). The current and Mason's gain, computed from the S-parameter we have just seen, are fundamental to retrieve the two main figures of merit of an HBT: f_T and f_{max}, respectively. Fig. 8 shows these important parameters. For f_T, measurements in the lower bands do not differ significantly, whilst simulation curves appear to indicate a few gigahertz difference. Interestingly, f_{max} simulation and measurement do not match at lower frequency. This behavior is often observed during technology characterization, where



(a) Magnitude of H_{21} (b) Mason's gain U (c) Transit frequency f_T (d) Max. oscillation freq. f_{max}

Fig. 10. Main figures of merit of the HBT measured for different bias points ($V_{CB} = 0\,V$, $V_{BE} = 0.75, 0.8, 0.9\,V$).

the measurement frequency stops most of the time at 67 GHz. This trend can be attributed to the measurement environment and not to the device itself. Reasonable results can be observed starting from 140 GHz, and in particular in the 220-360 GHz range. The growth around 500 GHz (meander) is present in simulation, hinting that this phenomenon is not (entirely, at least) linked to bad user's contact, like we might say for the straight line calibration case, instead.

To sum up, we highlight a degradation of the meander-type TRL calibration performance at high frequency. One may wish to better understand when exactly the loss of validity of this approach takes place and what is the underlying cause. By intrinsic simulation, we observed a strong dip in the magnitude of S_{11} and S_{22} of the 500 GHz meander line: see Fig. 9. These parameters are supposed to be ideally well below 0 dB (and indeed are at most -30 dB): however, at 350 GHz, they show a resonance and the values further decrease below -40 dB. If we compute the wavelength λ from the observed phenomenon's frequencies, we find a value of approximately 375 μm. We observe that this wavelength corresponds to around twice the central path length of the line: 225 μm (Table I). In short, at this frequency, the 500 GHz meander line behaves as half-wave microstrip resonators, reaching the $L = \lambda/2$ condition. Due to the high frequency of occurrence, the S-parameters of the line are perturbed during measurement and when used to find the error terms of the TRL calibration, they may become a contributing factor to calibrated measurements' degradation.

In conclusion, for the designed meander line, the validity range can be extended up to 340 GHz for the above reasons, and the comparison should stop at the 220-325 GHz band. To complete this analysis of the figures of merit of the transistor with the current gain $|H_{21}|$ and Mason's gain U, in Fig. 10 all of them are depicted for three different bias points. The -20 dB/dec characteristic slope is visible for both of them, with very few differences between the straight- and meander-type approach. The current gain and the transit frequency curves (Fig. 10a, 10c) show perfectly superimposed curves for every bias condition. Most of these differences show up at the unilateral gain (Fig. 10b), and therefore at the maximum oscillation frequency (Fig. 10d), those being particularly difficult to evaluate since they are computed from a combination of the Y-parameters computed from the measured S-parameters. The differences are magnified by looking at f_{max}. Since the device is always physically the same, the small discrepancies of the measured curves may be attributable to the wear on the RF pads. Nevertheless, the transistor's maximum frequency after both straight and meander calibration TRL approaches look closely akin and it looks like the best frequency range for f_{max} determination starts from 220 GHz up to 325 GHz.

V. Conclusion

In this work, we proved the validity of an on-wafer TRL calibration approach based on a meander-type design of the line standards up to sub-millimeter wave frequencies. This technique showed good accordance of measurements with both intrinsic and probe EM simulations and few differences with the classic straight line approach, when analysing the crucial de-embedding standards. Furthermore, on the device side, our design proved equally reliable, as it provides evidence to work well also when applied to an active device, reproducing the curves provided by the classic approach. However, SPICE+EM simulation allowed to find the validity limit of our design and the cause behind it, i.e. a resonance created by the physical length of our line. In our view, this is the dominant factor which causes the deterioration of the calibrated trends, more than any other possible explanation, such as measurement inaccuracy or signal coupling. Correspondingly, the meander-type calibration seems to manage the extraction of the main figures of merit of the HBT thoroughly up to the WR-3 band. In order to extend this frequency range, one may think to insert another –shorter– line for higher frequencies: with the meander design, we have gained in wafer area that could be now dedicated to a much less bulky third line (same area occupancy as the thru). Nevertheless, these results make us confident about this approach on on-wafer calibration, that will prove particularly useful in a fully-automated measurement setup, by way of example.

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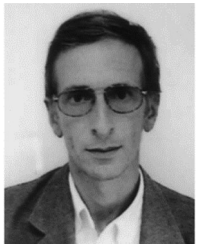
Marco Cabbia was born in Venice, Italy, in 1992. He received his master's degree in Electronics Engineering from the University of Padova, Italy, in 2017, and his PhD degree from the University of Bordeaux in 2021. He is currently a post-doctoral researcher with the IMS Laboratory, University of Bordeaux, France. His current research focuses on HF characterization of SiGe HBTs, including simulation and characterization of test-structures for on-wafer calibration.

Sébastien Fregonese was born in Bordeaux, France, in 1979. He received the M.Sc. and Ph.D. degrees in electronics from Université Bordeaux, Bordeaux, in 2002 and 2005, respectively.,During his Ph.D. research, he investigated SiGe heterojunction bipolar transistors (HBTs), with emphasis on compact modeling. From 2005 to 2006, he was a Post-Doctoral Researcher with TU Delft, Delft, The Netherlands, where his research activities dealt with the Si strain field-effect transistor (FET) emerging devices, focusing on process and device simulation. In 2007, he joined CNRS, IMS, Bordeaux, as a Researcher. From 2011 to 2012, he was a Visiting Researcher with the University of Lille, Villeneuve-d'Ascq, France, focusing on the graphene FET device modeling. He is involved in a couple of National and European research projects such as the European FP7 IP Dot5, Dot7, FET GRADE, and H2020 TARANTO. His current research interests include the electrical compact modeling and characterization of HF devices such as SiGe HBTs and carbon-based transistors.

Marina Deng received the Ph.D. degree in electronics from the University of Lille, France, in 2014. During her Ph.D. research with IEMN, she worked on SiGe HBT small-signal and high-frequency noise characterization and modeling in the sub-THz range. Since November 2015, she has been an Associate Professor with the University of Bordeaux, France, within the MODEL team. Her current research focuses on millimeter-wave and sub-millimeter-wave characterization of HF transistors, including on-wafer calibration and noise measurements.

Arnaud Curutchet received the Ph.D. degree from the University of Bordeaux 1, Bordeaux, France, in 2005, in characterization and modeling of low frequency noise on AlGaN/GaN HEMT technologies. Since 2007, he has been an Associate Professor with the IMS Laboratory of Bordeaux, Bordeaux.

Chandan Yadav received his Ph.D. degree in Electrical Engineering from IIT Kanpur, India, in 2017. From 2017 to 2019, he was postdoctoral researcher at the IMS laboratory, University of Bordeaux, France. In 2020, he joined National Institute of Technology Calicut, India, as an Assistant Professor with the Department of Electronics and Communication Engineering. His current research interest includes on-wafer characterization of semiconductor devices in sub-THz and THz frequency range, EM/TCAD simulation analysis and compact model development of Si and alternative channel material based nanoscale transistors.



Didier Céli was born in Suresnes, France, in 1956. He received the Degree from Ecole Superieure d'Electricite, Gif-sur-Yvette, France, in 1981.,In 1982, he joined the Semiconductor Division of Thomson-CSF, Saint-Égrève, France, and the Central Research and Development, STMicroelectronics, Crolles, France. He is currently a Project Manager, where he is involved in BiCMOS device modeling.

Magali De Matos received the M.S. degree in microelectronics from the University of Bordeaux, France in 1999. She then joined the Laboratory of Integration from Materials to Systems, IC Design Team, IMS, University of Bordeaux, as a Research Engineer. Since 2007, she has been in charge of the characterization platform NANOCOM at IMS, providing support to Ph.D. students working in the domains of IC design and compact modeling of devices. She is involved in sub-THz S-parameter characterization with the Nanoelectronics Group.

Thomas Zimmer received the M.Sc. degree in physics from the University of Würzburg, Germany, in 1989 and the Ph.D. degree in electronics from the University Bordeaux 1, Talence, France, in 1992. From 1989 to 1990, he was with the Fraunhofer Institute, Erlangen, Germany. Since 1992, he is with the IMS Institute, Talence, France. Since 2003, he is Full Professor at the University Bordeaux. His research interests are focused on electrical compact modeling and characterization of HF devices such as HBT (SiGe, InP), graphene nanotubes and Graphene transistors. He was a cofounder of the company XMOD Technologies and is Senior Member IEEE. He has served as a Reviewer for many journals (IEEE ED, EDL, SSE…), was the TPC (Technical Program Chair) of the ESSDERC 2012 conference and participated on the Program Committee of several conferences (BCTM, ESSDERC, EuMW, …). He has authored or co-authored more than 250 peer-reviewed scientific articles, two books and contributed to 8 book-chapters. He currently holds four patents. In 2018, he received the Jan Van Vessem Award from the IEEE International Solid-State Circuit Conference.