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Investigation of Variation in on-Si on-Wafer TRL Calibration in sub-THz

Chandan Yadav, *Member, IEEE*, Marina Deng, *Member, IEEE*, Sebastien Fregonese, Marco Cabbia, Magali De Matos and Thomas Zimmer, *Senior Member, IEEE*

Abstract—This work presents possible variations in TRL calibrated on-wafer S-parameters measurements with change in the on-wafer reflect design (pad open to pad short or vice-versa) in the TRL calibration method. The variations in each error-term values due to the change in the on-wafer reflect in the TRL calibration are examined which shows the source match and reflect tracking as possible error-terms bringing the observed variations in the on-wafer TRL calibrated S-parameter. In order to identify sources introducing these variations in the error-terms values and the S-parameters, TRL calibrated on-wafer S-parameters (S_{11} and S_{22}) of symmetric structures (both reflects i.e. pad open and pad short) are compared. Further, to develop a deep understanding about variations in error-terms values and in the S-parameters, a comprehensive 3D electromagnetic (EM) simulation study is performed. First, EM simulation analyses considering only one structure in simulation setup are performed to examine role of probe-to-probe and probe-to-substrate couplings. Later, EM simulation study is carried out to analyze the impact of the on-wafer neighbours, and the spatial position of the on-wafer neighbours. The EM simulation study shows a strong impact of the coupling of the DUT with the on-wafer neighbours, the spatial placement of the on-wafer neighbours, and the design of the reflect whereby the influence of the probe-to-probe coupling is partially masked by the aforementioned effects.

Index Terms—On-wafer TRL calibration, test structures, electromagnetic (EM) simulation, RF probes, SiGe HBT.

I. INTRODUCTION

ONCE largely unexplored due to lack of the supporting electronics and photonics devices/systems, the THz frequency is now being explored for many potential applications such as ultra-high-speed communication, automotive radar for safe driving, security, biomedical applications etc. [1]–[3]. Some of these applications require high-speed electronic circuits and systems operating in sub-THz or THz range. The development of high frequency electronic circuits and systems requires a prior focus on the fabrication, measurement and SPICE model development of the high frequency electronic components e.g. active (transistor) and passive elements (capacitance, inductance, resistance etc.). In the active high frequency components, the silicon-germanium (SiGe) HBT with f_T/f_{max} up to 505/720 GHz underlines its potential and

suitability in the sub-THz electronics system design [4]. In the sub-THz range especially above 110 GHz, precise on-wafer measurement of Si based devices is as challenging as for III-V based devices where very few measurement reports are available up to 500 GHz [5]–[7]. To obtain intrinsic data of a DUT, the measured raw data of the DUT is processed through a particular calibration algorithm e.g. TRL, LRRM, SOLT etc. (followed by a de-embedding process, if required) to remove the contributions of any additional but essential parts (RF pads and back-end-of-line (BEOL)) from the calibrated measured data. Although calibration methods and de-embedding techniques help to remove undesirable contributions from the measured data, they hardly provide the visualization ability to predict the root cause of any deviation in the measured data from its expected behaviour. In this aspect, the use of the EM simulation looks very worthy to gain insight information through the visualization functionality provided in the EM simulator which enhances the understanding about any existing effects and provide a guideline to reduce undesired effects.

Various research groups have demonstrated the use of the EM simulation to improve the high frequency measurement. In [8]–[15], effects influencing the calibrated S-parameters such as the multimode propagation, the substrate mode, crosstalk, the differences between the calibration and DUT substrate, the CPW ground width, probe geometry, parasitic coupling due to probe and adjacent test structures fabricated are studied mostly up to 110 GHz for structures fabricated on the $Al_2O_3/AlN/GaAs$ /borofloat/ceramic substrates. For structures fabricated on the Si substrate, the impact of the adjacent structures, the probe-to backend environment, the RF probe design, RF pad design and advantage of the on-wafer TRL over the SOLT calibration method in S-parameter measurement are discussed in [16]–[20].

In our previous work [21], on-wafer calibration kit structures design differences lead to variations in error-terms and are presented up to 220 GHz. In this work, we present TRL calibrated on-wafer S-parameters measurement of Si structures up to 500 GHz. The work focuses on variations in the TRL calibrated on-wafer S-parameters of DUTs (open-M1 and short-M1) with change in on-wafer reflect (pad open and pad short) in the TRL calibration method and explores reasons for the observed variations. To verify and develop a clear understanding about observations made in the on-wafer measurements, rigorous a 3D EM simulation study is carried out.

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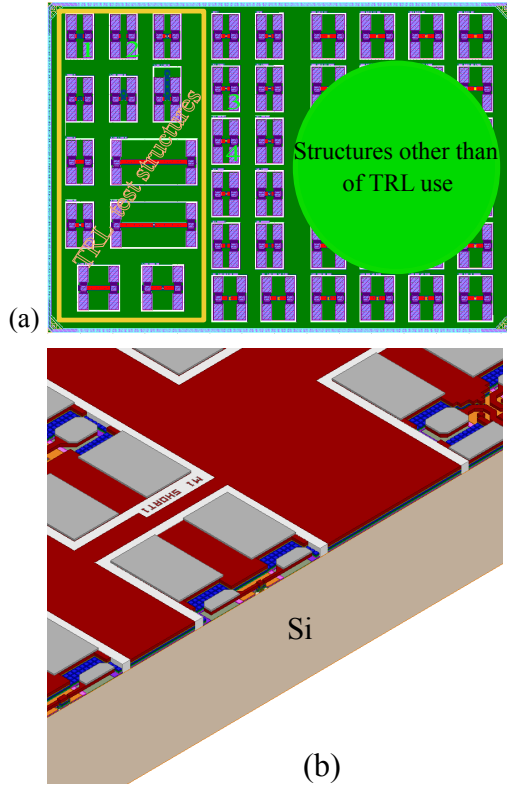


Fig. 1. (a) Top view of the layout used in this study which shows the spatial position of the TRL calibration kit structures, the de-embedding structures (open-M1 and short-M1) and the HBTs. All the TRL calibration kit structures are inside the yellow box, where the position 1 and 2 shows reflects pad open and pad short. The de-embedding structures and HBTs are placed right to the yellow box where the position 3 and 4 are corresponding to open-M1 and short-M1. The thin white boundary around all the structures indicates the oxide ring from M8 to the Si substrate surface and the same is shown in cross section view in (b). The white oxide ring is put in place around each structure to provide electrical isolation between them.

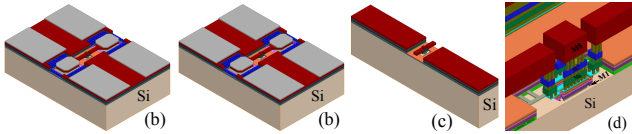


Fig. 2. 3D schematic views of de-embedding structures on Si substrate (a) short-M1, (b) open-M1, (c) only intrinsic structure of the open-M1, (d) zoomed image of the open-M1 near to the DUT space to show its design and exposure to the Si substrate. Note that the thickness of the Si substrate is not shown on the same scale used to show BEOL.

II. ON-WAFER CALIBRATION STANDARDS

In order to perform the on-wafer TRL calibration, the TRL calibration kit structures (thru, reflect, line) along with other structures are designed [22] and fabricated on the Si substrate according to the STMicroelectronics 55 nm BiCMOS (BiCMOS55 or B55) technology [23]. The top view of the complete layout in Fig. 1 shows the spatial position of the fabricated structures on the Si wafer. Each structure on the wafer is isolated from others by an oxide ring around the structure as shown by white color in cross sectional view in Fig. 1b. The aluminium based ground-signal-ground (G-S-G) RF pads are realized on top of the M8 copper metal layer (see in Fig. 2 and Fig. 3) and BEOL of each structure contains eight copper metal layers from M1 – M8 (see Fig. 2d). Using the designed TRL calibration kit structures, the on-

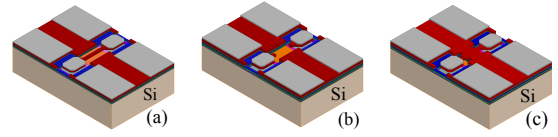


Fig. 3. 3D schematic of the structures on the Si substrate (a) thru of $35 \mu\text{m}$ length, (b) pad open and (c) pad short. After performing the on-wafer TRL calibration, the reference plane shifts at the end of access line which is the termination point of the access line in the pad open.

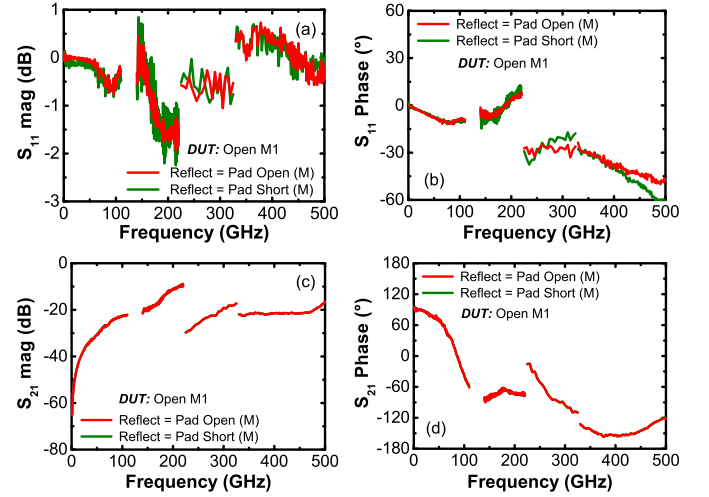


Fig. 4. Comparison of TRL calibrated on-wafer S-parameters of open-M1 obtained after using two on-wafer reflects (pad open and pad short). Magnitude and phase of S_{11} are shown in (a) and (b) while for S_{21} the same are shown in (c) and (d), respectively. In legends, M inside parenthesis indicates measurement. For both reflects, S_{11} values in (a) and (b) should be theoretically exactly the same like the S_{21} .

wafer TRL calibration is performed and applied on short-M1 and open-M1 shown in Fig. 2a and b. The on-wafer TRL calibration is carried out using two different designs of the reflect standard, pad open and pad short while a straight line of length of $35 \mu\text{m}$ is used as the thru standard (see in Fig. 3). Two straight lines of lengths $365 \mu\text{m}$ and $115 \mu\text{m}$ are designed and fabricated to be used in the on-wafer TRL calibration in the frequency range of 1 GHz - 110 GHz and 140 GHz – 500 GHz, respectively. Note that below 25 GHz, a longer line than $365 \mu\text{m}$ length can be used to extend the on-wafer TRL calibration bandwidth to lower frequencies. However accurate lower frequency measurements using the on-wafer TRL calibration method is difficult [24], therefore, off-wafer LRRM and SOLT calibration methods are usually used in lower frequency measurements [19], [25]. A load of approximately 50Ω is also designed and fabricated on the Si substrate in order to apply an impedance correction in the on-wafer TRL calibration using the procedure described in [26]. The impedance correction can also be performed using 3D EM simulation assisted method proposed in [27]. To verify the measurement results, 3D electromagnetic (EM) simulation is performed in HFSS following the EM simulation procedure described in [18].

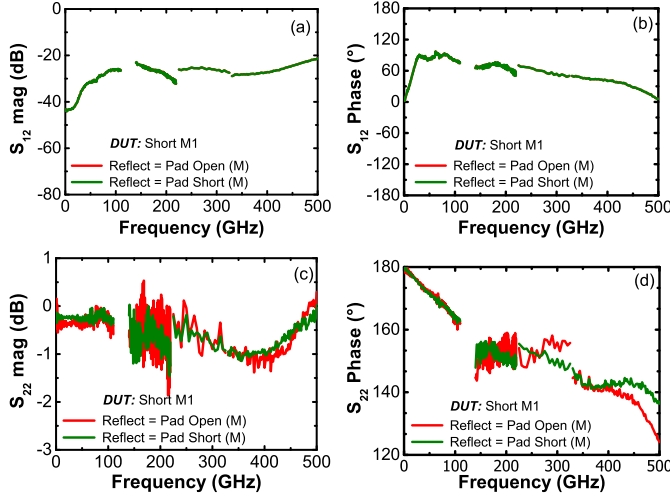


Fig. 5. The TRL calibrated on-wafer S-parameters (S_{12} and S_{22}) magnitude and phase of short-M1 obtained using two different reflects (pad open and pad short) during calibration. Visible differences can be observed in the magnitude and phase of the reflection S-parameter (S_{22}) obtained using two reflects while theoretically they should be exactly the same as obtained in the S_{12} .

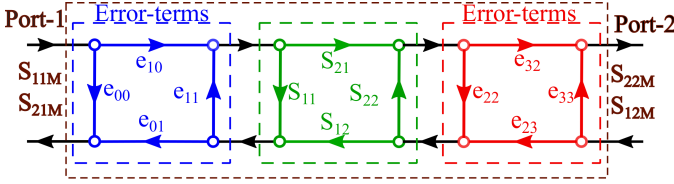


Fig. 6. Schematic of the 8 terms error model [28]. Out of eight error terms, forward direction error terms are e_{00} , e_{01} , e_{10} , e_{11} while e_{22} , e_{23} , e_{32} and e_{33} are backward direction error terms. The S_{11M} , S_{21M} , S_{12M} and S_{22M} denotes the measured raw S-parameters of a DUT including error terms.

III. RESULTS AND DISCUSSION

A. Validation of the TRL calibration: 220 GHz and beyond

First, non-calibrated S-parameters measurements of the fabricated test structures are completed in the frequency bands of 1 GHz – 110 GHz, 140 GHz – 220 GHz, 220 GHz – 325 GHz and 330 GHz - 500 GHz using the 50 μm pitch GGB Picoprobe probes. Then, on-wafer TRL calibration is performed and reference plane is set at the end of the access line (see Fig. 3c). Afterwards, the on-wafer TRL calibration is applied on the non-calibrated S-parameters of the de-embedding structures short-M1 and open-M1 (see Fig. 2a and b). Consequently, obtained TRL calibrated on-wafer S-parameters of both DUTs are shown in Fig. 4 - Fig. 5 in terms of phase and magnitude. Note that only one reflection (S_{11} or S_{22}) and one transmission (S_{12} or S_{21}) S-parameters are shown for each DUT due to the similar trend of the remaining reflection and transmission S-parameters. Throughout the paper, M and S inside parenthesis in figures legend are used to indicate results obtained using measurement and EM simulation data, respectively. In the measurement, the same power is set for each band. The reason behind more noise in 140 - 220 GHz band could be the design of the RF probes which does not allow having a good quality contact on aluminum pads.

TABLE I

TREND OF VARIATIONS IN ERROR-TERMS VALUES OBTAINED USING THE FABRICATED ON-WAFER CALIBRATION KIT STRUCTURES IN TRL CALIBRATION METHOD. IN SUBSCRIPT OF X, "O" REFERS TO USE OF PAD OPEN AND "S" REFERS TO USE OF PAD SHORT AS A REFLECT IN THE TRL CALIBRATION METHOD.

S. No.	Name of Error Terms (forward / backward)	% Error $\left(100 \left \frac{X_o - X_s}{X_o} \right \right)$
1.	Directivity (e_{00}/e_{33})	zero
2.	Source Match (e_{11}/e_{22})	non-zero
3.	Load Match (e_{22}/e_{11})	non-zero
4.	Source Tracking ($e_{01}e_{10}/e_{23}e_{32}$)	non-zero
5.	Transmission Tracking ($e_{10}e_{32}/e_{23}e_{01}$)	zero

B. Open as a Reflect or Short for the on-wafer TRL calibration?

In Fig. 4 and Fig. 5, TRL calibrated on-wafer S-parameters of DUTs are shown using following two sets of on-wafer standards in TRL calibration method:

- 1) Thru, line and reflect = pad open
- 2) Thru, line and reflect = pad short.

Note that in both sets of TRL standards, only reflect is different. The fundamental theory of the TRL calibration uses properties of a reflect standard to conceptualize this calibration method. A reflect standard design can be either open circuit (pad open) or short circuit (pad short) type. Both types of the reflect designs can be used in the TRL calibration method and the same results are expected using either design. But only transmission S-parameters (S_{12} and S_{21}) are showing equal values for use of either reflect design in TRL calibration as visible in Fig. 4 and Fig. 5. In Fig. 4 - Fig. 5, one observation can be made that TRL calibrated on-wafer S-parameters (S_{11} and S_{22}) of open-M1 are less noisy for reflect = pad open while the same is true for short-M1 using reflect = pad short. Note that raw S-parameters of both the reflects and DUTs are measured using the same instrument and on the same measurement conditions. This observation (more noticeable for noisy data in 140 - 220 GHz) may be due to the similarity in the basic design concept of the pad open with open-M1 (i.e. transistor open) and pad short with short-M1 (transistor short). Based on this observation, it can be said that pad open and pad short can be preferred to use as reflect in the on-wafer TRL calibration for open-M1 and short-M1, respectively.

C. Reasons for differences in on-wafer S-parameters with change in reflect type in TRL Calibration

To perform the on-wafer TRL calibration, calculation of the error-terms values using the on-wafer calibration kit structures are essential [28]. A variation in error-terms values calculated using on-wafer TRL calibration kit structures with change in reflect will bring variations in the TRL calibrated on-wafer S-parameters of a DUT. The values of all error-terms (X) of the eight-term model shown in Fig. 6 are calculated twice, once for each on-wafer reflect standard. Two forward direction error-terms i.e. directivity and source match are shown in Fig. 7a and Fig. 7b, respectively. The percentage differences in error-terms values due to the use of two reflect standards is calculated

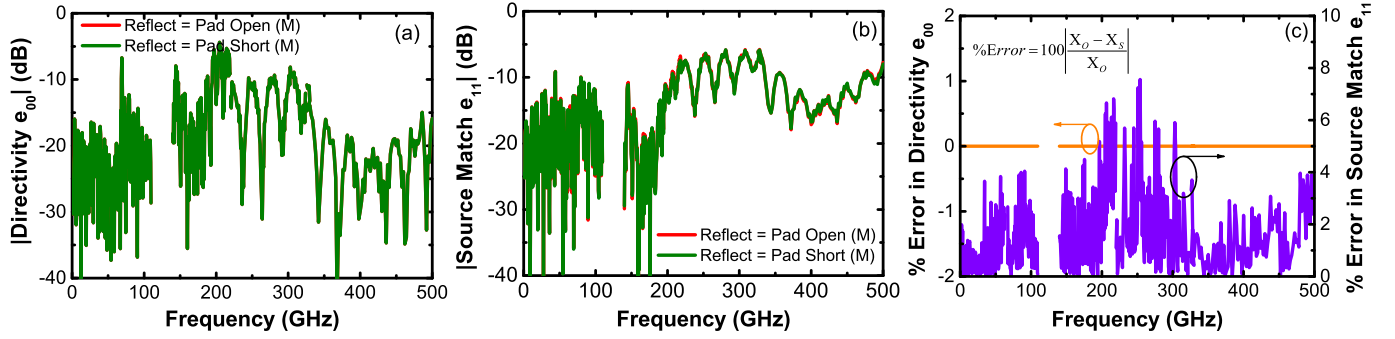


Fig. 7. The behavior of error-terms obtained using pad open and pad short as reflect standard in the on-wafer TRL calibration; (a) forward directivity and (b) source match at port-1. The panel (c) shows percentage error in the error-terms values obtained using pad open and pad short as reflect shown in panel (a) and panel (b). Note that all the error-terms are calculated using measured data of on-wafer TRL calibration kit structures. In calculation of error, "X" denotes a particular error-term while subscript "o" and "s" refers to the use of pad open and pad short as a reflect standard in the on-wafer TRL calibration, respectively.

as $100 \cdot (X_o - X_s) / X_o$ where "X" refers to an error-term while "o/s" in subscript refers to the use of the on-wafer pad open/short as reflect standard in calculation of X. The obtained percentage error in forward directivity and forward source match are shown in Fig. 7c. It is observed that few error-terms values change with change in reflect standard while values of few error-terms remain the same as mentioned in table-I and shown in Fig. 7. The zero percentage error in directivity and transmission tracking is due to their independence from the reflect standards [28].

A comparison of TRL calibrated on-wafer S-parameters of symmetric structures can also help to develop understanding about aforementioned variations in error-terms values and therefore in S-parameters. Both reflects are symmetric in design and their TRL calibrated on-wafer S-parameters (S_{11} and S_{22}) are calculated and shown in Fig. 8. In Fig. 8, S_{11} and S_{22} are expected to have exactly the same values owing to symmetrical design of the pad open and pad short but they have different values. Few possible reasons behind variations in S-parameters of symmetric DUTs can be probe placement error, different probe to pad coupling, different location and design of neighbours, variations in design parameters of the RF probes at port-1 and probe-2 etc. Note that the design of the RF probes in each band is different and therefore the amount of the unwanted coupling varies from one frequency band to other [29]. Due to this, the differences in obtained TRL calibrated on-wafer S-parameters with change in reflect designs are also varying in the different frequency band.

To examine the impact of these factors in the aforementioned variations, rigorous 3D EM simulations are performed. Since, 3D EM simulation is computationally complex and qualitative observation made up to 220 GHz can be extended up to 500 GHz. Therefore, 3D EM simulation analysis is only performed up to 220 GHz.

D. EM Simulation Analysis: Differences in S-parameter by changing Open as a Reflect with Short in on-wafer TRL calibration

First, the intrinsic structure of the open-M1 shown in Fig. 2c is simulated in the EM simulator HFSS. The obtained S-parameter (S_{11}) is shown with a solid pink line in

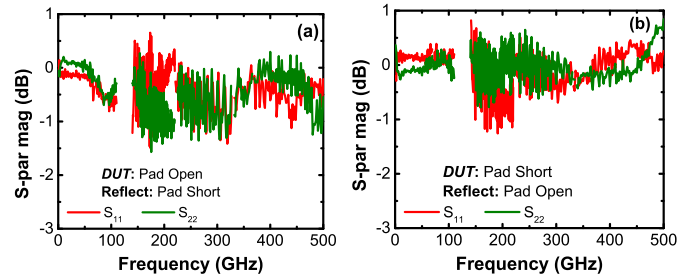


Fig. 8. TRL calibrated on-wafer S-parameters (S_{11} and S_{22}) magnitude of (a) pad open and (b) pad short. The used reflect in the TRL calibration for both DUTs are mentioned in the figures. Since the pad open and pad short has symmetric design, therefore, equal values of reflection S-parameters are expected theoretically (i.e. $S_{11} = S_{22}$) in both DUTs but the same behavior is not visible.

Fig. 9a along with corresponding TRL calibrated on-wafer S-parameters already shown in Fig. 4. In Fig. 9a, the intrinsic EM simulation and the measurement results show a similar trend at lower frequencies but deviation is visible with the increase in frequency. This is due to the fact that, in intrinsic EM simulation, the effect of the RF pads and RF probes are not included. Therefore, EM simulations of the complete structures (calibration kit + DUT) are performed using realistic RF probe models [18], [29] for a qualitative prediction of earlier discussed TRL calibrated on-wafer S-parameters. Note that until unless specified, further EM simulation based S-parameters of a DUT (open-M1) are shown after following the on-wafer TRL calibration procedure used for measurement data discussed earlier.

1) Impact of probe-to-probe and probe-to-pad coupling:

Using the realistic RF probe model corresponding to 140 - 220 GHz [18], [29], the EM simulation of the DUT (open-M1) and all calibration kit structures are carried out individually. The EM simulations are performed excluding all on-wafer neighbouring structures shown in Fig. 1. Note that during the EM simulation of all structures, placement of RF probes at both ports are at the equal distance from the end of the access line associated to respective RF pad. The obtained TRL calibrated on-wafer S_{11} of the open-M1 is shown in Fig. 9a with dashed

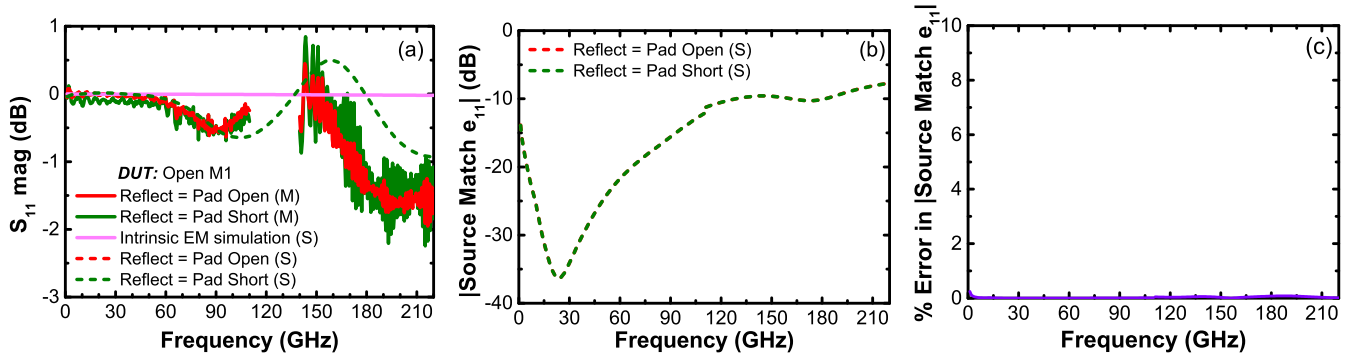


Fig. 9. The reflection S-parameter is shown in (a) while the error-terms are shown in panel (b) and (c). In panel (a), intrinsic EM simulation prediction is shown with solid pink line while the TRL calibrated on-wafer S-parameter obtained using measurement data are shown in solid green and red color lines (already shown in Fig. 4). Note that the EM simulation assisted TRL calibrated on-wafer S-parameters of open-M1 in panel (a) are shown by red and green dashed lines (here superimposed). In the legend, M and S refer results obtained using the measurement and EM simulation data, respectively. The EM simulations are performed excluding the on-wafer neighbours. The EM simulation based on-wafer S-parameter and error-terms for both the reflects are nearly overlapping.

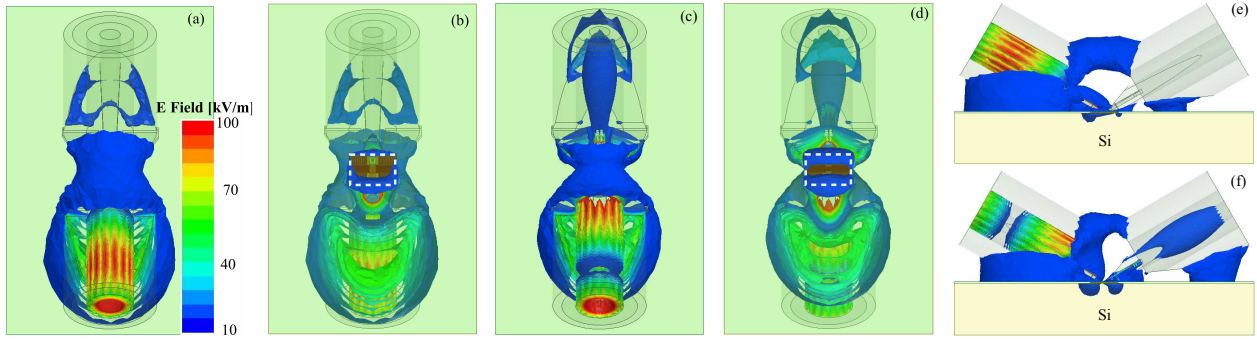


Fig. 10. Electric field distribution in the on-wafer reflects pad open and pad short at 200 GHz where all on-wafer neighbours are excluded in the simulation setup. Panels (a) and (b) show the top and the bottom view of the electric field in the pad open while (c) and (d) show the top and bottom view of the pad short. Panels (e) and (f) show side views in pad open and pad short, respectively. In both reflects, different amount of probe-to-probe and probe-to-substrate coupling can be observed. The bottom view shows coupling with the Si substrate through the oxide ring. The oxide ring surrounding both reflects is indicated by the white dashed box in the backside view shown in (b) and (d). In rest of this work, all the electric field distributions are shown on the scale included in the panel (a).

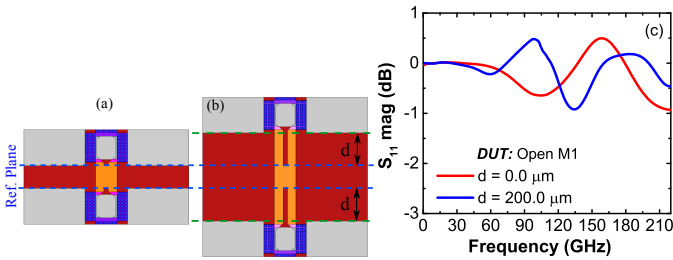


Fig. 11. Top view of the pad open with (a) original dimensions and (b) increased access line length by amount 'd' compared to the original structure. In panel (c), S_{11} above 0 dB for $d = 200 \mu\text{m}$ indicates that the $S_{11} > 0$ in case of $d = 0 \mu\text{m}$ is not due to cross-talk between probe-to-probe.

red and green lines. Noticeable point in Fig. 9a is nearly the same value of the S_{11} for both designs of reflect in the on-wafer TRL calibration. Since the EM simulations are carried out excluding on-wafer neighbours, therefore, this particular condition can be considered closer to the condition that is theoretically requested to apply the TRL calibration method. Looking into S-parameters shown in dashed lines in Fig. 9a, variations in all error-terms are expected to be nearly zero and the same can be observed in Fig. 9b and Fig. 9c. In this condition, comparing associated probe-to-probe and probe-to-substrate coupling in both reflects can help to understand the

role of these couplings in error-terms variations and further in the on-wafer S-parameters. In this perspective, electric field distributions in multi-views (i.e. top, bottom and side views) are shown in Fig. 10 for both reflects on the same scale at 200 GHz. Fig. 10 shows different amount of probe-to-probe and probe-to-substrate coupling in both reflects and differences in coupling are due to differences in design of reflects. From S-parameters and error-terms shown in Fig. 9 and associated couplings in Fig. 10, a conclusion can be made that despite the difference of the amount of probe-to-probe and probe-to-substrate coupling, these couplings are not a dominant factor in aforementioned variations in TRL calibrated on-wafer S-parameters with change in reflect standard.

In Fig. 9a, value of $S_{11} > 0$ is noticeable and the same behavior can also be noticed in [30]. It can be speculated that the obtained $S_{11} > 0$ is due to probe-to-probe coupling induced cross-talk. This aspect is assessed through increasing the access line length of calibration kit structures and DUT by an amount "d" as shown in Fig. 11a. An increased access line length will reduce the probe-to-probe coupling in air but $S_{11} > 0$ is even present for $d = 200 \mu\text{m}$ (see Fig. 11b). This indicates that using the designed on-wafer test structure, impact of probe-to-probe coupling is not a dominant factor to bring $S_{11} > 0$ as visible in Fig. 9a.

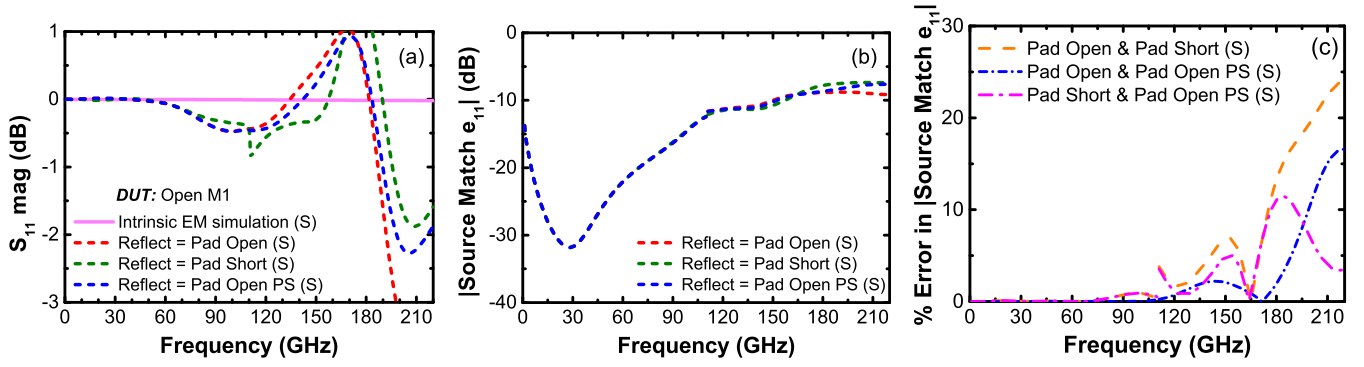


Fig. 12. EM simulation assisted results where "Pad Open PS" is the pad open reflect placed at the spatial position of pad short in the layout. (a) S-parameters behavior of intrinsic simulation is shown in solid pink line and the TRL calibrated on-wafer S-parameters are shown in dashed lines. The error-term values obtained using three reflects "Pad Open", "Pad Short" and "Pad Open PS" are shown in (b). The differences in obtained error term E_{11} values due to change in reflects are shown in (c) e.g. orange color dashed line indicate difference when Pad Open and Pad Short are used as reflects. In the EM simulation with RF probe model, adjacent on-wafer neighbours around DUTs are included.

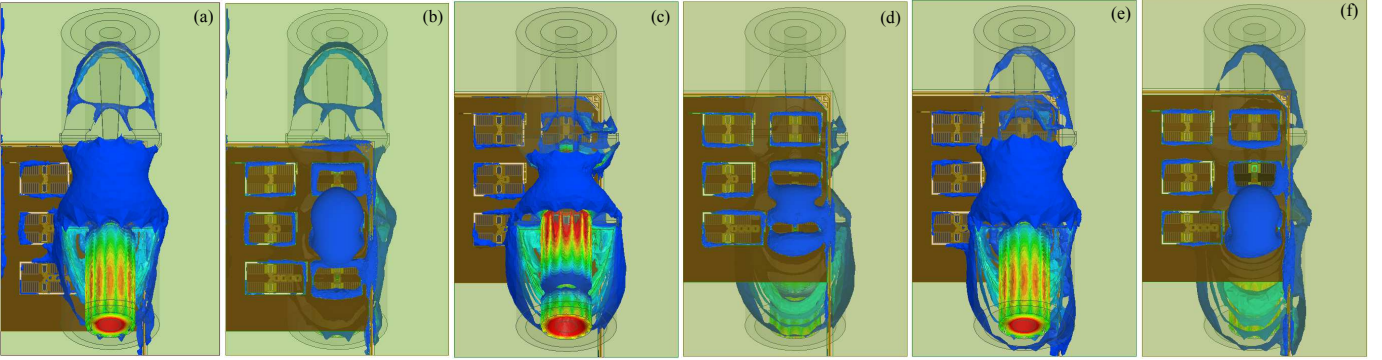


Fig. 13. Electric field contour for the pad open and the pad short at 200 GHz. Panels (a) and (b) show the top view and the bottom view of the electric field contour of the pad open while right (c) and (d) show the top and bottom view of the pad short. The (e) and (f) show top and bottom view of electric field contour for the pad open placed at location of the pad short in the layout. Note that according to our layout shown in Fig. 1, the reflects are positioned at one side of the layout and during the fabrication unknown structures of unknown research group/individual is fabricated besides these structures, therefore, no dedicated structure is placed right and top, we leave vacant spaces during EM simulation.

In the on-wafer S-parameters measurement, influence of the neighbouring structures cannot be ignored. Further, influence of the on-wafer neighbouring structures on the error-terms and S-parameters are investigated by accounting for adjacent neighbours according to layout design shown in Fig. 1a in EM simulation of calibration kit structures and DUT.

2) *Impact of On-Wafer Neighbours and RF Probe position*: For the calculation of source match and reflection tracking error-terms, raw S-parameters of the reflect standard are required. In case of unwanted coupling with on-wafer neighbours, measured raw S-parameters of the reflect standards are prone to vary from values measured excluding the on-wafer neighbours. For the on-wafer reflects with on-wafer neighbours, the impact on the error-term values and therefore on the S-parameter are shown in Fig. 12 with change in the reflect standard in the on-wafer TRL calibration. To gain insight knowledge, associated electric field contours for both on-wafer reflects with their adjacent on-wafer neighbours are shown in Fig. 13a - Fig. 13d on the same scale at 200 GHz. Since the on-wafer neighbours design and spatial placement around both reflects are different, therefore, the influence of undesirable coupling in raw-S-parameters of both reflects are different which lead to variations in error-terms values as shown in Fig. 12b and Fig. 12c.

In order to show the undesired coupling dependence on

the design of the reflect standard, "pad open" is placed at the spatial position of pad short in the layout design and is further referred as "Pad Open PS". A comparison of obtained error-terms and S-parameter for "Reflect = Pad Short" and "Pad Open PS" in the on-wafer TRL calibration are shown in Fig. 12. In Fig. 12, differences for "Reflect = Pad Short" and "Pad Open PS" indicate that the reflect design influences its coupling with on-wafer neighbours which can be observed in Fig. 13c - Fig. 13f.

A comparison of error-terms and S-parameters for "Pad Open" and "Pad Open PS" can also be made in Fig. 12. In these two reflects conditions, design of both reflects are the same but design and spatial position of on-wafer neighbours are different. A change in spatial position of an on-wafer neighbour w.r.t. DUT can change the interaction of a wave between them and results in change in the coupling as visible in Fig. 13. The visible differences for these two reflects in Fig. 12 highlights the importance of a careful spatial placement of on-wafer neighbours in the on-wafer calibration kit design.

E. Open or Short as reflect - based on coupling patterns

In the section III-B, a brief description about suitability of pad open and pad short for open-M1 (transistor-open) and short-M1 (transistor-short), respectively, is presented. To

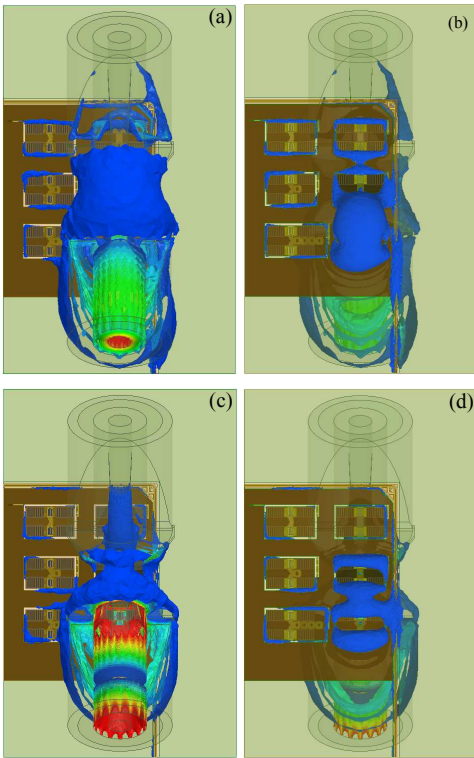


Fig. 14. Electric field contour at 200 GHz for DUTs i.e. open-M1 and short-M1. Note that open-M1 and short-M1 are placed on the spatial position of the pad short in the layout i.e. neighboring environment is the same for both. Top and back side views of open-M1 open are shown in panel (a) and (b) while for short-M1 top and back side views are shown in (c) and (d), respectively. By comparing electric field contours of open-M1 and short-M1 with Fig. 13, one can notice coupling patterns in the open-M1 is similar to pad open while for the short-M1 couplings are similar to pad short.

understand suitability of this combination, an electric field distribution of open-M1 and short-M1 are shown in Fig. 13 on the same scale and at 200 GHz as shown for pad open and pad short shown in Fig. 14. In this comparison, noticeable point is similarities in undesirable coupling patterns of open-M1 with pad open and short-M1 with pad short. The visible similarity in undesirable coupling is due to the open circuit termination in pad open and open-M1 while short circuit termination in the pad short and short-M1. These similarities in undesirable coupling patterns of a particular on-wafer DUT and the on-wafer reflect standard explain the less noisy TRL calibrated on-wafer S-parameters of the DUT and vice-versa.

IV. CONCLUSION

In this paper, we highlighted possible deviations of TRL calibrated on-wafer S-parameters measurements from its theoretical predictions by changing the on-wafer reflect standard in the TRL calibration. It is found that observed variations in S-parameters are due to variations in source match and reflection tracking related error-terms. A comparison of TRL calibrated on-wafer reflection S-parameters of symmetric structures led us to identify possible sources responsible for the variations in error-terms and S-parameters. Rigorous 3D EM simulation study revealed strong impact of undesirable coupling of the DUT with the on-wafer neighbours, spatial placement of the on-wafer neighbours, and the design of the reflect which

masked impact of the probe-to-probe coupling or probe-to-substrate coupling in the observed variations. Minimizing undesirable couplings is important to reduce the observed variations and to improve the S-parameters measurement. On basis of lower noise in TRL calibrated on-wafer S-parameters and similarities in electric field distribution, it can be said that one particular design of the reflect can suit more for a particular DUT than another reflect design.

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