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Yanxiao Sun,[1] Gang Niu,[1,a)] Wei Ren,[1,a)] Jinyan Zhao,[1] Yankun Wang,[1] Heping Wu,[1] Luyue Jiang,[1] Liyan Dai,[1] Ya-Hong Xie,[2] Pedro Rojo Romeo,[3] Jordan Bouaziz,[3] and Bertrand Vilquin[3,a)]

AFFILIATIONS

[1] Electronic Materials Research Laboratory, Key Laboratory of the Ministry of Education and International Center for Dielectric Research, School of Electronic Science and Engineering, Xi'an Jiaotong University, No. 28, Xianning West Road, Xi'an 710049, Shaanxi, People's Republic of China

[2] Department of Materials Science and Engineering, University of California, Los Angeles, Los Angeles, California 90024, USA

[3] Université de Lyon, Institut des Nanotechnologies de Lyon (UMR5270/CNRS), Ecole Centrale de Lyon, 36 Avenue Guy de Collongue, F-69134 Ecully Cedex, France

[a)] **Authors to whom correspondence should be addressed:** gangniu@xjtu.edu.cn; wren@mail.xjtu.edu.cn; and bertrand.vilquin@ec-lyon.fr

ABSTRACT

Field effect transistors (FETs) using two-dimensional molybdenum disulfide (MoS_2) as the channel material has been considered one of the most potential candidates for future complementary metal-oxide-semiconductor technology with low power consumption. However, the understanding of the correlation between the device performance and material properties, particularly for devices with scaling-down channel lengths, is still insufficient. We report in this paper back-gate FETs with chemical-vapor-deposition grown and transferred MoS_2 and Zr doped HfO_2 ($(Hf,Zr)O_2$, HZO) high-*k* dielectric gates with channel lengths ranging from 10 to 30 μm with a step of 5 μm. It has been demonstrated that channels with the length to width ratio of 0.2 lead to the most superior performance of the FETs. The MoS_2/HZO hybrid FETs show a stable threshold voltage of ~1.5 V, current on/off ratio of $>10^4$, and field effect mobility in excess of 0.38 $cm^2\ V^{-1}\ s^{-1}$. The impact of the channel lengths on FET performance is analyzed and discussed in depth. A hysteresis loop has been observed in the $I_{ds} - V_{gs}$ characteristics of the hybrid FETs, which has been further studied and attributed to the charge effect at the interfaces. The HZO films show a relatively weak ferroelectric orthorhombic phase and thus serve mainly as the high-*k* dielectric gate. Charge trapping in the HZO layer that might induce hysteresis has been discussed. Our results show that MoS_2/HZO hybrid FETs possess great potential in future low power and high-speed integrated circuits, and future work will focus on further improvement of the transistor performances using ferroelectric HZO films and the study of devices with even shorter MoS_2 channels.

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I. INTRODUCTION

The continuous scaling-down of the integrated circuits (ICs) and transistors leads to increasing power consumption. The reduction of the power consumption needs to increase the on/off ratio of the transistor and give better turn-off characteristics. It is thus necessary to define novel materials with high carrier mobility and new device structures.

According to the International Technology Roadmap for Semiconductors (ITRS), Molybdenum disulphide (MoS_2), together with graphene and boron nitride, is a potential new material for integration into nanometer scale structures due to its ultra-thin structure and outstanding electrical properties.[1,2] In fact, transition metal dichalcogenides (TMDs), such as MoS_2,[3] $MoSe_2$,[4] and WSe_2,[5] have already been examined as channel materials in field effect transistors. Among them, MoS_2 and WSe_2 have relatively higher carrier

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mobility (up to ~200 cm^2 V^{-1} s^{-1}),[5] while MoS_2 is currently the most studied one due to its outstanding electrical and optoelectronic properties.[5] MoS_2 could be fabricated by chemical vapor deposition (CVD), which is capable of forming large scale monolayers to multilayers with uniform morphology and remarkable optical, electrical, and optoelectronic properties. MoS_2 has the bandgap ranging from 1.2 to 1.9 eV when its thickness decreases from bulk to monolayer, which demonstrates the MoS_2 potential in device modulation and its capability of being "switched off" in electronic devices.[3,6–8] Moreover, CVD fabricated MoS_2 has the mobility of 0.01–13 cm^2 V^{-1} s^{-1} on SiO_2, which is lower than that of the exfoliated MoS_2 nanosheets transferred on SiO_2. Therefore, CVD MoS_2 with higher mobility is more favorable in electronic devices.[9–11]

The 2D material-based FET devices also require low leakage current, therefore, high-k dielectrics have been employed as the gate dielectric in FETs. Hafnia-based materials are applied as standard dielectrics in the current complementary metal-oxide-semiconductor (CMOS) technology due to its high-k characteristic, which is of great potential to realize the low leakage current of the FETs.[12–14] Previous work has reported on FETs based on MoS_2 and HfO_2 dielectric gates with high mobility and on/off ratios, however, the impact of channel lengths in the FETs was not discussed in detail, which was essential in the device fabrication and application of large scale electronic arrays.[15] Recently, intensive studies reported ferroelectricity in Zr doped HfO_2 ($(Hf,Zr)O_2$, HZO), which could be induced with external stimuli. Meanwhile, HZO is also a high-k dielectric material, which has potential in FETs.

Here, we present back-gate field effect transistors based on MoS_2 in combination with HZO thin films as gate dielectrics. The electrical properties of the FETs with channel lengths ranging from 10 to 30 μm with a step of 5 μm were studied. The impact of the channel lengths on the performance of the MoS_2/HZO FETs has been shown. The back-gate MoS_2/HZO FETs exhibit a high on/off ratio of $>10^4$ with the carrier mobility of 0.38 cm^2 V^{-1} s^{-1}, which is premier to conventional Si-based devices. Moreover, the hysteresis in the MoS_2/HZO back-gate FETs was discussed, which was attributed to the charge effect in the FETs. The MoS_2/HZO hybrid system has been proved as a promising candidate for future low power consumption devices due to their CMOS compatible property and ultra-thin structure.

II. MATERIALS AND METHODS

A. Materials synthesis

The HZO nanolayer was fabricated by magnetron sputtering. Deposition details of the HZO film have been reported in the previous work.[16] A phosphor doped (10^{18}/cm^3) n-type Si (100) substrate was prepared by ultrasonic cleaning in acetone and ethanol for 5 min. The native SiO_2 layer on the Si substrate was removed by immersing it in a buffered oxide etching (BOE) solution, followed by cleaning in deionized (DI) water for 4 min. A 100 nm-thick TiN layer was deposited onto the substrate by a radio frequency (RF) reactive magnetron sputtering system with a high purity TiN target in the Ar and N_2 atmosphere. A 10 nm-thick HZO layer was then deposited.

A single layer MoS_2 (6Carbon, China) was fabricated on SiO_2 (200 nm)/n-Si (500 μm) by CVD and then was transferred onto HZO/TiN/Si (001). The polymethyl methacrylate (PMMA)-assisted transferring method was used to transfer the CVD MoS_2 from the silicon substrate to the HZO sample. Details of the transfer process are as follows: PMMA was first coated on the MoS_2 and heated at a temperature of 100 °C. The sample was then placed into a 2 mol/l KOH solution for 2 h to separate the PMMA/MoS_2 nano-flake from the silicon substrate. The separated PMMA film was then cleaned in DI water to remove the residual KOH. Next, the target substrate was applied to take the PMMA film out and MoS_2 could attach to the target substrate. The transferred MoS_2/HZO sample was heated on a hot stage for 30 min at 80 °C after air drying to make sure the MoS_2 is tightly attached to HZO. The sample was then soaked in acetone to etch the PMMA layer.

B. Device fabrication

A highly n-type doped Si (10^{18} cm^{-3}) was used as the substrate. An ~70 nm-thick TiN film serves as the bottom electrode, and HZO thin films with a thickness of 10 nm were applied as gate dielectrics. CVD fabricated MoS_2 was utilized as the channel material. Cr (10 nm)/Au (50 nm) top electrodes were prepared using a lift-off process to realize the drain and source contacts. Optical microscopy (OM) images demonstrated that the morphology of the MoS_2 was uniform and smooth after transferring to the HZO. Details of the lithography process were as follows: the MoS_2/HZO sample was annealed at 150 °C for 30 min in advance to further enhance the adhesion between MoS_2 and HZO. Photoresist (AR-P 3510T, Allresist, Germany) was spin coated on the MoS_2 and placed inside a convection oven for 15 min. Lithography was carried out with the exposure time of 30 s. Developer solution (AR 300-26, Allresist, Germany) was diluted with DI water with the ratio of 1:2. Then, the samples were put into the developer solution for 1 min and rinsed with DI water to remove residual developer solution. After 5 min of drying in the convection oven, the drain and source contacts were fabricated by magnetron sputtering.

C. Characterization

The lattice structure of the HZO layer was measured with a grazing incidence X-ray diffractometer (GIXRD) (SmartLab, Rigaku, Japan). The MoS_2 after transferring to HZO was characterized by Raman spectroscopy (DXR 3xi, Thermo Fisher, USA) using a 532 nm laser with laser power of 2 mW. The MoS_2/HZO FETs were fabricated by lithography and sputtering processes, and OM was performed to measure the channel size of the devices. The surface morphology and the cross section of the MoS_2/HZO heterostructure were examined by a scanning electron microscope (SEM) (Quanta FEG 250, FEI, USA). A Keithley 4200A-SCS semiconductor parameter analyzer was used to measure the electrical properties of the devices, and the measurements were carried out under an atmospheric condition and room temperature without illumination.

III. RESULTS AND DISCUSSION

Raman spectroscopy was performed to study the quality of the MoS_2 after transfer, and the result is shown in Fig. 1(a). The characteristic $E_{2g}{}^1$ and A_{1g} peaks of the MoS_2 were observed at 383.7 and 403.2 cm^{-1}, respectively, corresponding to the in-plane vibration

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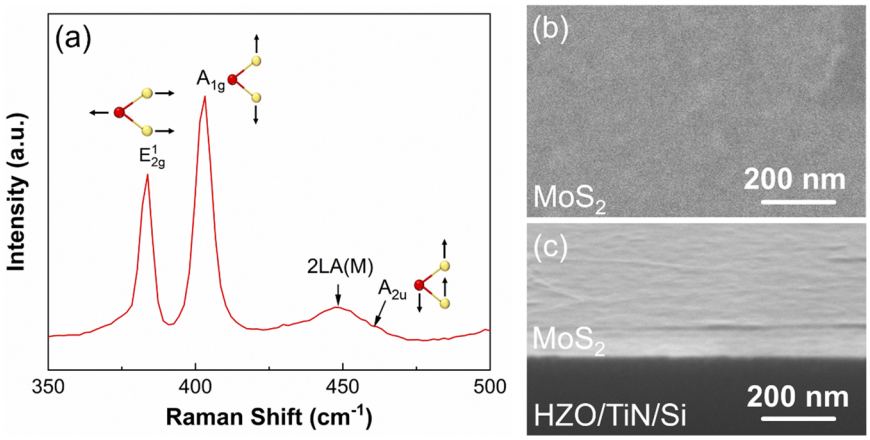


FIG. 1. (a) Raman spectroscopy of MoS_2/HZO samples. Insets of (a) show the bonding vibrations of $E_{2g}{}^1$, A_{1g}, and A_{2u}. (b) Surface and (c) cross-sectional SEM images of the MoS_2/HZO heterostructure.

of two S atoms with respect to the Mo atoms and the out-of-plane vibration of S atoms in the opposite direction, respectively, as shown in the insets of Fig. 1(a).[17] The A_{2u} vibration mode at ~460 cm^{-1} is an IR-active mode, which involves the vibration of both Mo and S atoms. The 2LA(M) mode at ~450 cm^{-1} refers to a second order process involving the LA(M) phonon.[18–20] The difference between $E_{2g}{}^1$ and A_{1g} is 19.5 cm^{-1}, which is in good agreement with the reported mode difference of the MoS_2.[21,22] The SEM image of the MoS_2/HZO surface, as shown in Fig. 1(b), demonstrated that the MoS_2 surface was uniform and a few defects were observed in a large scale. Moreover, the interface of MoS_2/HZO, as shown in Fig. 1(c), was quite sharp with no contaminant or polymer residue. Figures 2(a) and 2(b) show the top view OM images of the fabricated devices, where Fig. 2(b) shows the zoomed-in image of one of the devices with a channel length of 10 μm [marked by a red square in Fig. 2(a)].

The schematic diagram of the MoS_2/HZO FETs is illustrated in Fig. 3(a). The electrical properties of the devices with various channel lengths were investigated. The transfer and output characteristics were measured with channel lengths of 10–30 μm with a step of 5 μm. The variation of the source–drain current density as a function of the source–drain bias (I_{ds} – V_{ds}) of the MoS_2/HZO hybrid MOSFET with different gate bias (V_{gs}) was applied, and the results are shown in Fig. 3(b). The I_{ds} property of the transistor was measured with the V_{ds} that swept from 0 to 4 V, and V_{gs} was applied with a step of 0.1 V ranging from −0.5 to 0.5 V. The highest measured I_{ds} was ~0.1 μA cm^{-1} with V_{gs} of 0.5 V (green circles). It was observed that I_{ds} increased with augmentation of the V_{gs}, which demonstrated the rising conductivity of the channel. Moreover, with the decrease in V_{gs} to 0 V (red triangles) and negative values, the variation of the current I_{ds} flowing through the FETs became smaller, i.e., the control of the FET by V_{gs} became weaker for V_{gs} < 0 V.

At low V_{ds} (< 3 V), a clear sub-linear behavior was observed in the I_{ds} – V_{ds} curve, which demonstrated that the Schottky barrier exists at the drain contact between the electrode and MoS_2.[23,24] The inset of Fig. 3(b) shows the band diagram of the Schottky contact and electron mobility at the Schottky barrier. The existence of such a Schottky barrier on the one hand suppresses the output current and on the other hand reduces the off current of the transistor. The current density of the "off" state of our MoS_2/HZO FETs reaches ~10^{-11} A [see Fig. 4(a)].

Source–drain transfer characteristics [Log(I_{ds}) – V_{gs}] were also measured for the MoS_2/HZO FETs. Figure 4(a) shows the result of the MoS_2/HZO FET with a channel length of 20 μm and a channel width of 100 μm. V_{gs} was applied from 0.5 to 4.2 V with the V_{ds} ranging from 0.1 to 0.9 V with a step of 0.2 V. The threshold voltage (V_{th}) was defined as the transverse distance of the rising edge. It was found that V_{th} = 1.5 V at V_{ds} = 0.1 V and V_{th} = 1.82 V at V_{ds} > 0.1 V. Devices with different channel lengths showed variation of the V_{th}

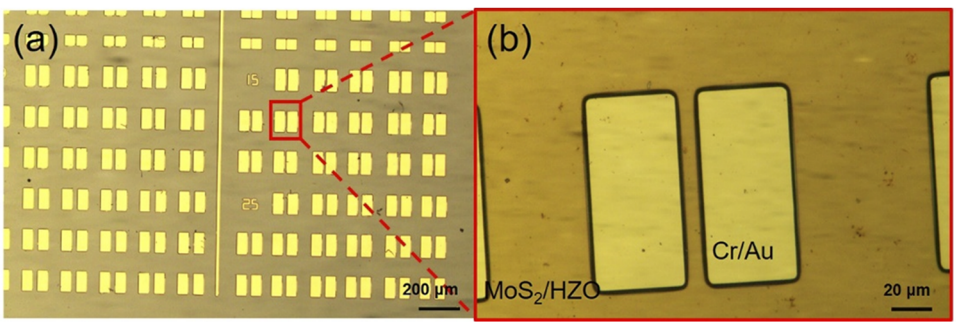


FIG. 2. (a) Optical microscopy image of the overview of the MoS_2/HZO FETs and (b) the zoomed-in image of one of the devices with a channel length of 10 μm.

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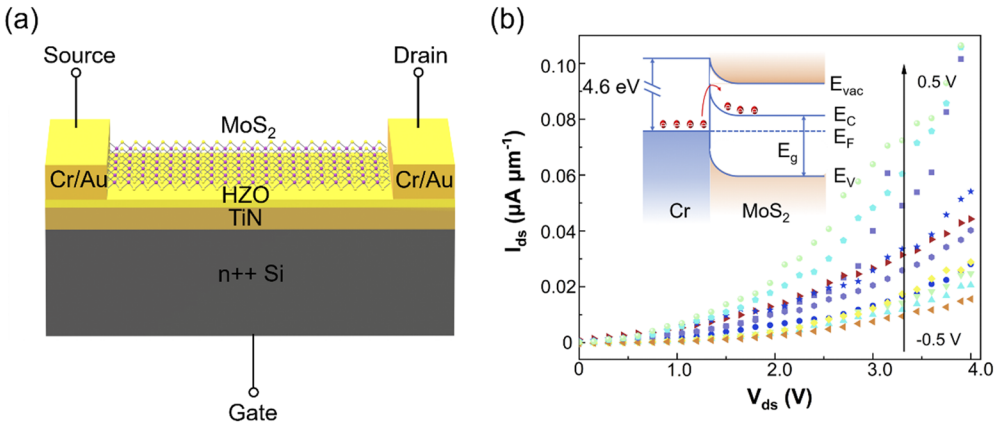


FIG. 3. (a) The schematic diagram of MoS_2/HZO FETs and (b) $I_{ds} - V_{ds}$ of MoS_2 FETs with a channel length of 20 μm and width of 100 μm. V_{gs} ranges from −0.5 to 0.5 V with a step of 0.1 V, and the inset is the band diagram at the Schottky barrier, where E_{vac} is the vacuum level; E_C, E_F, and E_V are the energy of the conductive band, Fermi level, and valence band, respectively; and E_g is the bandgap of MoS_2.

of only ~0.3 V, which demonstrated the stable V_{th} of the MoS_2/HZO FETs. Based on the $I_{ds} - V_{gs}$ curves, the field effect mobility of the devices could be measured by

$$\mu = \frac{dI_{ds}}{dV_{gs}} \times \frac{L}{WC_iV_{ds}}, \quad (1)$$

where L and W are the channel length and width, respectively, and C_i is the dielectric capacitance per unit area ($C_i = \varepsilon_0\varepsilon_r/d$, where ε_r = 24.5 and d = 10 nm).[25] The mobility of the FETs could be extracted from the data presented in Fig. 4(a) and calculated to be 0.38 $cm^2\ V^{-1}\ s^{-1}$, which is in good agreement with the previously reported carrier mobility of devices based on CVD MoS_2.[26,27] It was noticed that only the non-saturated region was measured in both the output and transfer characteristics of the FETs due to a relatively low breakdown voltage (at V_{gs} = 4.5 V) of the ultra-thin HZO gate dielectrics.

A hysteresis loop in the MoS_2/HZO FETs was also observed and investigated. This phenomenon could be possibly attributed to the intrinsic trapping in MoS_2, the adsorption of moisture and O_2 of MoS_2, the interface effect, and/or the fabrication process of the devices.[28–31] With multiple cycles on the same device, the hysteresis loop remained in the $I_{ds} - V_{gs}$ curve [Fig. 4(b)]. This suggests that the fixed charge that originated from the defects at the MoS_2/HZO interface is a probable origin contributing to the hysteresis.[32,33] It is known that in the dielectric layer, the charge trapping/detrapping process and their dynamics depend on the capture and emission time of the carriers. As the charging time is longer than the releasing time with V_{gs} sweeping from positive to negative, injected carriers in the defects reached a dynamic equilibrium, which resulted in the observed hysteresis loop.

In order to further understand the contribution of the dielectric layer to the device characteristics, the crystallinity of the HZO thin film was also characterized by GIXRD. The result was shown in Fig. 5. It can be seen that in addition to the TiN Bragg peaks that

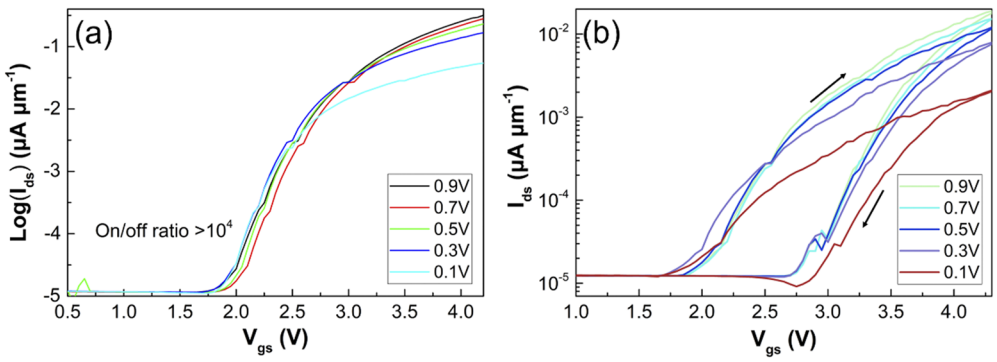


FIG. 4. (a) $I_{ds} - V_{gs}$ transfer characteristics with V_{ds} ranging from 0.1 to 0.9 V with a step of 0.2 V. The on/off ratio of the devices was measured to be $>10^4$. (b) $I_{ds} - V_{gs}$ of the MoS_2 FET with a channel length 20 μm and a width of 100 μm, with V_{gs} ranging from 0.1 to 0.9 V.

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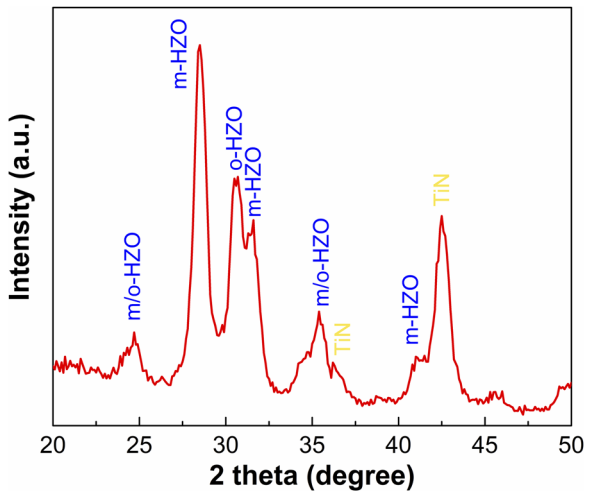


FIG. 5. Lattice structure of the HZO nanolayer measured by GIXRD. The characteristic peaks of the o-HZO were observed, but the m-phase is more dominating.

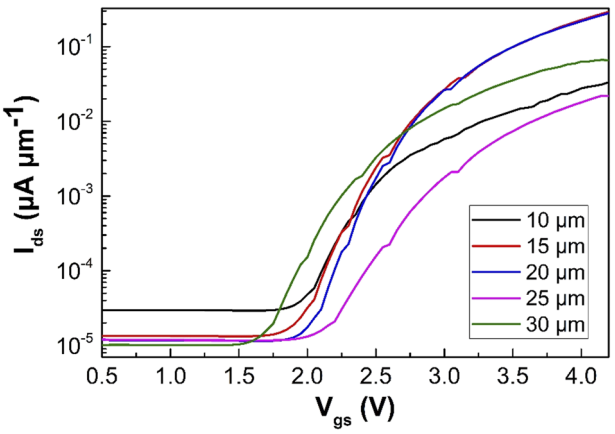


FIG. 6. $I_{ds} - V_{gs}$ of the MoS_2 FET with the channel lengths varying from 10 to 30 μm with a step of 5 μm and V_{ds} = 0.7 V.

appear at $2\theta = 36.2^\circ$ and 42.5°, six Bragg reflections appear, corresponding to the HZO layer. It is known that the diffraction peak at $2\theta = 30.5^\circ$ corresponds to the orthorhombic (o) phase, which is related to the ferroelectricity in HZO. However, it is evident that the monoclinic (m) phase (Bragg peaks at $2\theta = 24.7^\circ$, 28.5°, 31.6°, 35.4°, and 41.0°) is dominating in the diffraction pattern.

It has been widely reported that the formation of the o-phase in HZO requires the tensile stress from the TiN electrodes, both on the top and at the bottom, in the sandwich structure. One of our previous works has proved the ferroelectricity in the 10 nm-thick HZO film with a TiN (50 nm)/HZO (10 nm)/TiN (50 nm) sandwich structure.[25] It is noted here that the observed hysteresis in the $I_{ds} - V_{gs}$ curves of MoS_2/HZO FETs that originated from the fixed charge and ferroelectricity in the HZO nanolayer has the opposite direction, which might induce neutralization of the hysteresis.[34] However, in our case, as observed in Fig. 3(b), the clockwise hysteresis is still dominated by charge trapping in the transistor.

It has to be noted that the HZO layers used in our FETs were fabricated without top-layer stressors, which probably consequently led to weak ferroelectricity in HZO layers and resulted in partial neutralization. Despite this, the HZO film is still promising in FETs, thanks to its high-k property and ultra-thin structure.

The channel length impact of the MoS_2/HZO FETs was then investigated. $I_{ds} - V_{ds}$ transfer curves were measured for devices with different channel lengths. The results are shown in Fig. 6. Because the channel lengths in the MoS_2/HZO FETs are >10 μm and much larger than the electron mean free path, the carriers in the channel operate in diffusion regimes. The carrier mobility of the devices remains constant in long channel devices, and the current in the FETs is mainly contributed by the channel resistance and electrode resistance. It can be seen in Fig. 6 that I_{ds} initially increases with the increase in the channel length and then reaches the highest value when the channel length is 20 μm. A significant drop in the current was observed on further increasing the channel length, which could have resulted from the high resistance of the long channel devices. With the decrease in the channel length in the MoS_2, the device with a length to width ratio of 0.2 shows a superior performance.

IV. CONCLUSION

In conclusion, we have successfully fabricated the MoS_2-based back-gate FETs with CVD MoS_2 and an HZO high-k dielectric gate. The electrical properties of devices with channel lengths ranging from 10 to 30 μm with a step of 5 μm have been studied in detail. The channel length to width ratio of 0.2 was proved to lead to the highest performance, i.e., a high on/off ratio of $>10^4$ and a field effect mobility of 0.38 cm^2 V^{-1} s^{-1}. A stable V_{th} of ~1.5 V was achieved in our MoS_2/HZO FETs. A hysteresis loop was also observed in the $I_d - V_{ds}$ curves of MoS_2/HZO FETs, which were carefully discussed and attributed to the intrinsic trap and adsorbates of MoS_2 as well as the interfacial fixed charge. Further studies will focus on the optimization of the devices, including the improvement of the quality of the MoS_2, and the optimization of the dielectrics as well as the minimization of the charge effect in FETs. Short channel devices based on MoS_2 and ferroelectric HZO materials will also be further studied for future high speed, high on/off ratio, and low power consumption devices.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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