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# Restricted Channel Migration in 2D Multilayer ReS<sub>2</sub>

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**Abstract:** When the thickness-dependent carrier mobility is coupled with Thomas-Fermi screening and interlayer resistance effects in two-dimensional (2D) multilayer materials, a conducting channel migrates from the bottom surface to the top surface under electrostatic bias conditions. However, numerous factors including i) an insufficient carrier density, ii) atomically thin material thickness, and iii) numerous oxide trap/defects considerably limit our deep understanding of the carrier transport mechanism in 2D multilayer materials. Herein, we report the restricted conducting channel migration in a 2D multilayer  $\text{ReS}_2$  after a constant voltage stress of the gate dielectrics is applied. At a given gate bias condition, a gradual increase in the drain bias enables a sensitive change in the interlayer resistance of  $\text{ReS}_2$ , leading to a modification of the shape of the transconductance curves, and consequently demonstrates the conducting channel migration along the thickness of the  $\text{ReS}_2$  before the stress. Meanwhile, this distinct conduction feature disappears after stress, indicating the formation of additional oxide trap sites inside the gate dielectrics that degrade the carrier mobility and eventually restrict the channel migration. Our theoretical and experimental study based on the resistor network model and Thomas–Fermi charge screening theory provides further insight into the origins of channel migration and restriction in 2D multilayer devices.

## INTRODUCTION

Among numerous two-dimensional (2D) van der Waals (vdW) layered materials, a distorted octahedral (1T') rhenium disulfide (ReS<sub>2</sub>) multilayer provides unique properties such as anisotropic in-plane carrier transport,<sup>1-4</sup> a thickness-independent direct bandgap at approximately 1.5 eV,<sup>5,6</sup> and weak interlayer coupling.<sup>5,7</sup> These intrinsic properties of ReS<sub>2</sub> allow various applications such as a field-effect transistor,<sup>1,3,8,9</sup> tunneling diode,<sup>10-12</sup> logic device,<sup>4,13,14</sup> and phototransistor with excellent responsivity, absorption efficiency, and detectivity to be demonstrated.<sup>15-17</sup> In particular, the strongly decoupled interlayer interaction in the multilayer ReS<sub>2</sub> leads to a relatively larger interlayer resistivity ( $\sim 10^5 \Omega \cdot \mu\text{m}$ )<sup>18</sup> than that of other 2D transition metal dichalcogenide materials such as MoS<sub>2</sub> ( $\sim 10^3 \Omega \cdot \mu\text{m}$ )<sup>19,20</sup> and graphite ( $\sim 10^2 \Omega \cdot \mu\text{m}$ ),<sup>20</sup> rendering this multilayer ReS<sub>2</sub> an ideal platform for studying the carrier transport mechanism among other 2D vdW multilayer materials. When this interlayer energy barrier is coupled with the thickness-dependent carrier mobility and Thomas–Fermi screening effects in 2D multilayer materials, it has been theoretically and experimentally demonstrated that a conducting channel migrates from the bottom surface to the top surface under electrostatic bias conditions,<sup>3,19,20</sup> which is in clear contrast to their Si bulk counterparts where its inversion channel centroid exhibits nearby gate dielectrics.<sup>3,21,22</sup>

For example, Das et al. systematically reported a non-monotonic thickness-dependent carrier mobility with respect to different metal electrodes ascribing to the Thomas–Fermi charge screening and interlayer coupling in MoS<sub>2</sub> multilayers.<sup>19,20</sup> In addition, Shim and Moon et al. investigated systematically the thickness-dependent optoelectronic properties of ReS<sub>2</sub> thin film transistors,<sup>14,16</sup> and Lee and Kim et al. probed the effects of interlayer tunneling barrier effects on the current fluctuation in a multilayer ReS<sub>2</sub> transistor with respect to the top and bottom surfaces.<sup>3,21</sup> Furthermore, Goyal et al. demonstrated a feasible memory

application using few-layer ReS<sub>2</sub> transistors upon the observance of two plateaus in its transconductance curves.<sup>23</sup> Nevertheless, this genetic carrier transport mechanism of a 2D multilayer platform has not been extensively explored because of i) an insufficient electrostatic vertical electric field or minimum accumulated carrier density necessary to observe the conducting channel redistribution, ii) an atomically thin material thickness limiting the spatial channel migration, and iii) numerous oxide trap/defect sites degrading carrier mobility. These experimental constraints considerably prevent our full understanding of the carrier transport mechanism in 2D multilayer materials, consequently implying the importance of the thickness of such materials and the degree of the interlayer energy barrier, which relies strongly on the electrostatic drain ( $V_D$ ) and gate ( $V_{BG}$ ) bias conditions to achieve a clear insight into the distinct carrier transport mechanism in multiple 2D layers.

Herein, we report the restricted drain bias-dependent conducting channel migration in a 2D multilayer ReS<sub>2</sub> device by presenting i) the presence of two plateaus and their shape modification in the transconductance ( $g_m$ ), and ii) a variation of the turn-on voltage ( $V_T$ ) shift with respect to the top and bottom channels as a function of the drain voltage before and after electrical stress at  $V_{BG} = 60$  V for 40,000 s. Within a small  $V_D$  regime of 20 to 100 mV, the channel centroid migration is clearly observed before the  $V_{BG}$  stress, whereas the channel centroid is mostly confined within the multilayer ReS<sub>2</sub> after the  $V_{BG}$  stress, masking the formation of the conducting channel near the degraded gate dielectrics. Meanwhile, as  $V_D$  increases, the separated top- and bottom-channel combines together regardless of the stress. The degradation in carrier mobility after the electrical stress further supports the presence of additional oxide trap sites, which hampers the channel formation at the bottom layers, consequently leading to a restricted channel migration. Our numerical resistor network calculation, which considers the Thomas–Fermi screening effect and interlayer resistance,

further rationalizes this anomalous carrier transport feature in a 2D multilayer ReS<sub>2</sub>.

## RESULTS AND DISCUSSION

To achieve a clear insight regarding the physical origin of channel migration and restriction in 2D multilayer devices, we first consider the resistor network model and Thomas–Fermi charge screening theory, as illustrated conceptually in Figure 1a, for a pristine ReS<sub>2</sub> device.

The thickness-dependent effective carrier mobility ( $\mu_i$ ) corresponding to a certain layer thickness ( $i^{\text{th}}$  layer of 2D vdW multilayer materials) has been described by

$\mu_i = \mu_1 + (\mu_\infty - \mu_1) \left( 1 - \exp\left(-\frac{(i-1)t_{\text{Int}}}{\lambda_{\text{TF}}}\right) \right)$ ,<sup>19,20</sup> where  $\mu_1$  ( $= 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ),<sup>1</sup>  $\mu_\infty$  ( $= 200 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ),<sup>13,24</sup> and  $t_{\text{Int}}$  ( $= 0.65 \text{ nm}$ ) are the monolayer mobility of ReS<sub>2</sub>, bulk carrier mobility of ReS<sub>2</sub>, and interlayer distance, respectively. Such an anomalous carrier mobility enhancement along the thickness (up to 10 nm) at the given  $V_{\text{BG}}$  and  $V_{\text{D}}$  conditions for the  $i^{\text{th}}$  layer of a 2D multilayer system can mainly be ascribed to the presence of fixed oxide charges inside the dielectrics and charged Coulomb impurities on the bottom and/or top surfaces of the 2D materials, in addition to an interlayer resistance and the effects of the Thomas-Fermi screening.<sup>13,16,25,26</sup> The thickness-dependent carrier mobility of multilayer ReS<sub>2</sub> is presented elsewhere, including our previous report.<sup>16,27</sup> The Thomas–Fermi charge screening length

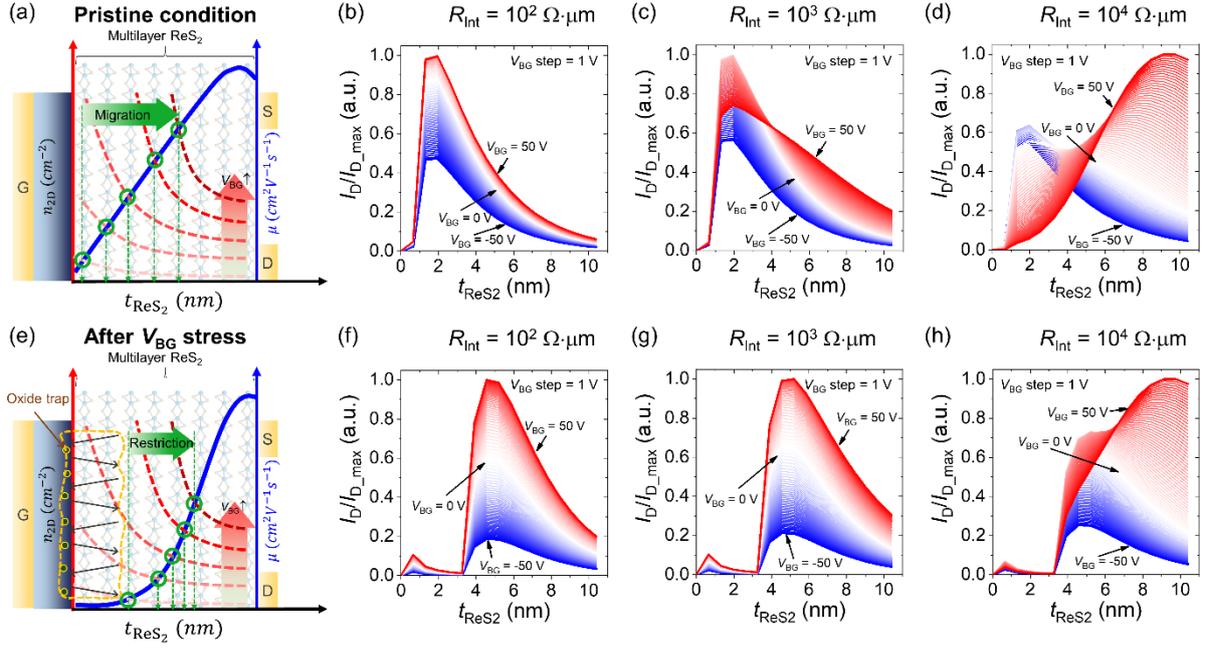
( $\lambda_{\text{TF}} = \sqrt{\left(\frac{\epsilon_{\text{ReS}_2}}{\epsilon_{\text{SiO}_2}}\right) t_{\text{ReS}_2} t_{\text{SiO}_2}}$ , where  $\epsilon_{\text{ReS}_2}/\epsilon_{\text{SiO}_2}$  ( $= 7/3.9$ )<sup>28</sup> and  $t_{\text{ReS}_2}/t_{\text{SiO}_2}$  ( $= 11 \text{ nm}/90 \text{ nm}$ ) denote the dielectric constant and thickness of ReS<sub>2</sub>/SiO<sub>2</sub>, respectively.) used in our multilayer ReS<sub>2</sub> is  $\approx 42 \text{ nm}$ , which is much thicker than the  $t_{\text{ReS}_2}$  in this study, implying the proper thickness range of the ReS<sub>2</sub> in the vertical direction. The much smaller value of  $\lambda_{\text{TF}}$  than  $L_{\text{ReS}_2}$  allows a negligible contribution of the fringing field effect on the oxide planar capacitance ( $C_{\text{OX}}$ ).<sup>19,20</sup> In addition, provided that we obtain the charge density of the  $i^{\text{th}}$  layer

( $Q_i$ ) by taking into account  $\lambda_{\text{TF}}$  and the screened Coulomb potential of the  $i^{\text{th}}$  layer according to the Thomas–Fermi screening theory, the conductivity ( $\sigma_i = Q_i \times \mu_i$ ) and conductance ( $G_i = \sigma_i \times (W/L)$ , where  $W$  and  $L$  are the channel width and length, respectively) can be determined for each layer, enabling the visualization of which layer is the most conducting layer inside the multilayer ReS<sub>2</sub>.<sup>3,19</sup> Based on the resistor network model, the drain current contribution of the  $i^{\text{th}}$  layer ( $I_{\text{D}}^i$ ) to the total drain current ( $= \sum_i I_{\text{D}}^i$ ) can be confirmed under the boundary condition of the interlayer resistivity of ReS<sub>2</sub> ( $R_{\text{Int}} = 10^5 \Omega \cdot \mu\text{m}$ ). This  $R_{\text{Int}}$  range of ReS<sub>2</sub> was further supported by the voltage-dependent current obtained from a 12-nm thick ReS<sub>2</sub> *via* conductive-AFM (c-AFM) using a Pt-coated tip (= 25 nm) (see Figure S1 in the Supporting Information (SI)). As  $V_{\text{BG}}$  increases, the channel that exhibits the highest conductivity in the layers migrates from the bottom surface to the top surface of the ReS<sub>2</sub> in a conventional back-gate configuration mainly owing to the interplay between  $R_{\text{Int}}$  and  $\lambda_{\text{TF}}$ , mirroring the  $V_{\text{BG}}$ -dependent spatial channel modification. This is a distinct feature in comparison with monolayer and conventional 3D bulk semiconductor systems. A more detailed explanation of this theoretical approach is described elsewhere.<sup>3,19,21</sup>

The numerically calculated  $R_{\text{Int}}$ -dependent current distribution profile along the thickness of ReS<sub>2</sub> as a function of  $V_{\text{BG}}$  after the maximum current normalization for each layer is displayed in Figures 1b-d display, where  $I_{\text{D\_max}}$  is the maximum  $I_{\text{D}}$  among  $I_{\text{D}}^i$ . Here, we take the variable  $R_{\text{Int}}$  into account our calculation ranging from  $10^2$  to  $10^4 \Omega \cdot \mu\text{m}$  for a deeper understanding of channel migration in 2D multilayer. When  $R_{\text{Int}}$  is  $10^2 \Omega \cdot \mu\text{m}$ , the significant channel migration is not observed clearly, although the relative volume of top-channel expands slightly (see Figure 1b). However, when  $R_{\text{Int}}$  is larger than  $10^3 \Omega \cdot \mu\text{m}$  (see Figures 1c-d), the conducting channel centroid tends to move upward to exclude large contribution of  $R_{\text{Int}}$  in its total resistance of ReS<sub>2</sub> with the increasing  $V_{\text{BG}}$ , implying clearly that the enhanced

contribution of top-channel to the total current comparing to that of bottom-channel. In addition, this fact further suggests that this distinct channel migration can be tuned by  $V_D$  because of  $R_{\text{Int}}$  (or the interlayer tunneling barrier height) reliance on  $V_D$  in addition to  $V_{\text{BG}}$ . These results clearly demonstrate the importance role of  $R_{\text{Int}}$  in the transport mechanism of 2D vdW multilayers.

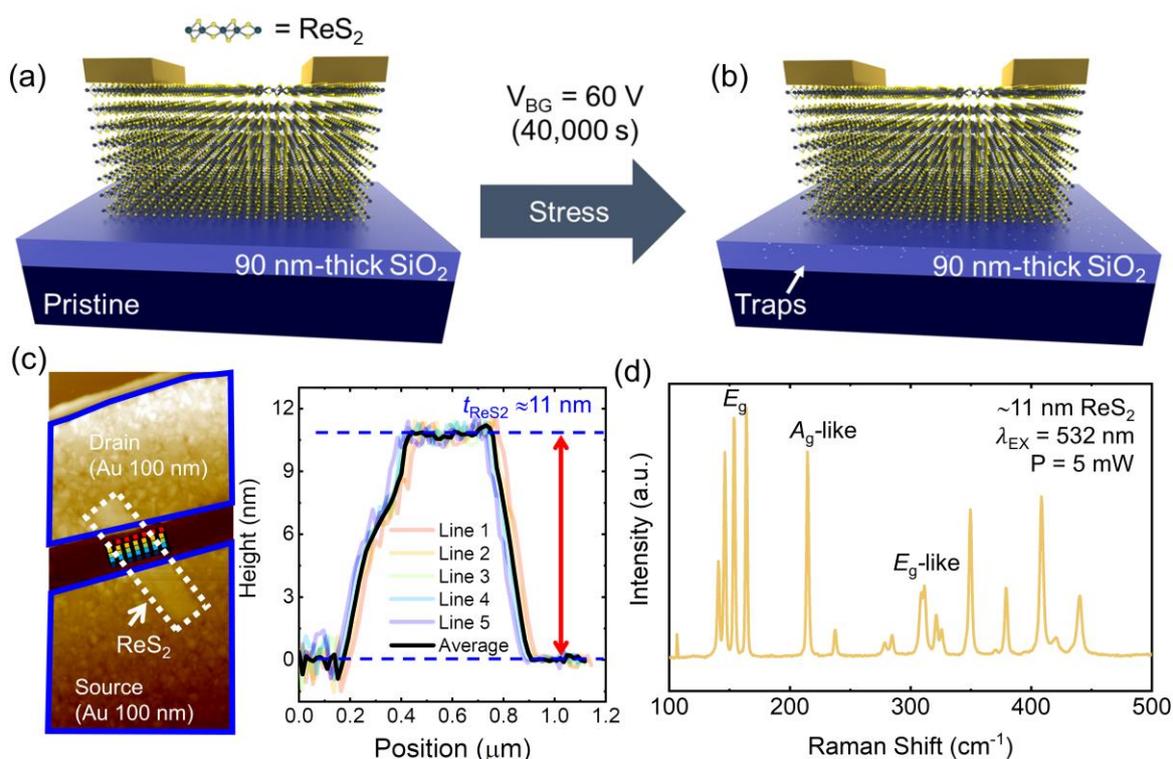
Next, we investigate the restricted channel migration in 2D vdW multilayers by assuming that the carrier mobility is degraded by the electrical  $V_{\text{BG}}$  stress, as illustrated in Figure 1e. The additional oxide trap sites created inside the dielectrics considerably reduces  $\mu_i$  and suppresses  $Q_i$  for the bottom layers in particular,<sup>25,29-31</sup> hampering the bottom channel formation inside the multilayer  $\text{ReS}_2$ , and consequently leading to a restricted spatial channel migration. Figures 1f-h further support this restriction, which is obtained from our numerical calculation by taking the degradation of the carrier mobility into account as a function of  $R_{\text{Int}}$ . Herein, we simply assume  $\mu_1 - \mu_5 (= 0.5 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1})$  and  $\mu_\infty (= 200 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1})$  to reflect the effects of the oxide trap. It has been reported that the electrical  $V_{\text{BG}}$  stress degrades the oxide quality by creating undesired oxide trap/defect inside the dielectrics.<sup>31-34</sup> This oxide degradation is often linked to a gate dielectric break down, a severe malfunction of the analog/digital circuit, and the life time of the memory. Understanding the effects of the oxide quality degradation on this distinct 2D carrier transport is essential for employing various 2D materials as next-generation logic devices and optoelectronics.



**Figure 1. Conducting channel migration and restriction in 2D multilayer ReS<sub>2</sub>.** (a) Conceptual illustration of conducting channel migration as a function of  $V_{\text{BG}}$  at a given thickness-dependent carrier mobility  $\mu$ . Numerical simulation results for current distribution along the  $c$ -axis of ReS<sub>2</sub> as a function of  $R_{\text{Int}}$ ; (b)  $R_{\text{Int}} = 10^2 \Omega \cdot \mu\text{m}$ , (c)  $R_{\text{Int}} = 10^3 \Omega \cdot \mu\text{m}$ , and (d)  $R_{\text{Int}} = 10^4 \Omega \cdot \mu\text{m}$ . (e-h) Corresponding panels after electrical  $V_{\text{BG}}$  stress. (e) Illustration of restricted channel migration after  $V_{\text{BG}}$  stress. The oxide trap sites created degrade the carrier mobility, particularly at the bottom layers, which hampers the formation of the bottom channel.  $R_{\text{Int}}$ -dependent current distribution after the  $V_{\text{BG}}$  stress in terms of (f)  $R_{\text{Int}} = 10^2 \Omega \cdot \mu\text{m}$ , (g)  $R_{\text{Int}} = 10^3 \Omega \cdot \mu\text{m}$ , and (h)  $R_{\text{Int}} = 10^4 \Omega \cdot \mu\text{m}$ .

To study this anomalous feature of multilayer ReS<sub>2</sub>, we fabricated an 11-nm thick 1T' multilayer ReS<sub>2</sub> transistor onto a 90-nm thick SiO<sub>2</sub>/p<sup>+</sup>-Si substrate and investigated the variation of the carrier transport mechanism before and after applying electrical stress at  $V_{\text{BG}} = 60$  V for 40,000 s with a zero-drain and source bias, as illustrated in Figures 2a and b, respectively. The fabricated device was thermally annealed for 3 h at 473 K under a high vacuum condition ( $\approx 10^{-6}$  Torr). A detailed description of the device fabrication is presented in the Experimental Section. The various geometrical parameters of the pristine multilayer ReS<sub>2</sub>, such as  $L$  ( $\approx 1 \mu\text{m}$ ),  $W$  ( $\approx 0.614 \mu\text{m}$ ), and  $t_{\text{ReS}_2}$  ( $\approx 11$  nm) were confirmed using an atomic

force microscope (AFM) (see Figure 2c). The negligible thickness difference at the whole channel confirmed by AFM clearly demonstrates a uniform thickness of our ReS<sub>2</sub>. The optical Raman spectrum obtained from 11-nm thick ReS<sub>2</sub> under ambient conditions using a laser excitation wavelength of 532 nm ( $\lambda_{\text{EX}}$ ) with 5 mW of power (P) is shown in Figure 2d. The dominant  $E_g$  ( $\approx 150 \sim 160 \text{ cm}^{-1}$ ),  $A_{1g}$ -like ( $\approx 215 \text{ cm}^{-1}$ ), and  $E_g$ -like ( $\approx 312 \text{ cm}^{-1}$ ) are clearly observed, which is consistent with previous reports.<sup>5,16</sup>



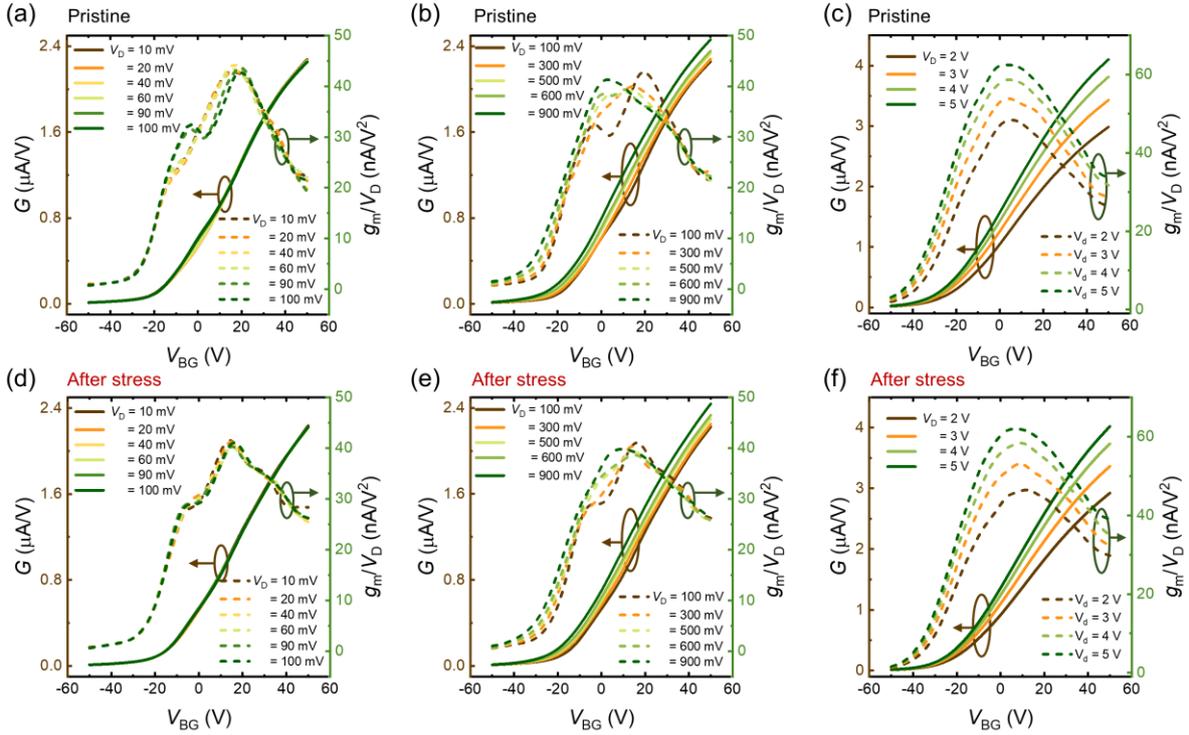
**Figure 2. Device structure and optical Raman property of 2D multilayer ReS<sub>2</sub>.** Cross-sectional view of a multilayer ReS<sub>2</sub> transistor in (a) pristine state and (b) after  $V_{\text{BG}}$  stress. (c) AFM topography image of multilayer ReS<sub>2</sub> fabricated on SiO<sub>2</sub>. The thickness profiles along the numerous lines are displayed in the right inset. (d) Raman spectrum of 11-nm-thick ReS<sub>2</sub> flake on SiO<sub>2</sub> substrate measured at  $\lambda_{\text{EX}} = 532 \text{ nm}$  with  $P = 5 \text{ mW}$ .

The two-probe measured  $V_{\text{BG}}$ -dependent conductance ( $G = I_{\text{D}}/V_{\text{D}}$ ) curves of the pristine ReS<sub>2</sub> transistor clearly represent a typical  $n$ -type behavior, in which the populated electrons are visible with increasing  $V_{\text{BG}}$  (see Figures 3a–c) regardless of  $V_{\text{D}}$ . To further reveal the

physical implications of  $V_D$ -dependent  $G$  curves, the corresponding  $g_m$  ( $=\partial I_D/\partial V_{BG}$ ) normalized by  $V_D$  ( $=g_m/V_D$  or  $\partial G/\partial V_{BG}$ ) curves are directly compared in the same panel. In principle, the  $G$  (or  $g_m/V_D$ ) curves obtained should be identical regardless of  $V_D$  when there is a negligible metal-to-ReS<sub>2</sub> Schottky barrier, particularly for very small  $V_D$  regimes.<sup>21</sup> This feature is observed in our multilayer ReS<sub>2</sub> device. However, as  $V_D$  increases from 10 to 100 mV (see Figure 3a), two plateaus are clearly exhibited in the  $g_m/V_D$  curve at near  $V_D = 100$  mV, implying the emergence of channel migration, which was mainly triggered by the increasing  $V_D$ , as previously described (see Figures 1a–d). Indeed, the double enhancement of  $g_m$  has been interpreted as the coexistence of a different conduction mechanism, e.g., MoS<sub>2</sub>/Gr heterointerface transistors<sup>35,36</sup>, double-gate silicon-on-insulator transistors<sup>37</sup>, and Si junction-less transistors<sup>38,39</sup>. Moreover, the two peaks observed for the  $g_m/V_D$  curve are gradually merged (see Figure 3b), which is further broadened and extended with an increase in  $V_D$  (see Figure 3c). This  $V_D$  dependency in the observed  $g_m/V_D$  indicates the suppression of  $R_{int}$ , resulting in a channel migration and carrier mobility enhancement, particularly at high  $V_D$  regimes. This observation is in clear contrast to the conventional short-channel effects in Si transistors driven by the drain-induced-barrier-lowering, which degrades the carrier mobility in high  $V_D$  regimes.<sup>40</sup>

This anomalous signature indicating a channel migration is significantly suppressed after the electrical  $V_{BG}$  stress, particularly in small  $V_D$  regimes (see Figure 3d). The  $V_{BG}$ -dependent  $G$  and  $g_m/V_D$  curves are almost identical to each other regardless of  $V_D$ , mirroring the spatially limited channel migration in the observed small  $V_D$ . The oxide traps created in the SiO<sub>2</sub> under the  $V_{BG}$  stress degrade the carrier mobility and suppress the available free electrons inside ReS<sub>2</sub>, which makes the bottom-channel formation difficult, consequently leading to a restricted channel migration, as we previously demonstrated (see Figures 1e–h). Nevertheless,

in high  $V_D$  regimes, the observed  $g_m/V_D$  after the  $V_{BG}$  stress demonstrates features similar to those of pristine ReS<sub>2</sub> (see Figures 3e and f), implying the stronger contribution of damaged oxide traps to the bottom channel formation rather than the top channel formation inside the ReS<sub>2</sub>. In addition, the narrower distance of  $V_{BG}$  between the first and second maximum  $g_m/V_D$  after the  $V_{BG}$  stress also demonstrates the limited spatial channel migration.



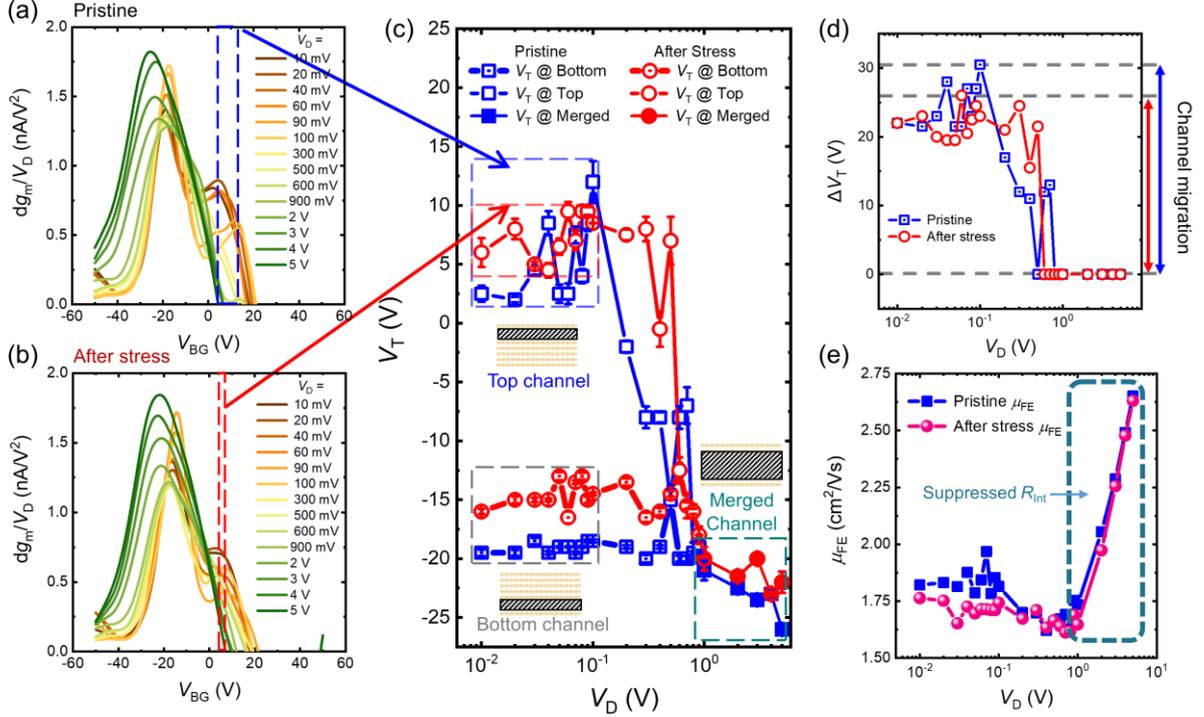
**Figure 3. Electrical properties of 2D multilayer ReS<sub>2</sub>.** (a–c)  $V_D$ -dependent  $G$  ( $= I_D/V_D$ , the solid lines with the left y-axis) and  $g_m$  normalized by  $V_D$  curves ( $= g_m/V_D$ , the dotted lines with the right y-axis) under pristine condition at (a)  $10 \text{ mV} \leq V_D \leq 100 \text{ mV}$ , (b)  $100 \text{ mV} \leq V_D \leq 900 \text{ mV}$ , and (c)  $2 \text{ V} \leq V_D \leq 5 \text{ V}$ , respectively. (d–e) The corresponding results after the  $V_{BG}$  stress at (d)  $10 \text{ mV} \leq V_D \leq 100 \text{ mV}$ , (e)  $100 \text{ mV} \leq V_D \leq 900 \text{ mV}$ , and (f)  $2 \text{ V} \leq V_D \leq 5 \text{ V}$ , respectively.

To qualitatively discuss the channel migration and restriction, the turn-on voltage ( $V_T$ ) for the bottom and top channels of the multilayer ReS<sub>2</sub> was determined using the second-derivative of the current method ( $dg_m = \partial g_m / \partial V_{BG}$ ) before and after the  $V_{BG}$  stress (see Figures 4a and b).<sup>41</sup> In these figures, when  $V_D$  is less than 100 mV, owing to the existence of two clear

humps of  $g_m$ , the first and second maximum  $dg_m$  peaks of the pristine ReS<sub>2</sub> (after the  $V_{BG}$  stress) clearly appear at  $V_{BG} \approx -18.5$  V ( $V_{BG} \approx -14.5$  V) and  $2.5$  V  $\leq$   $V_{BG} \leq$   $12$  V ( $4.5$  V  $\leq$   $V_{BG} \leq$   $9.5$  V), respectively. However, as  $V_D$  increases, both peaks gradually merge together and eventually exhibit a single  $dg_m$  peak at  $V_D$  higher than  $100$  mV (see Figure 4c), manifesting a broadening channel inside the multilayer ReS<sub>2</sub> by combining the top and bottom channels. The upshifted  $V_T$  after the  $V_{BG}$  stress particularly for the bottom channel mirrors the additionally created trap density to be filled, i.e.,  $C_{OX}/q \times (5$  V)  $\approx 1.2 \times 10^{12}$  cm<sup>-2</sup>, where  $q$  denotes the electronic unit charge and consequently limits the total channel migration distance along the  $c$ -axis of the ReS<sub>2</sub>. The irreversible conductance and enhancement of gate leakage current after the electrical stress and recovery further support this observation as displayed in Figure S2 in the Supporting Information. We further note that taking into account of our device configuration ( $p^+$ -Si/SiO<sub>2</sub>/ $n^+$ -ReS<sub>2</sub>/Au), the established electric field should be mainly focused on SiO<sub>2</sub> (i.e., the most resistive (or capacitive) element), implying a negligible Joule heating effect of current on our ReS<sub>2</sub>.

Moreover, the abrupt change in the difference in  $V_T$  observed between the top and bottom channels ( $\Delta V_T$ ) after the  $V_{BG}$  stress rationalizes the limited channel migration (see Figure 4d). Figure 4e displays the field-effect mobility ( $\mu_{FE} = g_m \cdot (L/W) \cdot C_{OX}^{-1} \cdot V_D^{-1}$ ) determined from the maximum value of  $g_m$  for both cases. Because of the additional oxide trap sites created, the  $\mu_{FE}$  of pristine ReS<sub>2</sub> obtained is always larger than that of the stressed sample when  $V_D$  is less than  $1$  V. However, this observed difference in  $\mu_{FE}$  mostly vanishes as  $V_D$  further increases ( $V_D > 1$  V), reflecting the suppressed contribution of  $R_{Int}$  and the oxide trap sites to  $\mu_{FE}$  and supporting the channel migration along the  $c$ -axis of the multilayer ReS<sub>2</sub>. The  $I_D$ - $V_D$  output characteristic and output transconductance curves as a function of  $V_{BG}$  further confirm this channel migration and carrier mobility enhancement (see Figure S3 in SI). This fact further

implies that the observed degradation of  $\mu_{FE}$  is exclusively dominant for the bottom-channel of the ReS<sub>2</sub>, leading us to conclude that there is a negligible stress effect on the ReS<sub>2</sub> channel itself comparing to that of SiO<sub>2</sub>.



**Figure 4. Turn-on voltage determination and carrier mobility enhancement.**  $V_D$  normalized  $V_{BG}$ -dependent  $dg_m$  curves (a) before and (b) after the  $V_{BG}$  stress. Blue and red regions represent the second  $dg_m$  peak position in both cases as a function of  $V_D$ . (c)  $V_D$ -dependent  $V_T$  corresponding to top- and bottom-channels determined from the first and second maximum  $dg_m$  peak position, respectively. As  $V_D$  increases, the top- and bottom-channels merge together, and exhibit a single  $dg_m$  peak particularly when  $V_D$  is larger than 1 V. (d)  $V_T$  differences between the  $V_T$  obtained in Figure 4c as a function of  $V_D$  for both cases. (e)  $V_D$ -dependent  $\mu_{FE}$  before (blue rectangular) and after (purple circle) the  $V_{BG}$  stress.

## CONCLUSION

We clearly demonstrate the electric field-dependent conducting channel migration in 2D multilayer ReS<sub>2</sub> and its spatial restriction after  $V_{BG}$  stress is applied. The  $V_D$ - and  $V_{BG}$ -dependent  $R_{Int}$  enables modulating the position of the maximum conducting channel along the  $c$ -axis of the ReS<sub>2</sub>, which is further rationalized by the numerical calculation results by taking

into account the resistor network model and Thomas–Fermi charge screening theory. The oxide trap sites created after the occurrence of  $V_{BG}$  stress significantly degrades the carrier mobility and hampers the formation of the bottom channel inside the  $\text{ReS}_2$ , resulting in a restricted channel migration. However, as  $V_D$  increases, the contribution of  $R_{\text{int}}$  to the total carrier transport is considerably suppressed regardless of the  $V_{BG}$  stress, which consequently facilitates the channel migration toward the top channel and broadens the channel inside the multilayer  $\text{ReS}_2$  by combining the top and bottom channels. This fact clearly indicates the stronger effects of the damaged oxide traps on the bottom channel formation rather than the top channel formation inside the  $\text{ReS}_2$ . Our findings will be of significant help in the development of next-generation semiconductor electronic devices using 2D multilayer materials and will deepen our understanding of their charge transport behavior.

## **METHODS**

### **Device Fabrication**

Micromechanically exfoliated 1T' multilayer  $\text{ReS}_2$  (purchased from 2D Semiconductors) flakes were first transferred onto a 90-nm  $\text{SiO}_2/p^+$ -Si substrate using a conventional scotch type method. After finding an optimal  $\text{ReS}_2$  flake with a thickness of  $\sim 11$  nm using AFM (Nx-10, Park Systems), selective electron-beam lithography (MIRA3, TESCAN) was carried out to define the dimensions of the channel and electrodes. Au ( $\approx 100$  nm) metal was deposited using an electron-beam evaporator (INFOVION). The geometrical channel length ( $\approx 1$   $\mu\text{m}$ ) and width ( $\approx 0.614$   $\mu\text{m}$ ) were also confirmed using AFM and an optical microscope (BX53M, Olympus). The optical Raman spectrum of a  $\text{ReS}_2$  flake with a thickness of  $\approx 11$  nm was acquired using a LabRam ARAMIS IR2 system with a 532-nm laser source at a power of 5 mW. The frequency range used was 100–500  $\text{cm}^{-1}$  at room temperature.

## **Electrical Characterization**

All electrical measurements were conducted after an annealing process at 200 °C for 10 h in a high vacuum metal chamber ( $\approx 10^{-6}$  Torr) using a commercial semiconductor characterization system (B1500A Keysight /4200-SCS Keithley). The fabricated ReS<sub>2</sub> device was first placed in a vacuum probe station. The transfer and output characteristic curves of the pristine ReS<sub>2</sub> device were obtained as a function of the  $V_D$  (from 10 mV to 5 V) and  $V_{BG}$  (from -50 V to 50 V) at room temperature. A constant  $V_{BG}$  of 60 V was then applied to the ReS<sub>2</sub> for 40,000 s to create numerous trap sites in the SiO<sub>2</sub>. We repeated the same measurements to obtain the transfer and output characteristic curves after the stress was applied.

## **DATA AVAILABILITY**

Data are available upon request.

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## **AUTHOR CONTRIBUTIONS**

C.K. and M.-K.J. conceived and developed the study under the guidance of G.T.K. C.K., S.Y.K., Y.K., and Y.S. fabricated the device. C.K., M.S., B.C.L., and C.T. conducted the electrical measurements and characterized the data. D.K. and Y.K. analyzed the optical Raman properties. C.K., M.-K.J., and G.T.K. wrote the manuscript and discussed the final presentation with all of the authors.

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## Competing interests

The authors declare no competing interests.

**Supporting Information** Supporting figures and discussion contains the interlayer resistivity of 2D ReS<sub>2</sub> confirmed by c-AFM measurement, the enhancement of gate leakage current after the electrical stress, and the  $I_D$ - $V_D$  output characteristic and corresponding output transconductance curves as a function of  $V_{BG}$ , respectively. These materials further confirm the restricted channel migration and are available free of charge via the Internet at <http://pubs.acs.org>.

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