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## Switching Behavior and Comparison of Wide Bandgap Devices for Automotive Applications

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## **Keywords**

 $\ll$ Gallium Nitride (GaN) $\gg$ ,  $\ll$ Silicon Carbide (SiC) $\gg$ ,  $\ll$ Switching losses $\gg$ ,  $\ll$ Device characterisation $\gg$ ,  $\ll$ Automotive application $\gg$ .

#### **Abstract**

Wide Bandgap devices allow building more compact power converters. To study these new devices (SiC and GaN), static and dynamic tests are performed to models validating. A simulation for each target device is developed considering the main parasitic elements and the measurement instrument models. Thus, the switching losses are calculated and compared to experimental results. Since the whole system is validated, in order to compare the SiC and GaN devices for automotive applications, a DC-DC converter simulation is used for comparing each device under different operation points. Measurement results are presented to validate the simulation approach.

#### Introduction

The high power density capability of Wide Bandgap (WBG) power devices with the potentially fast switching and low losses make them suitable for automotive applications where performance and low weight are keys for the development of more compact power converters. To compare these devices, the static and dynamic characterization is performed for model validation. Afterwards, a simulation considering the same power and gate loop inductance is performed for each device, this allows us to evaluate the switching performance under equal conditions. A figure of merit (FOM) based on static resistance and switching losses is used as the main comparison element [1]. With the validated models, it is possible to develop a DC-DC converter simulation for each power device and comparing their performance for an automotive application at 200-400 V for different charge levels [2,3] [4–6]. The comparative analysis of the devices in a DC-DC operation is performed focusing on the switching FOM.

#### **Measurement Setup**

The characterization of WGB devices should be performed finely in order to develop reliable models in simulation. The transistor characteristics are measured with a Curve Tracer Keysight B1505A, Fig. 1. The output and capacitance characteristics are obtained as part of model validation. The test protocol should be performed carefully, given the unique properties of WGB devices. For instance, the drain

leakage current characteristics could modify the I-V response due to the current collapse associated with GaN components. Therefore, the output and capacitances characteristics tests are performed for two different samples, and without any previous leakage current measurements [7].

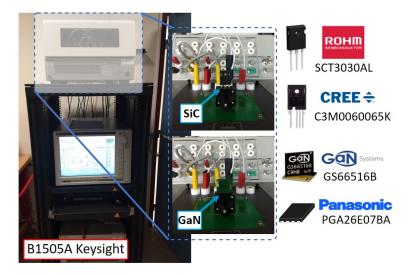


Fig. 1: Curve Tracer Keysight B1505A and the devices used in this work.

The switching behavior is analyzed by a Double Pulse Test (DPT) setup, as can be seen in Fig. 2. The devices chosen with nominal voltage of 600 V and 650 V are presented in Table I. An instrumented PCB is built for the GaN dynamic tests, given that the impact of parasitic elements is relevant for this technology. For the SiC components, an evaluation board from CREE is used. The waveforms of voltage, current and power switching losses are compared during a DPT for different operating points.

Table I: Selected power semiconductor devices with typical properties.

Component	Material	Type	V (V)	Inom (A)	$R_{DS(ON)}$ $(m\Omega)$	Driver	$R_{ON}(\Omega)$	$R_{OFF}(\Omega)$
		71	* nom ( * )	( )	RDS(ON) (Mass)		· · /	NOFF (SE)
GS66516T	GaN	eHEMT	650	60	25	Si8271 @ $-3/+6$	10	I
PGA26E07BA	GaN	GiT	600	31	56	1EDB7275F @0/3.4V	6	5
SCT3030AW7	SiC	MOSFET	650	70	30	Si8261 @ -3/+15	4	1
C3M0060065K	SiC	MOSFET	650	37	60	Si8261 @ -3/+15	4	1

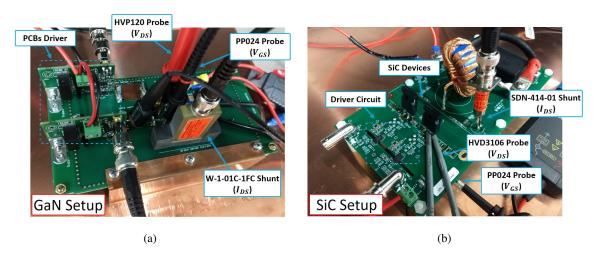


Fig. 2: (a) Instrumented PCB developed for switching characterization of GaN components. (b) Evaluation board KIT-CRD-3DD12P adapted for SiC components.

## Static and Capacitance Characterization for Model Validation

The output characteristics of the device need to be accurately measured. The linear mode for I-V graph is represented by the region where drain-source voltage is below the limit  $V_{gs} - V_{th}$ . This region is important for a good estimation of the ON-losses. If the drain-source voltage is above  $V_{gs} - V_{th}$ , the curve represents the saturation region, being important for a good estimation of the switching losses [8–11]. The capacitance characteristics define the energy amount involved in the device during a switching, being a fundamental element for the model validation.

In Fig. 3 and Fig. 4, a comparison between measurements, datasheet values and simulations can be seen. Some difference between experimental and simulation results are mostly related to a slight variation of the threshold voltage characteristic for each device. The Spice model from PGA26E07BA is adjusted in function of the experimental test through the changing of transconductance and threshold voltage.

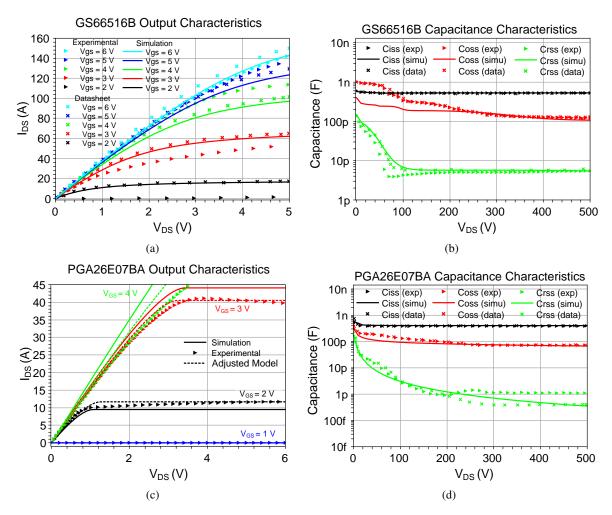


Fig. 3: GS66516B (GaN Systems): (a) output and (b) capacitance characteristics. PGA26E07BA (Panasonic): (c) output and (d) capacitance characteristics.

The comparison between experimental and simulation results presents a good correlation. The static and dynamic device characterization allows validating the SPICE models to use them in switching mode. Thus, considering some adjustments on threshold voltage, switching loss estimation can be performed by using the manufacturer available models.

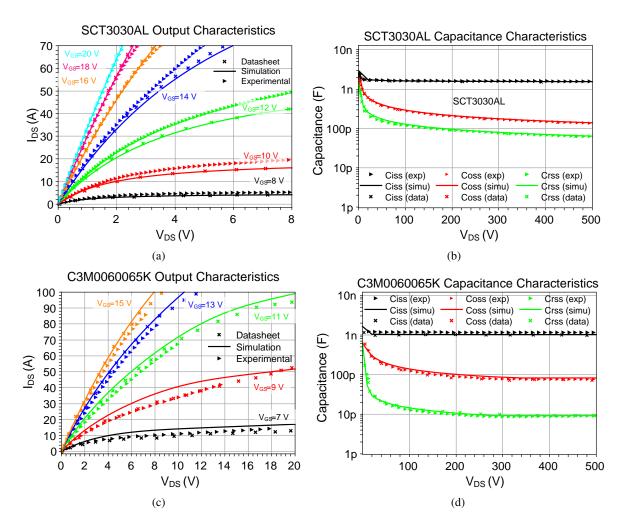


Fig. 4: SCT3030AL (Rohm Semiconductor): (a) output and (b) capacitance characteristics. C3M0060065K (CREE): (c) output and (d) capacitance characteristics.

## **Switching Characterization for Model Validation**

To validate the simulation models, a comparison of voltage and current waveforms is performed. In this study, two main elements are used to achieve a good correlation between simulation and experimental results: the effect of the gate inductance and power loop inductance. In Fig. 5, the result of gate and power loop inductance variation can be seen.

For the GaN simulation, the drain current slope is synchronized with the experimental test by means of the power loop inductance value. Afterwards, by considering the drain current peak reference, the gate inductance is adjusted. For the SiC simulation, the effect of power loop inductance variation on current slope is less pronounced, therefore the gate inductance is initially modified and then the power inductance is adjusted. The circuit test topology used for SiC and GaN validation follows the same concept (one-leg inverter), but the PCB used for SiC devices has not an optimized design since it comes with an evaluation test board. Hence, to perform the simulation comparison, the power and gate loop inductance are defined at same values.

To validate this methodology, the extraction of parasitic elements of the instrumented GaN PCB, Fig. 2(a), is performed. The software used is ANSYS Q3D Extractor. An Impedance Analyser is also used to measure the parasite inductance values. The comparison between simulation and experimental results can be seen in Fig. 6. The results found through the experimental test shows a good correlation with the inductance values extracted by Q3D.

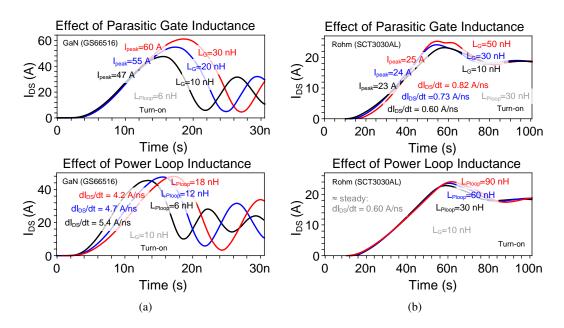


Fig. 5: (a) Effect of gate inductance and power loop inductance on drain current (GaN). (b) The same effect can be seen, but it is less pronounced for SiC devices.

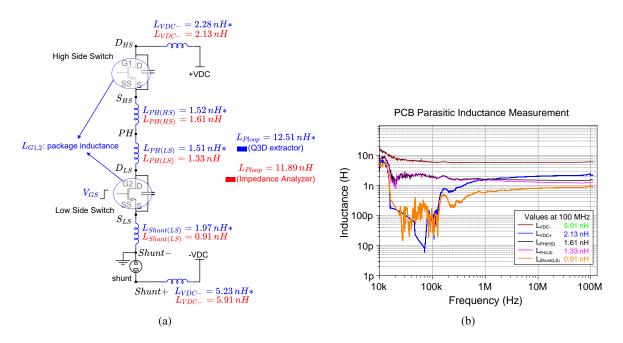


Fig. 6: (a) Parasitic inductance calculated extracted by ANSYS Q3D and measured values. (b) Parasitic inductance measurement obtained by an Impedance Analyser (E4990A).

The comparison between the performed simulations and the experimental data for switching of GaN and SiC device comparison can be seen in Fig. 7.

#### **Switching Losses**

The parasitic elements of the passive and active devices and geometry of the PCB layout determine the total power loop inductance on the circuit. In addition, it is important to highlight that there are parasitic effects which influence directly the oscillations detected during the switching time [2, 12]. The parasitic elements introduced by the test board and measurement instruments can overshadow the device behavior and lead to erroneous measurement results. The loss estimation is performed by using a simulation which

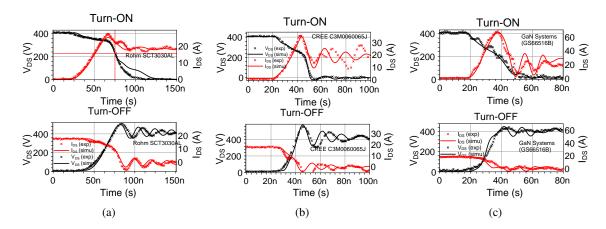


Fig. 7: Switching behaviour comparison for (a) SCT3030AL (Rohm), (b) C3M0060065K (CREE) and (c) GS66516B (GaN Systems).

takes into account the switch SPICE model, driver circuit, power and gate loop inductance ( $L_{Ploop}$ ,  $L_G$ ) and the electrical circuits of the measurement instruments (voltage probe and shunt). In this case, the total power loop inductance is estimated by the sum of the inductance values associated with the PCB tracks, switch package, and shunt. Furthermore, the speed at which the energy is transferred to a load is mostly determined by the equivalent series inductance (ESL) of a capacitor. This variable is also added to capacitor models. Mainly when it comes to high power or high frequency applications, these values can be very important and if not considered might lead to unexpected results.

The difference between each delay added by the shunt and voltage probes defines the variable delay compensation. The propagation speed of traveling waves through the transmission line is defined by a function of the cable inductance and capacitance, and can be deduced from the Telegrapher's equations. Where  $L_L$  and  $C_L$  represent the inductance and capacitance of the cable. With the propagation speed calculated and knowing the cable length l and its wavelength  $\lambda$ , the added delay due to the probe can be estimated by using (1).

$$u = \frac{1}{\sqrt{L_L C_L}}$$
 and  $\lambda = uT \Rightarrow \tau = l\sqrt{L_L C_L}$  (1)

Initially, by using Equation (1), the propagation time is calculated and applied in the Spice model of the measurement instrument. For the GaN evaluation board, the delay compensation is equal to 4.75 ns, due to the signal delay difference of the HVP120 voltage probe and W-1-01C-1FC shunt. For the SiC evaluation board this value is 8.9 ns, due to the HVD3106 voltage differential probe and SDN-414-01 shunt. This calculation is performed by subtracting the delay from voltage probe of the delay from shunt. In experimental results, by reading the values on the oscilloscope and performing a signal synchronization referenced to the gate source voltage, the delays are approximately equal to 4 ns and 9.4 ns for the GaN and SiC evaluation boards, respectively.

The Table II presents the switching loss values for the GaN device under different operation points, at 400 V the error between simulation and experimental data for total losses is about 16%. In Table III and Table IV the same results for the SiC devices. The maximal error at 400 V is about 8%, between simulation and experimental results. The column "Switch" represents the signal read directly at the device, and the column "Scope" the variable is read after the measurement instrument model. The difference error between SiC and GaN can be related to the GaN devices have more sensitivity to the delay compensation, because of their faster switching speed. Additionally, some high frequency disturbances not taken into account could generate more impact on GaN components.

Table II: Switching loss energy of GS66516. Parameters:  $L_{Ploop} = 19.5 \, nH$  and  $L_G = 47 \, nH$ .

Operation Points	Turn-ON (μJ)					
(V A)	Simulation		Experimental			
$(\mathbf{v} \mathbf{A})$	Switch	Scope	Delay Comp.	Scope		
100   4.3	9.4	14.4	10.1	15.2		
200   8.5	49.9	68.7	51.6	71.6		
300   12.6	128.2	160.2	136.5	171.8		
400   18 3	232.7	284.2	261.8	314 7		

Turn-OFF ( $\mu$ J)					
Simul	ation	Experimental			
Switch	Scope	Delay Comp.	Scope		
2.7	1.5	7.47	4.5		
6.2	3.2	13.3	9.5		
11.5	3.7	20.2	11.8		
16.5	5.2	36.8	19.9		

Table III: Switching loss energy of SCT3030AL. Parameters:  $L_{Ploop} = 58.5 \, nH$  and  $L_G = 30 \, nH$ .

Operation Points	Turn-ON (μJ)				
(V A)	Simulation		Experimental		
( <b>v</b>   A)	Switch	Scope	Delay Comp.	Scope	
100   3.6	8.9	12.9	11.7	16.2	
200   7.5	45.7	61.7	53.2	70.2	
300   12.8	131.8	172.1	141.7	181.8	
400   17.5	282.7	357.2	296.3	375.4	

Turn-OFF (μJ)					
Simul	ation	Experimental			
Switch	Scope	Delay Comp.	Scope		
2.9	1.1	2.6	1.2		
11.2	3.6	13.0	4.5		
40.4	16.8	42.3	19.8		
96.5	44.5	101.5	54.3		

Table IV: Switching loss energy of C3M0060065K. Parameters:  $L_{Ploop} = 58.5 \, nH$  and  $L_G = 30 \, nH$ .

Operation Points	Turn-ON (μJ)				
(V A)	Simulation		Experimental		
$(\mathbf{v} \mathbf{A})$	Switch	Scope	Delay Comp.	Scope	
100   3.6	2.8	7.5	4.2	10.6	
200   7.5	19.7	35.7	23.4	40.0	
300   12.8	44.2	85.8	62.2	98.3	
400   17.6	102.7	173.9	128.7	196.4	

Turn-OFF (μJ)					
Simul	ation	Experimental			
Switch	Scope	Delay Comp.	Scope		
1.6	0.3	1.4	0.5		
4.0	0.7	2.7	0.7		
15.7	2.6	9.3	1.0		
37.3	9.1	23.4	3.6		

## **Switching Characteristic Comparison**

The comparison between different power devices is commonly achieved by using different figures of merit. In automotive DC-DC applications, a high frequency performance is suitable, seen that the sizes of the passive components decrease proportionally. To compare the different switches in terms of switching losses, a simulation is performed by considering the same values for power loop inductance ( $L_{Ploop} = 6$  nH) and gate inductance ( $L_G = 10$  nH). This is possible due to the fact that each model was validated in static, dynamic and switching characterization by means of experimental tests.

Further comparability is reached by adding a conduction loss term namely switching FOM, thus the product between total switching energy and ON-resistance is plotted  $(E_{total} \cdot R_{DS(on)})$  [1]. The results for different currents are shown in Fig. 8. To study the thermal behavior aiming automotive applications, the switching losses and the mentioned FOM are also plotted at 150 °C, by using the ON-resistance in this temperature provided from datasheet. The Fig. 8(a) and Fig. 8(b) presents the turn-ON and turn-OFF energies, respectively.

As expected, the switching losses increase with higher current levels. The Fig. 8(c) shows lower total switching losses for the CREE device (C3M0060065K) at both temperatures analyzed. This is related to this device having a lower nominal current comparing to the other devices, thus a lower charge is required for the switching process. In Fig. 8(d), the effect of adding a conduction losses factor becomes evident the better performance for the GaN HEMT device (GS66516), at 25 °C. This is associated to the fact that the GaN having a lower ON-resistance and capacitances proportionally lower than SiC devices. However, due to the strong temperature dependency of the ON-resistance presented by the GaN HEMT, its switching FOM increase significantly at 125 °C.

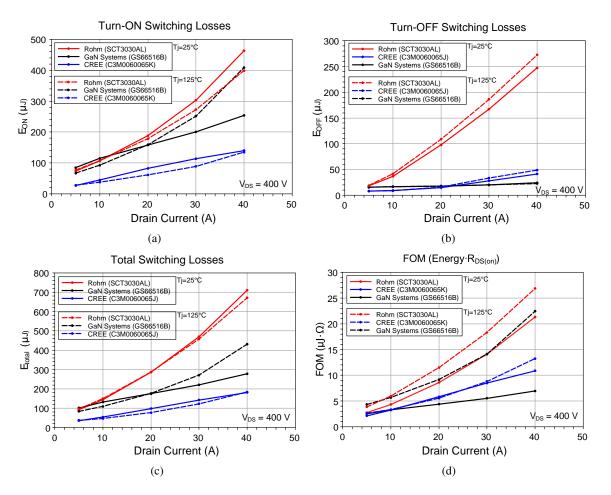


Fig. 8: (a) The turn-ON, (b) turn-OFF and (c) total switching losses. (d) Switching FOM (the lower the better) at different current levels. Simulation parameters: GaN Systems GS66516B -  $R_{ON},R_{OFF}$ : (10,1)  $\Omega$  and  $V_{GS}$ : (+6, -3) V; Rohm SCT3030AL -  $R_{ON},R_{OFF}$ : (0,0)  $\Omega$  and  $V_{GS}$ : (+18, -3) V; CREE C3M0060065K -  $R_{ON},R_{OFF}$ : (2.5,2.5)  $\Omega$  and  $V_{GS}$ : (+15, -4) V. These parameters are extracted from datasheets.

#### **Automotive Application**

The performance of power converters relies on the switching and conduction losses of power devices, given that lower power losses ensures maximum efficiency, high power density and downsizing the heat sink and cooling circuit [13]. Thus, the WBG devices are promising candidates for automotive applications. A typical DC-DC converter for an on-board charger can operate within a current range of 10-20 A, by considering a specification rated at 200-400 V for 3.6 kW. A boost converter simulation for each target device is performed under different frequencies and power levels. Thus, by considering the same conditions regarding to parasitic elements, the more adaptable device to an operating point can be named.

In Fig. 9 the synchronous boost converter is presented, as well as the current waveforms during transient period referenced to  $Q_{SW}$ . The turn-ON losses dominate the total losses because when the switch is turning-ON, the discharge current from the output capacitor ( $C_{dec}$ ) goes through the switches. Furthermore, the voltage fall time (turn-ON) of the switch is higher than its voltage rise time (turn-OFF) [14]. As seen in Fig. 9, during the turn-ON transient the main switch ( $Q_{SW}$ ) has higher losses than the complementary switch ( $Q_{sync}$ ). This is related to the turn-OFF moment of ( $Q_{sync}$ ). The initial value of ( $Q_{sync}$ ) is equal to the inductor current ( $Q_{sync}$ ), what decreases the channel losses. The reverse conduction also has a more resistive path, hence current peaks less accentuated are achieved.

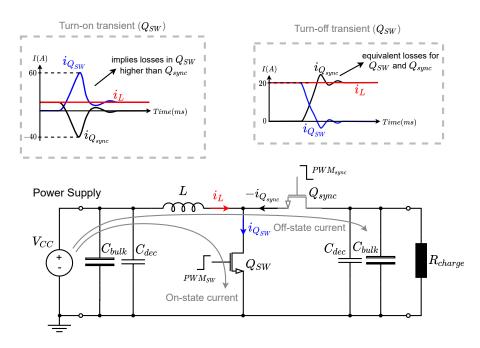


Fig. 9: Boost converter in switching transient.

The total losses are estimated by a SPICE simulation. In Fig. 10 the total power losses on switches can be seen. All simulations are performed at  $25\,^{\circ}C$  and  $125\,^{\circ}C$  as junction temperature. For an input power up to 3 kW the SiC CREE presents lower losses, due to its faster switching capability. As the power increases, the ON-resistance for SiC CREE starts to increase and becomes the more and more pertinent on total losses estimation, thus the GaN Systems device becomes the more efficient, given its inferior ON-resistance. Regarding the behavior at high temperature, all devices show higher switching losses. The GaN HEMT presents the difference more accentuated among devices, due to its strong temperature dependence, as previously discussed. Nevertheless, as shown in Fig. 10(b), for a nominal power rated at 3.6 kW, the GaN-based boost converter exhibits the lower total losses.

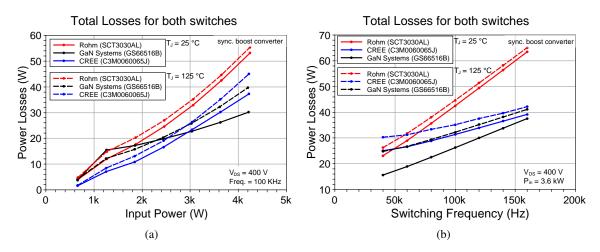


Fig. 10: (a) Total power losses for  $Q_{SW}$  and  $Q_{sync}$  versus (a) input power and (b) switching frequency.

#### **Conclusion**

The static and dynamic characterization is essential to ensure a good modeling for loss estimation. The parasitic elements extracted by numerical calculation was validated by measurement tests. A good correlation between simulation and experimental data was achieved for all power devices. The methodology

of turn-on current synchronization allows obtaining a maximum error of about 16% for GaN device and 8% for SiC devices. Regarding the switching figure of merit and our preliminary results, the comparison of switches shows that the GaN HEMT device exhibits better performance for the automotive application proposed.

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