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► **To cite this version:**

Etienne Sicard, Lionel Trojman. Introducing 5-nm FinFET technology in Microwind. 2021. hal-03254444

**HAL Id: hal-03254444**

**<https://hal.science/hal-03254444>**

Submitted on 8 Jun 2021

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# Introducing 5-nm FinFET technology in Microwind

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**Abstract:** This paper describes the implementation of a high performance FinFET-based 5-nm CMOS technology in Microwind. After a general presentation of the electronic market and the roadmap to 1-nm technology, design rules and basic metrics for the 5-nm node are presented. Concepts related to the design of FinFET and design for manufacturing are also described. The performances of a ring oscillator, basic cells and a 6-transistor RAM memory are also analyzed.

**Keywords:** FinFET, CMOS design, 5-nm, Ring oscillator, interconnects, SRAM, logic gates

## Introduction

Manufacturing smaller circuits begets the integration of more complex components to comply with a demand for an increased operating frequency and reduced power consumption. Continuous advances in process fabrication are enabling a vision of future nodes such as 5, 3.5, 2 and 1nm for the next decade [Anandtech 2019].

Through 8 application notes, we have tried to illustrate the increased performances of devices, specifically for the 14-nm and 7-nm nodes [Sicard 2017]. As two major silicon foundries, namely TSMC from Taiwan and Samsung from South-Korea have introduced 5-nm technologies in 2019, time has come to describe in more details the main characteristics of the 5-nm node, by exploiting available scientific literature and information released by semiconductor manufacturers.

Technology node	Year of introduction	Key Innovations	Application note
180nm	2000	Cu interconnect, MOS options, 6 metal layers	
130nm	2002	Low-k dielectric, 8 metal layers	
90nm	2003	SOI substrate	[Sicard2005]
65nm	2004	Strain silicon	[Sicard2006]
45nm	2008	2nd generation strain, 10 metal layers	[Sicard2008]
32nm	2010	High-K metal gate	[Sicard2010]
20nm	2013	Replacement metal gate, Double patterning, 12 metal layers	[Sicard2014]
14nm	2015	FinFET	[Sicard2017]
10nm	2017	FinFET, double patterning	[Sicard2017]
7nm	2019	FinFET, quadruple patterning	[Sicard2017]
5nm	2021	FinFET enhancement, EUV	This application note
3nm	2023	Ultimate FinFET, EUV	
2nm	2025	Multi Gate FET, buried supply	
1nm	2027	MGFET, n/p co-engineering	

Table 1: Most significant technology nodes over the past 20 years and prospective vision for 2023-2027

We take the opportunity of this publication to outline the electronic market growth, the motivation for 5-nm process. Then, we review the basic design rules, describe the transistor characteristics, and detail the implementation of basic cells such as the inverter, the ring oscillator, and the static memory. We conclude this document by discussing the switching performances of this node. We recall in table 1 the main innovations over the past recent years.

### Electronic Market growth

The growth of the overall electronic market over the last 40 years is illustrated in Figure 1. We note that electronic equipment for companies was the main driving force for electronic market growth up to 1995. From 2000, home computers, Internet-related devices and personal mobile phones took the lead. Although the economic recessions in 1990 and 1997 did not severely impact the electronic industry, the “telecom crash” in 2000 led to a historic decrease, with the market shrinking by nearly 12%.

While DVDs, flat screens, automobile equipment and 3G phones stimulated a market recovery in the 2002-2007 period, the “subprime” bank crash of 2008 again slowed down the electronics economy. In the 2010-2015 period, new markets related to modern society need such as renewable energy, 4-5G smartphones, Internet of Things (IoT) and high-resolution TV have led to sustainable growth. The latter was confirmed in 2019/2020 and likely explained by the ever-increased needs for electronic devices to maintain a relatively stable worldwide economy, spite of the sanitary crisis triggered by the covid pandemic. The pandemic has also changed consumer behaviors and boosted sales of personal computers, smartphones, entertainment devices starting mid-2020 and led to the global chip shortage in 2021, specifically in automotive and data center industry. Analysts say the global chip sales should reach 8 % in 2021 (nearly twice the estimated 4% growth in 2020).

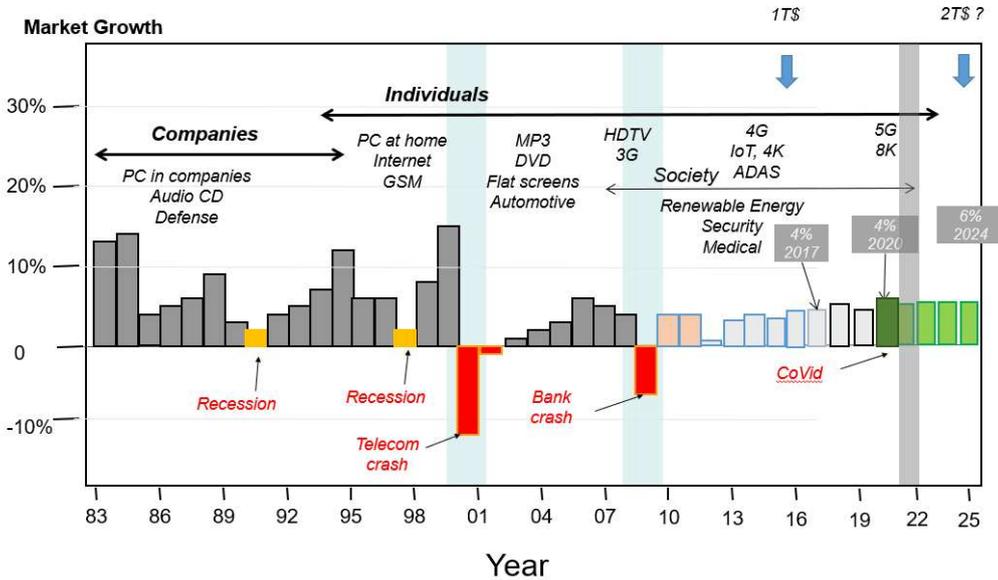


Figure 1: The Consumer electronics market growth over 40 years

### Motivation for 5-nm technology

The worldwide increase of disposable income along with the urban population demography, the expansion of the internet penetration and the availability of strong distribution network leading to accelerated digitalization of industry & services should result on a cumulated growth rate over the period 2020-2025 (CAGR) of about 16% for mobile communications, 15% for data centers, 12% for laptops, etc. (Fig. 2) according to a compilation of financial analysis such as Bloomberg, Mordor Intelligence & IDC.

Share of system sales  
2025 vs 2020

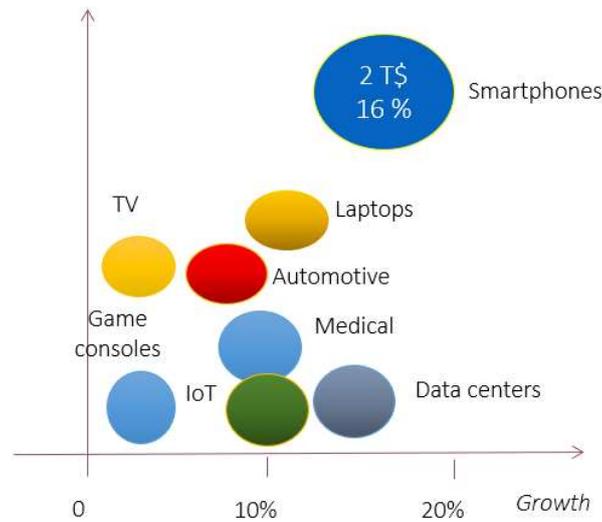


Figure 2: Expected cumulated growth 2025 vs 2020 (Adapted from Bloomberg, Mordor Intelligence, IDC)

Then, advanced technology nodes are expected to be in high demand for applications where speed and low power are critical, such as 5G mobile communications (smartphones), artificial intelligence, data centers & high-performance computing (HPC), secure & low-power networking, advanced systems for autonomous drive (ADAS) among others. A wide range of end-market applications is concerned, that span from cloud data centers to the harsh environment of the automotive market.

However, few semiconductor companies have claimed to operate the 5nm manufacturing process. In fact, only companies that produce very high volumes and require the highest operating efficiency can afford to pay the 100 M\$ design & fabrication costs. For instance, the first commercialized chip manufactured on a 5-nm process node is the Apple A14 processor [AnandTech 2020] for next generation smartphones, and Qualcomm's Snapdragon SD875 embedding a 5G baseband chip combined with an Adreno GPU (Graphic Process Unit), also for the smartphone market (Figure 3). In short, the need to switch as soon as possible to the 5nm is specific to the highly competitive smartphone segment.

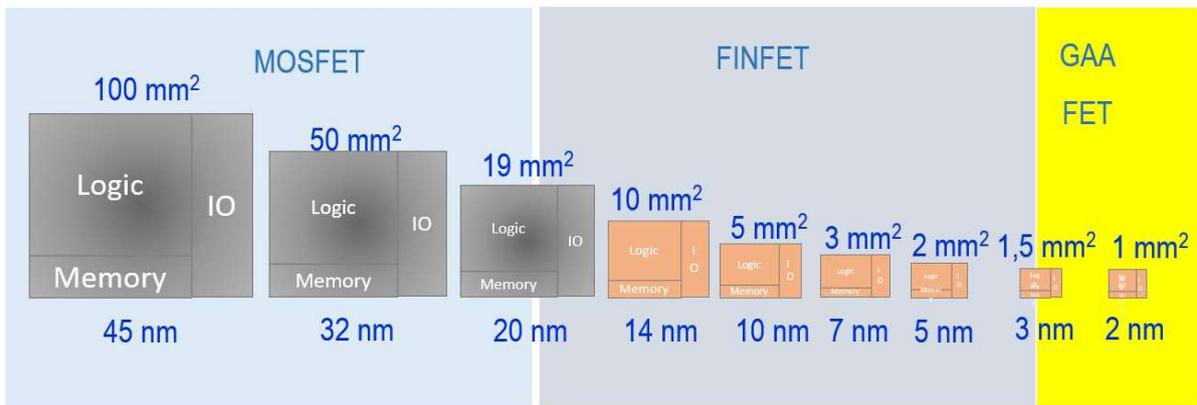


5-nm A14 by Apple (TSMC)



5-nm Snapdragon 875 by Qualcomm™

Figure 3: products fabricated in 5-nm technology by TSMC foundry and design by fabless companies as Qualcomm and Apple.



Adapted from Mistry, K. (2017). 10 nm technology leadership, Technology and Manufacturing Day, Intel. 2017.

Figure 4: Scale down benefits in terms of silicon integration, and associated FET technology.

The 5-nm process is largely design-rule compatible with previous 7-nm one [Sicard 2017], which should save time and limit the cost of redesign. At the time of the writing of this note, only Samsung and TSMC were offering 5-nm (N5) foundry services. One of the key arguments for scaling down the lithography is the ability to implement the same processor within a smaller silicon area, as shown in Figure 4. The 5-nm process enables more than 150 million transistors per millimeter square. A 10-billion devices such as 5G processor Kirin 990 from HiSilicon/Huawei would fit in an 8 x 8 mm<sup>2</sup> Silicon area.

A second argument is that the 5-nm technology node extends by 20-30 % the power saving and not the least the speed by 10-15% compared to 7-nm process (N7). Indeed, if we consider a basic cell such as a logic inverter with typical loading condition (3 similar gates with proper average distance), a 5-nm inverter would have around 1.5 ps average delay for each stage (Figure 5).

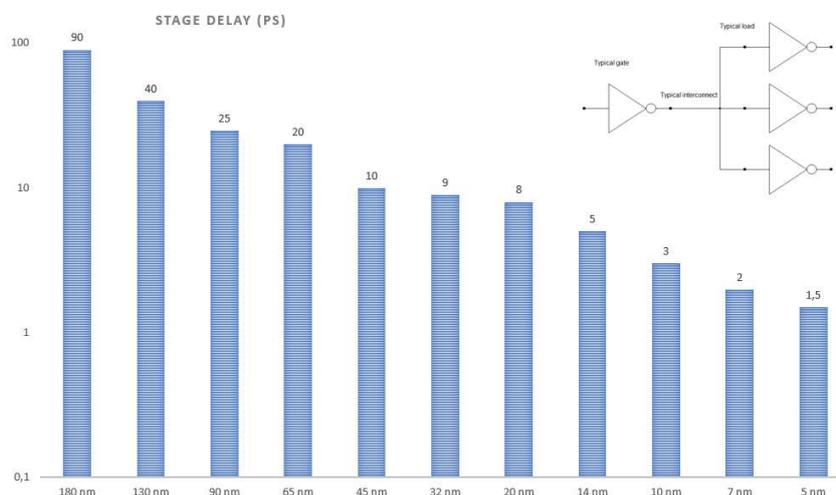


Figure 5: Average switching delay per gate for technologies ranging from 0.18 μm down to 5 nm

## FinFET

FinFETs have started to replace MOSFET starting 20-nm generation (Figure 6). Intel's 22-nm process was the first technology to use FinFETs, soon followed by TSMC and Samsung with their 14-nm process. The ability to scale FinFETs has enabled significant gains in switching performances down to 3-nm. Various boosters have been introduced in the FEOL device: SiGe channel strain, high-k metal gate, low-resistivity contacts (USJ, Silicide) Silicon-on-insulator wafer (SOI) [Sharan 2019], etc. to meet the ever-increasing performance targets.

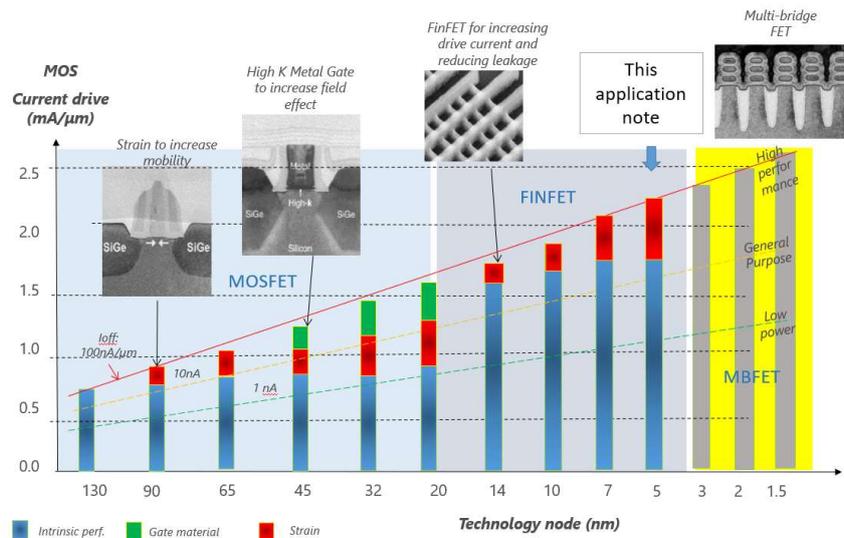


Figure 6: The 5-nm process is still FinFET, with several device enhancements as compared to 7-nm technology.

### Roadmap to 1nm

In the applications notes related to 14-nm [Sicard 2017a] and 7-nm technology [Sicard 2017b], we paid a lot of attention to Intel, TSMC, Samsung, GlobalFoundries and UMC process characteristics based on the available scientific publications. Intel’s 7nm process, initially scheduled for 2017, was shifted to mid-2021, with a production ramp-up late 2021 with the 12th CPU generation Alder Lake GPU. The Intel’s 5nm process appears in the 10-years roadmap “In Moore we trust” (Figure 7) reported by [Anandtech 2019], but 2023 seems very optimistic considering the extended lifetime of Intel’s 14nm and 10nm nodes. On the other hand, the Intel company is not directly involved in the smartphone segment and keeps highly competitive in its key application segment focused on computer microprocessor.



Figure 7: “In Moore we trust” by Intel™ cited by [Anandtech 2019]

It should be noted that process improvements within the same node (N5, N5P for Samsung) usually deliver additional performance in terms of operating frequency, power savings and density. Looking at Intel’s roadmap, successive iterations of process nodes (Like 7, 7+, 7++) conduct to an overlapping with the next process node for possible backporting of the newer process into the oldest ones. This can be understood as a strategy to smoothen the economic transition and sustain the financing of the next generation technological node.

### Fabrication & Costs

As detailed in [Wikichip 5nm], around 80 lithography masks are required to process a 5-nm chip, which is a bit less than for previous 7-nm node. The introduction of EUV (DUV) has decreased the number of masks but has increased the fabrication costs. As suggested in the previous paragraph the lithography is an economical limitation for the company leading to adopt different strategy for the CMOS scaling (smoother transition). Development & qualification costs of libraries, Intellectual Properties (IP) have gradually increased, to attain around 110 Million \$ for the 5-nm node (Fig. 8). The 5-nm process development cost is estimated between 2 and 3 Billion \$ while the fab itself costs nearly \$10 billion, which explains why only 2 companies, namely Samsung & TSMC (and potentially a 3<sup>rd</sup> company Intel in 2023) were able to bear such incredible costs.

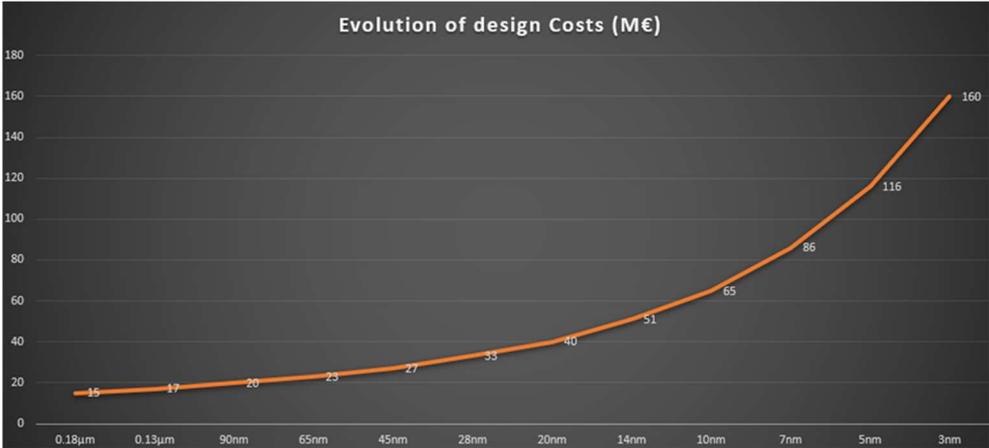


Figure 8: rising design, test & fabrication cost of integrated circuits with nano-scale technologies

### Gate-All-Around FET

While 5nm & 3nm nodes should be using exclusively FinFET’s [Wikichip 5nm], as far as TSMC & Samsung are concerned, we should enter a transition period from FinFETs to new device architectures, such as the ‘Gate-All-Around’ FET (GAAFET) [Das 2020]. The GAAFET has been presented as “Nano-ribbon” by Intel (Figure 9), as reported by [AnandTech 2019], or Multi-Bridge-Channel MOSFET (MBCFET) by Samsung [Bae 2018], with significant gains in terms of electrostatic efficiency.

However, TSMC has announced that its 3nm process technology would remain with FinFETs, as sufficient progresses have been made on devices to allow performances which are comparable to next generation devices. It is not a surprise that process engineers, who are quite conservative, are trying to extend the use of the FinFET as long as possible, to pay back the considerable costs of R&D and manufacturing process.

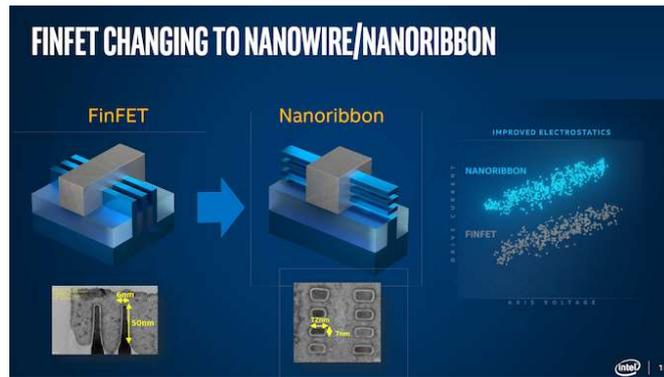


Figure 9: Intel's vision of the shift from FinFET to Nanoribbon/GAAFet [Anandtech2019]

## Basic design rules

We justify here the choice we made to tune the MOS device and interconnect generator of Microwind to the most realistic design rules. We detail important metrics such as the metal pitch & gate pitch.

### The value of $\lambda$

We fix  $\lambda$  to 4.0 nm, just the same as for 7-nm technology [Sicard 2017]. In other words, we do not comply any more with the simple rule which stated that “ $\lambda$  is (approx.) half of the technology”, which was applied without any exception in previous application notes. The main reason is that nano-scale patterning has become so difficult that technology engineers can no longer afford to scale down dimensions as was done in the past.

Then, the next question may rise: is the so-called 5-nm process a physical scaling or is an improvement/optimization of the 10nm/7nm technology node process? Descriptions of the 5-nm technology such as proposed in [Wikipedia 5nm] have put in parallel existing rules from Samsung & TSMC and the International Roadmap for Devices & Systems (IRDS), 2017 edition. In table 2 the available 5-nm processes do not even match the ground rules for logic device technologies published by IRDS for 7-nm process. Unlike TSMC's 5-nanometer node, Samsung 5-Nanometer Low-Power Early (5LPE) seems to be only a “quarter node” successor to the 7-nanometer process, with limited gains in terms of density, mostly by the reduction of the logic cell height (see section below) and not by the decrease of  $\lambda$ .

### ^ 5 nm process nodes

	Samsung <sup>[21]</sup>	TSMC <sup>[22]</sup>	Intel	IRDS roadmap 2017 <sup>[23]</sup>	
Process name (nm)	5LPE	N5	P1278 <sup>[24]</sup>	7	5
Transistor density (MTr/mm <sup>2</sup> )	127	173 <sup>[25]</sup>		?	?
SRAM bit-cell size ( $\mu\text{m}^2$ )	0.026	0.017–0.019		0.027 <sup>[26]</sup>	0.020 <sup>[26]</sup>
Transistor gate pitch (nm)	57	48		48	42
Interconnect pitch (nm)	36	28 <sup>[27]</sup>		28	24
Risk production year	2018 <sup>[14]</sup>	2019 <sup>[15]</sup>		2019	2021

Table 2: Key dimensions of Samsung's 5LPE & TSMC's N5 processes compared to 5-nm node forecast of ITRS in 2017 according to [Wikipedia 5nm]

## Metal pitch

Published values for metal pitch in 5-nm node range between 24 and 36 nm. To be compatible with older processes, we keep metal1 & metal2 width to  $4\lambda$  and spacing to  $4\lambda$ , to achieve a metal pitch (MP) of 32 nm, which is close to Samsung's 36 nm and TSMC's 28 nm interconnect pitch (Table 3). Smaller MP values such as 24 nm [Lee 2016] correspond to  $3\lambda$  width &  $3\lambda$  spacing. Therefore, for the sake of compatibility with previous nano-scale nodes, the minimum metal1 width r501 remains at  $3\lambda$  and metal1 spacing r502 too. However, a Samsung/TSMC-compatible design style should be based on  $4\lambda$  width,  $4\lambda$  spacing. Figure 10 compares the design of lower metal lines with  $8\lambda$  metal pitch (upper design, close to TSMC & Samsung) and  $6\lambda$  (lower design). These values are the same for metal1 & metal2.

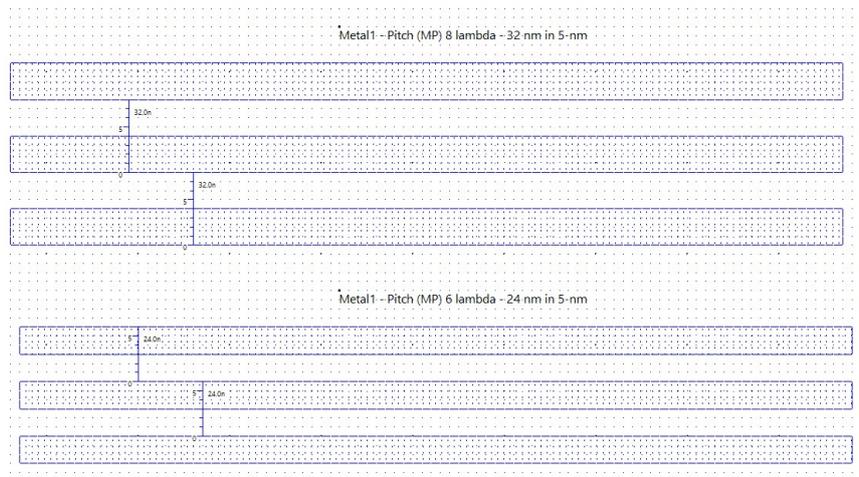


Figure 10: Illustration of metal width, spacing & pitch for two variants: minimum pitch 24 nm & regular pitch 32nm used for automatic routing (5nm\metal pitch.MSK)

Design parameter	Unit	Code	Name in rule file	Value in 5-nm process	Bloc level
Lambda	nm	$\lambda$	lambda	4.0	
M1 Pitch	nm	MP	R501+R502	24	Cell
M2 Pitch	nm		R701+R702	24	Cell
M3 Pitch	nm		R901+R902	40	Bloc
M4 Pitch	nm		Rb01+Rb02	40	Bloc
M5 Pitch	nm		Rd01+Rd02	64	Macro-bloc
M6 Pitch	nm		Rf01+Rf02	64	Macro-bloc
M7 Pitch	nm		Rh01+Rh02	160	Power grid Supply, embedded C, L
M8 Pitch	nm		Rj01+Rj02	320	Power grid Supply, embedded C, L
Rule file				Cmos5nm.rul	

Table 3: metal pitch parameters of the 5nm process implemented in Microwind

Metal pitch information concerning upper metal layers may be found in [Prasad 2019]. It can be seen that the metal 3..4 pitch is increased to  $10\lambda$  (40 nm), metal 5..6 pitch to  $16\lambda$  (64 nm), while the two last layers are dedicated to very thick & large supply grid with low resistivity to enable an efficient chip supply.

## Supply Voltage

We summarize in figure 11 around 30 years of technological advances with details about the internal core supply and the external I/O supply. The nominal I/O supply has been reduced gradually from 5.0V down to 1.0V while the internal core supply VDD has been further reduced from 3.3V down to 0.65 V, with prospective 0.6V supply for 2nm node (figure 11). Considering a voltage noise margin of 10% VDD, we may consider that the largest acceptable noise within signals and supply interconnects should be less than 65 mV in 5-nm technology.

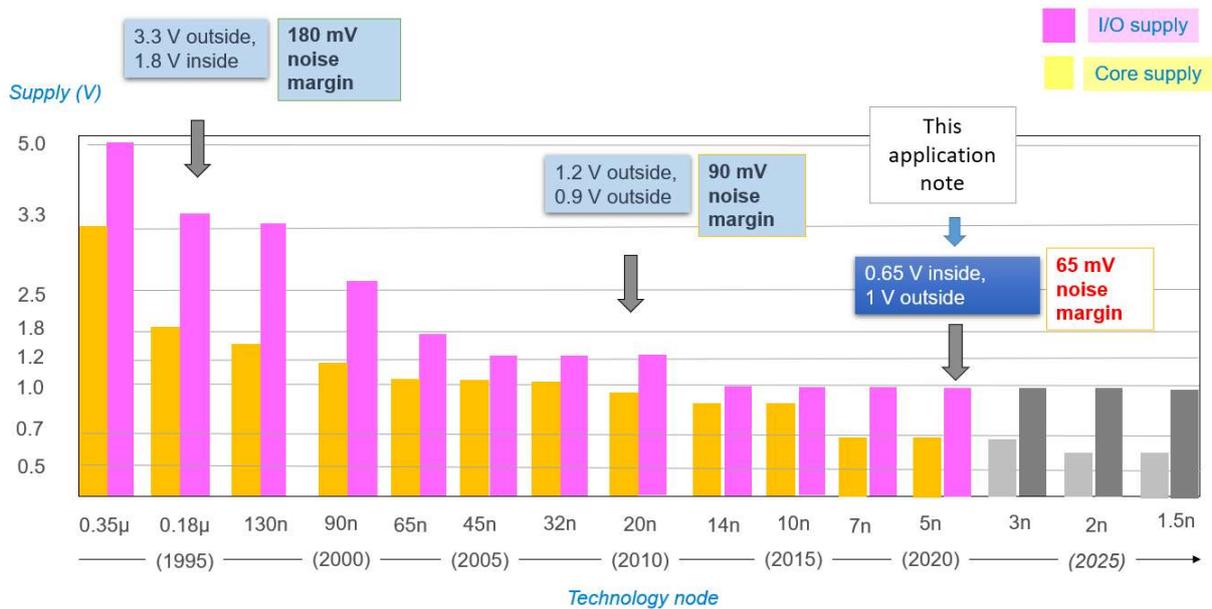


Figure 11 : Illustration of the supply voltage reduction with feature size reduction over 30 years of technology progresses

## Reduced number of masks

The 5-nm node is the first technology to make extensive use of extreme ultraviolet lithography (EUV). With a wavelength around 13.5 nm, EUV light can produce extremely fine patterns on silicon. Instead of the self-aligned quadruple patterning [Sicard 2017], extreme ultraviolet lithography (EUVL) lowers the number of masks & process steps (Figure 12), as announced in [Yeap 2019]. One Extreme UltraViolet (EUV) mask can replace up to 5 immersion masks, with better patterning yield & shorter fabrication time.

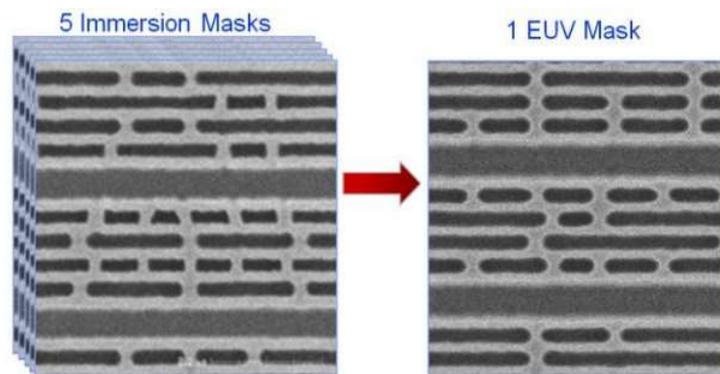


Figure 12 : One Extreme UltraViolet (EUV) may replace 5 immersion masks, with better patterning yield & shorter fabrication time [Yeap 2019]

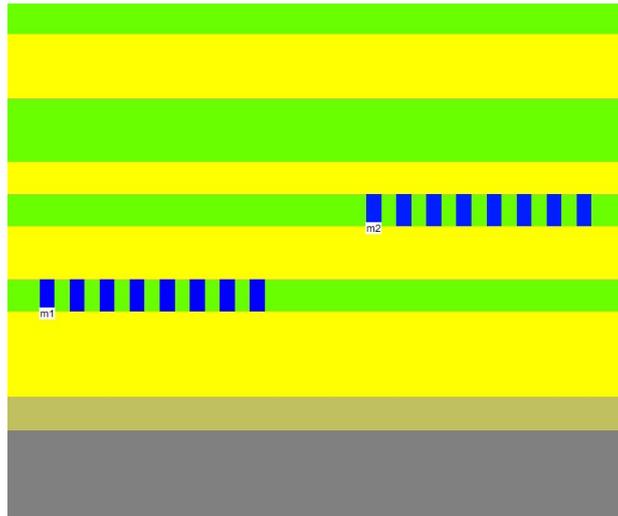


Figure 13: Cross-section of a metal bus in metal 1 (left) and metal 2 (right) with a 32-nm lower metal pitch

For upper metal layers used for interconnecting blocs and cores, the metal pitch is nearly the same for M1, M2 & M3, and rises 50% for M4 & M5, and 50% more for upper metal layers M6 & M7 [Lee 2016]. Figure 13 shows the cross-section of a metal bus in metal 1 (left) and metal 2 (right) with a 32-nm pitch.

### Gate pitch & length

For the past decades, CMOS scaling has enabled about 50% area gain per generation. In other words, a 10nm design was implemented with a silicon area nearly half of a 14 nm design, same for 7nm vs. 10nm, etc. The nano-scale patterning complexity has slowed down the scaling of the metal pitch, as discussed in the previous paragraphs, not to mention the so-called “contacted gate pitch”, which is the minimum separation between 2 active gates (Fig. 14). The overall area gain is evaluated by less than 30 % between 7 and 5 nm (against the 50 % expected). This gain could even decrease at 25% from 5 to 3 nm and be as low as 10 % from 3 to 2 nm [Mocuta 2018]. The area gain is no more obtained by aggressive scale down of elementary features like fin, gate & metal tracks, but by smaller cell area obtained by design optimization, as will be presented in the following chapters.

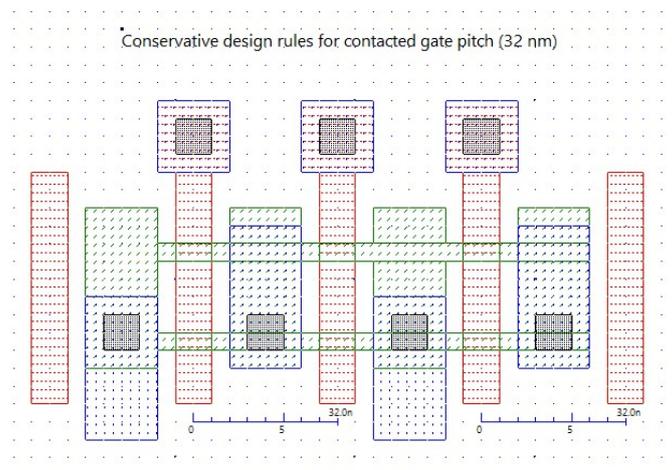


Figure 14: Illustration of the Contacted Gate Pitch CGP (contacted gate pitch.MSK)

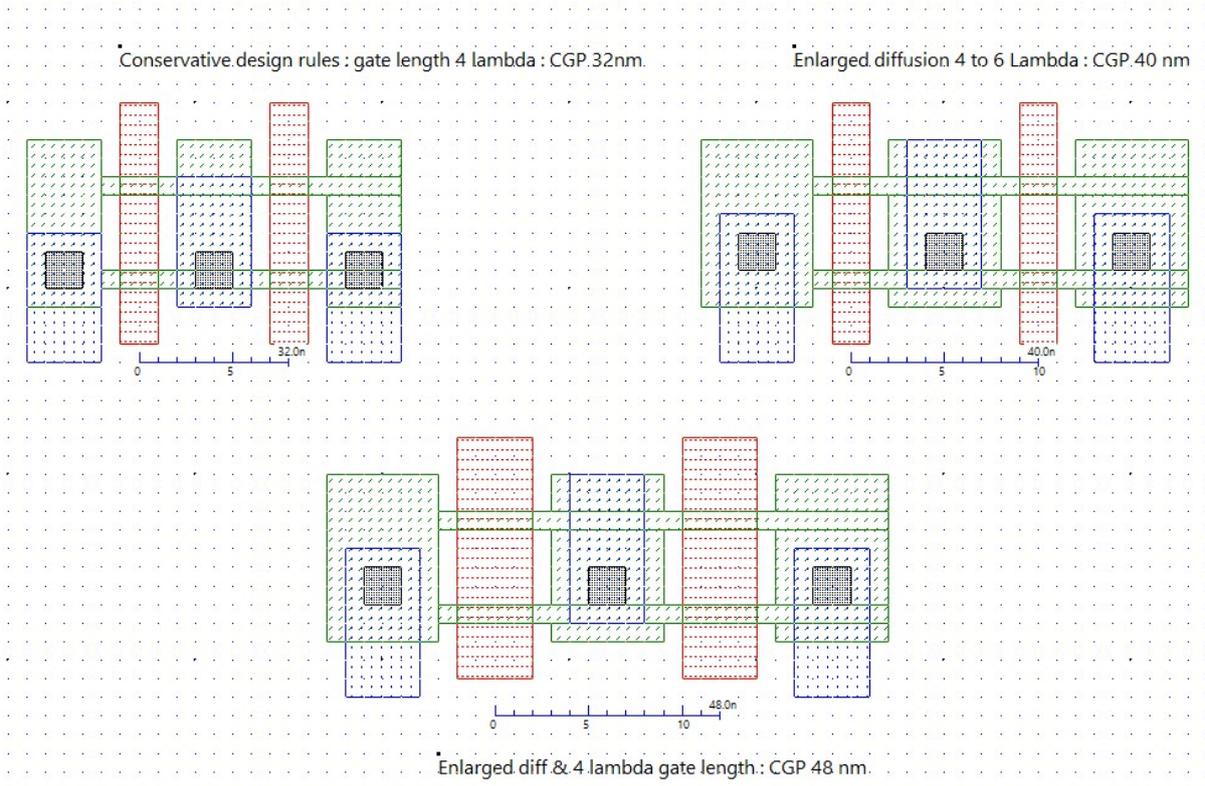


Figure 15: The Contacted Gate Pitch is extended to 48-nm using enlarged diffusion and larger distance between diffusion and gate (contacted gate pitches.MSK)

Using conservative design rules would lead to a 32 nm Contacted Gate Pitch (CGP), close to the assumptions of [Huynh-Bao 2017][Das 2020] as shown in Figure 15, significantly more aggressive than the 48..57-nm pitch announced by Samsung & TSMC [Wikipedia 5nm]. To be consistent with a larger CGP, the diffusion area needs to be extended from 4 to 6  $\lambda$ , which gives a 40-nm CGP. If the gate length is enlarged from 2 to 4  $\lambda$  (8 to 16 nm), we get 48 nm, close to the CGP values used by TSMC & Samsung which is not what we could expect if we use a traditional scaling process (conservative design rule, Fig. 14) and illustrates the difficulties to scale down for these companies.

In Microwind, we increase the diffusion width (r201) from 4  $\lambda$  (conservative rules) to 6  $\lambda$  (enlarged rules), and the distance contact/gate from 2  $\lambda$  to 3  $\lambda$  (r406), in order to achieve a FinFET layout tuned to 40-nm CGP (Fig. 14, upper right). The resulting FinFET design is significantly larger than the FinFET drawing with linear scale down & conservative design rules (Figure 14, upper left). The gate length  $L_g$  is controlled by rule r302. The conservative design rule is 2  $\lambda$  (8 nm). It should be noticed that the fin is in reality 4  $\lambda$  long (16 nm) due to a little space (1  $\lambda$ ) required between the gate and drain/source areas (Figure 14, bottom and Fig. 15).

## Transistor characteristics

### Fin pitch & width

Different values are considered for the fin pitch. Table 4 gives some numbers comparing 10-nm, 7-nm and 5-nm nodes [Yoon 2019] [Wu 2020]. Looking for example at [Yoon 2019], we see that the fin pitch (FP) has only been reduced 25 % from 10-nm to 5-nm, and not 50% according to general scaling rules, as mentioned earlier for gate pitch.

Geometrical Parameters		Values (nm)		
		10-nm	7-nm	5-nm
<i>CPP</i>	Contacted poly-gate pitch	54	44	36
<i>FP</i>	Fin pitch	34	30	26
<i>SP</i>	P/N-type separation length	68	60	58
$L_g$	Gate length	18	16	14
$L_{sp}$	Spacer length	7	6	5
$L_{sd}$	S/D length	22	16	12
$W_{fin}$	Fin width	7	6	5
$H_{fin}$	Fin height	46	46	46

[Yoon 2019]

Technology Node	10 nm	7 nm	5 nm
Fin Pitch (nm)	33~42	27~30	22.5~25
Contact to Poly Pitch (nm)	66~68	54~56	44~50
Metal Pitch (nm)	44~48	36~40	30~32

[Wu2020]

Table 4: Geometrical parameters of the FinFETs in 10, 7 and 5nm proposed in [Yoon 2019] & [Wu2020]

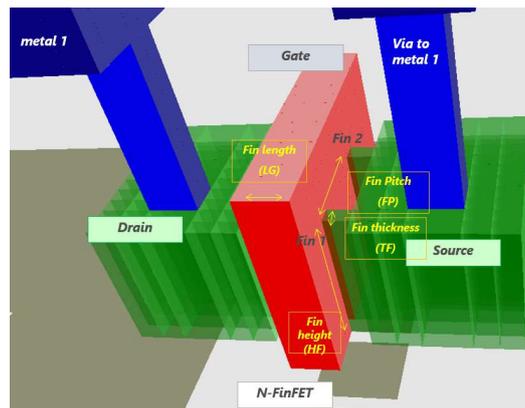


Figure 16: Illustration of Fin thickness, length & pitch

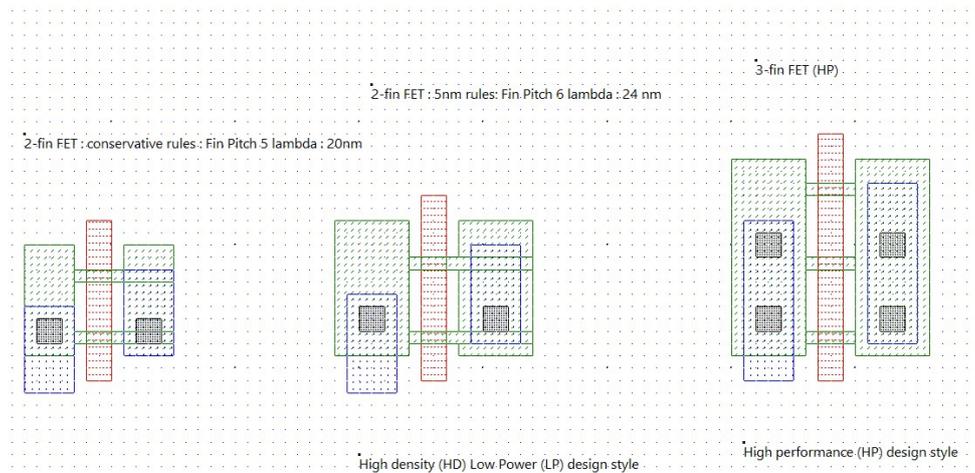


Figure 17: The fin pitch is set to 24 nm in the 5-nm process (Fin pitch.MSK)

The fin pitch (FP) ranges from 22 to 26 nm according to publications. Consequently, the FP rule r308 in Microwind is fixed to  $6\lambda$ , that is 24 nm. The fin width is  $1\lambda$ , that is 4 nm, close to 5 nm proposed by [Yoon 2019]. It is worth noting that the height fin is assumed to not affect the Si area occupation and should not affect physically  $\lambda$ .

Two examples of FinFET designs with 24-nm fin pitch (vertical distance between 2 fins) are reported in Figure 17 : 2 fins for “high density” (HD) or “Low Power” (LP) (center) and 3 fins for “high performance” (right). In 5-nm technology, FinFET devices are mostly proposed with 2 or 3 fins. The 2-fin device is more compact, the corresponding cell library is usually called “High density” (HD). The 3-fin device features a 10% boost in current drive [Yeap 2019], but requires a larger cell, and belongs to the “High performance” (HP) library. In 7-nm, we used to have 4 fins for HP and 2 fins for HD. The RUL file enables to change the number of fins through parameters  $b4Hpfin$  (HP) and  $b4lpfin$  (LP).

The fin height ranges between 40 and 50 nm [Yoon 2019] [Feng 2017][Shang 2020]. We choose 45 nm in Microwind, by setting parameter  $b4hfin$  to “45e-9”.

### About $I_{on}$ , $I_{off}$ and $I_{eff}$

It is a bit difficult to tune I/V characteristics of FinFET devices based on scientific publications from 5-nm process providers, as  $I_{on}$  &  $I_{off}$  are often presented (Fig. 18) using the fatal “a.u.” which stands for “Arbitrary Unit”, probably due to confidentiality issues, sometimes to hide poor performances compared to competitors or significant mismatch as compared to roadmaps. In other words, we do not know the exact numbers. Only the Drain-Induced Barrier Lowering (DIBL) and swing are detailed for TSMC 5-nm technology [Yeap 2019].

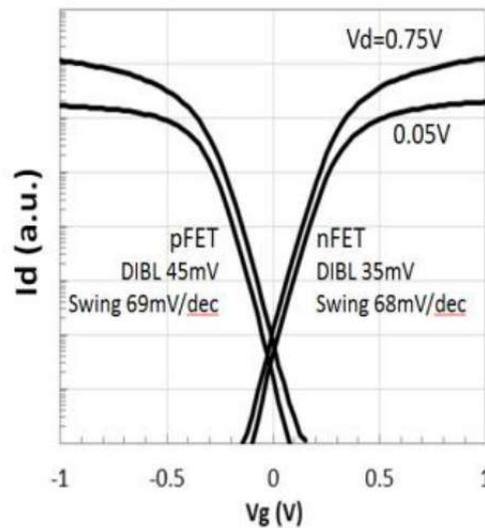


Figure 18: 5-nm  $I_d/V_g$  characteristics presented in arbitrary units [Yeap 2019]

Device	$I_{on}$	$I_{off}$	Reference	Supply voltage
<i>n</i> -FinFET	1.5 mA/ $\mu$ m	1 nA/ $\mu$ m	[Lee 2016]	0.6
<i>n</i> -FinFET	2.1 mA/ $\mu$ m	10 nA/ $\mu$ m	[Pal 2019]	0.7
<i>p</i> -FinFET	1.9 mA/ $\mu$ m	10 nA/ $\mu$ m	[Pal 2019]	0.7
<i>n</i> -FinFET	75 $\mu$ A/fin	na	[Shang 2019]	
<i>n</i> -FinFET	1.5 mA/ $\mu$ m	100 nA/ $\mu$ m	[Agarwal 2018]	0.65
<i>n</i> -FinFET	1.8 mA/ $\mu$ m		[Kurniawan 2018]	0.5
<i>p</i> -FinFET	1.5 mA/ $\mu$ m		[Kurniawan 2018]	0.5
<i>n</i> -FinFET	42 $\mu$ A/fin	10 nA/fin	[Huang 2017]	0.6
<i>n</i> -FinFET	12 $\mu$ A ( $I_{eff}$ )	10 pA (LP)	[Yoon 2019]	0.7

<i>p-FinFET</i>	25 $\mu\text{A}$ ( <i>I<sub>eff</sub></i> )	0.1 nA (MP)	[Yoon 2019]	0.7
	50 $\mu\text{A}$ ( <i>I<sub>eff</sub></i> )	1 nA (HP)		
	8 $\mu\text{A}$ ( <i>I<sub>eff</sub></i> )	10 pA (LP)		
	18 $\mu\text{A}$ ( <i>I<sub>eff</sub></i> )	0.1 nA (MP)		
	38 $\mu\text{A}$ ( <i>I<sub>eff</sub></i> )	1 nA (HP)		

Table 5: published *I<sub>on</sub>/I<sub>off</sub>* values for the 5-nm node

Luckily, some publications give explicit numbers for *I<sub>on</sub>* and *I<sub>off</sub>* currents (Table 5). However, the metrics are not always the same, or do not correspond to the same *I<sub>off</sub>* target nor the same supply voltage, but we may try to link this numbers for comparison purpose. If we know the fin height (FH, in nm) and fin width (FW, in nm) and assume that the current is dominated by the top and the fin sides, we can extract the fin perimeter which is FH+FW+FH, which is the equivalent channel width for 1 fin.

$$I_{on_{mA/\mu m}} = \frac{I_{on_{\mu A/fin}}}{(2 \times FH + FW)_{nm}} \quad \text{eq. 1}$$

For example, in [Shang 2019], *FH* (nm) = 50, *FW*=5, *I<sub>on</sub>*( $\mu\text{A}/\text{fin}$ ) = 75, so *I<sub>on</sub>*(mA/ $\mu\text{m}$ ) = 0.71 mA/ $\mu\text{m}$ . In table 5, we do not only see *I<sub>on</sub>*, but also *I<sub>eff</sub>*. In figure 19, n-FinFET and p-FinFET with equivalent width of 1.0  $\mu\text{m}$  are shown. To achieve this result, 11 fins have been used. Although not used for cell design, this device is convenient to extract directly *I<sub>d</sub>/V<sub>d</sub>* and *I<sub>d</sub>/V<sub>g</sub>* curves in mA/ $\mu\text{m}$ .

As described in [Sicard 2017], *I<sub>eff</sub>* corresponds to the average current during switching operation and may be approximated to half of *I<sub>on</sub>*. In other words, *I<sub>eff</sub>*=50  $\mu\text{A}$  would correspond to *I<sub>on</sub>*=100  $\mu\text{A}$  for an equivalent width (*FW*+2*FH*) estimated around 50 nm, that would lead to 2.0 mA/ $\mu\text{m}$  (Fig. 20). The cross-section of this device is reported in Fig. 20.

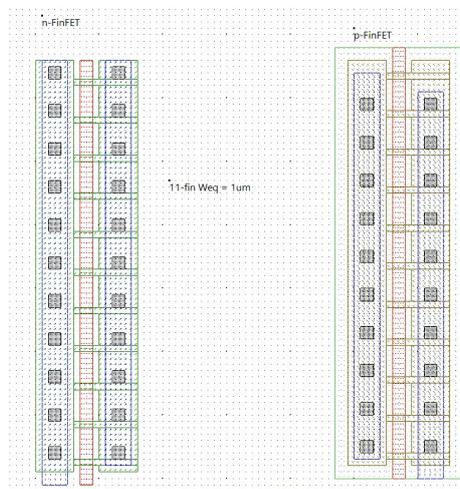


Figure 19: designing a FinFET with 1 $\mu\text{m}$ -eq. width would require 11 fins (*finFET-5nm-Weq1um.MSK*)

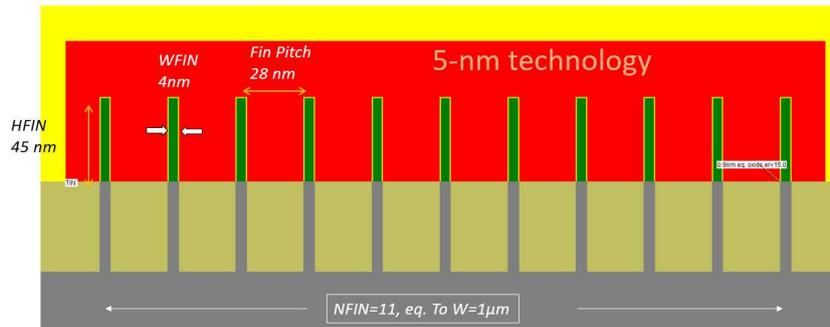


Figure 20: Cross-section of the FinFET with  $1\mu\text{m}$ -eq. width with 11 fins (finFET-5nm-Weq1um.MSK)

### Transistor capacitances

An important parameter which impacts the FinFET switching performances is the capacitance of the gate stack which is in the range  $0.25..1.0 \text{ fF}/\mu\text{m}$  [Agarwal 2018][Kao 2020][Yoon 2019]. We have seen previously that  $W_{eq}=1\mu\text{m}$  corresponds to 11 fins. Considering a 2-fin device, we may consider a global gate capacitance within the range 50-200 aF. In our implementation of the 5-nm process in Microwind, the global gate capacitance of an inverter, which includes mainly the n-FinFET and p-FinFET gate capacitance, is around 135 aF (Fig. 21).

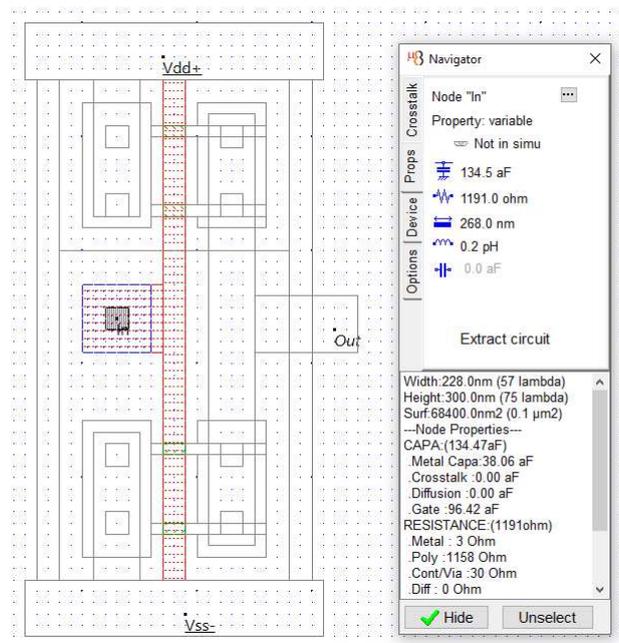


Figure 21: extracting the input capacitance of an inverter (inv.MSK)

### Transistor Options

It is worth noting the huge difference between  $I_{on}$  values for low-power (LP), medium-power (MP) and high-performance (HP) devices [Yoon 2019] with variations close to a factor 4 between LP and HP. Similarly, Samsung's 5-nm technology [Yeap 2019] proposes up to 7 variants of the FinFET devices: Standard-VT Low Voltage (SVT-LL), Standard VT (SVT), Low VT, Low leakage (LVT-LL), Low Threshold Voltage (LVT), ultra-low Vt Low leakage (uLVT-LL), Ultra-Low VT (uLVT) & extremely low Vt (eLVT). The  $I_{on}$  difference between extreme situations is nearly 100 %. One way to achieve variable threshold voltage  $V_t$  is to modify the work function (WF) by means of the proportion of metal layers used to build

the gate stack [Yoshida 2017]. Another way is to use a Germanium-based channel to provide a high-mobility channel (HMC) [Sharan 2019].

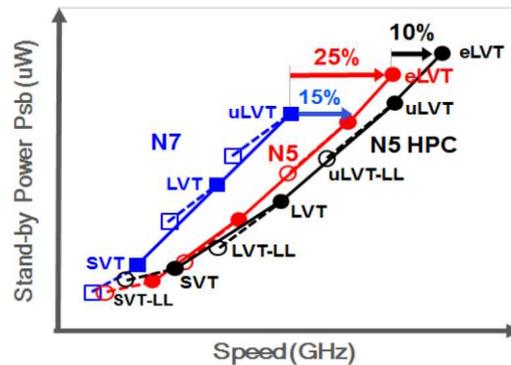


Figure 22 : Seven variants of the Fin-FET are proposed by TSMC in its 5-nm process [Yeap 2019]

In Microwind, we may only consider 3 FinFET options (Figure 23):

- Low Leakage (Standard Vt - SVT): Vt is relatively high, the FinFET do not deliver a very high current but has a low parasitic leakage current. This is the most common device. The target  $I_{on}$  value is 1.8 mA/ $\mu$ A @ 0.65 V with  $I_{off}$  10 nA/ $\mu$ m for nFET, 1.6 mA/ $\mu$ A for pFET.
- High Speed (ultra-low Vt - uLVT): Vt is very low, the FinFET delivers a high current at the cost of a high parasitic leakage current. This device is used to enhance the switching performances, for example in the critical path. The target  $I_{on}$  value is 2.3 mA/ $\mu$ A @  $I_{off}$  100 nA/ $\mu$ m @ 0.65 V for nFET, 2.0 mA/ $\mu$ A for pFET.
- High Voltage (HV): this device is used for I/Os or high-voltage analog interfaces. The devices can withstand very high voltages as may be found in drivers such as SerDes, Sata, etc.

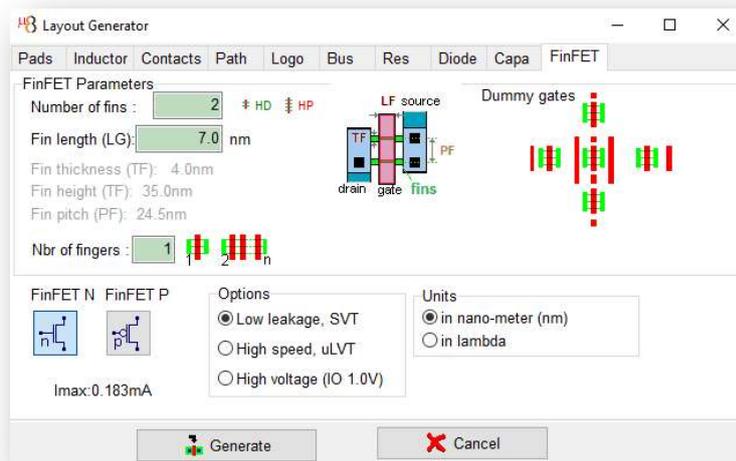
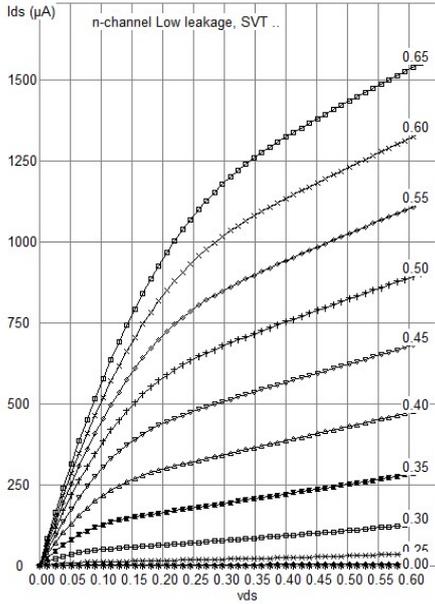


Figure 23: MOS options available for FinFET in Microwind for 5-nm node

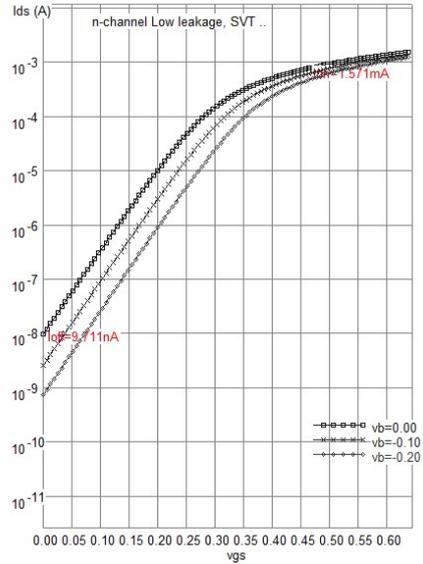
### ID/VD characteristics

We consider a 11-fin device,  $N=11$ ,  $FH=45\text{nm}$ ,  $FW=4\text{nm}$ . The resulting  $W_{eq}$  (eq. 2) is 1034 nm, close to 1  $\mu\text{m}$ .

$$W_{eq} = N \times (2FH + FW)$$

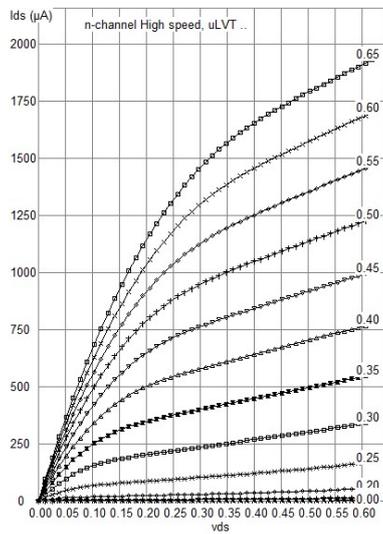


*n*-FinFET SVT – Low power:  $I_{on}=1.6$  mA

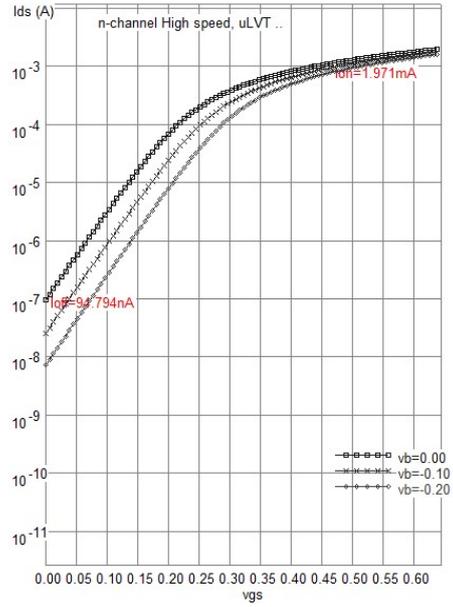


*n*-FinFET SVT – Low power:  $I_{off}=12$  nA

Figure 24: *n*-FinFET Low Power, standard  $V_T=0.3V$ ,  $I_{on}=1.6mA$ ,  $I_{off}=10nA$  @  $V_{DD}=0.65$  V



*n*-FinFET uLVT – High-Speed:  $I_{on}=2.0$  mA



*n*-FinFET uLVT – High-Speed:  $I_{off}=100$  nA

Figure 25: *n*-FinFET High Speed ultra-low  $V_T=0.25V$ ,  $I_{on}=2.0$  mA,  $I_{off}=100$  nA @  $V_{DD}=0.65$  V

Using this device in its *n*-finFET & *p*-finFET versions, we may extract  $I_{on}$  and  $I_{off}$  for default LP device and HP device, directly in mA/ $\mu$ m. Figure 24 shows the  $I_d$ - $V_d$  characteristics of the LP device (left) with its subthreshold curves (right) and Figure 25 shows the  $I_d$ - $V_d$  characteristics of the HP device (left) with its subthreshold regime (right). Having a 67 mV/decade subthreshold slope for  $T=27^\circ C$  close to [Yeap 2019], we achieve  $I_{on}$  1.5 mA/ $\mu$ m @ 0.65 V, and  $I_{off}$  10 nA, with  $V_{T0}=0.3V$ . Note that these very good performances are linked to the fact that the fin has a low depletion capacitance ( $C_p$ ).

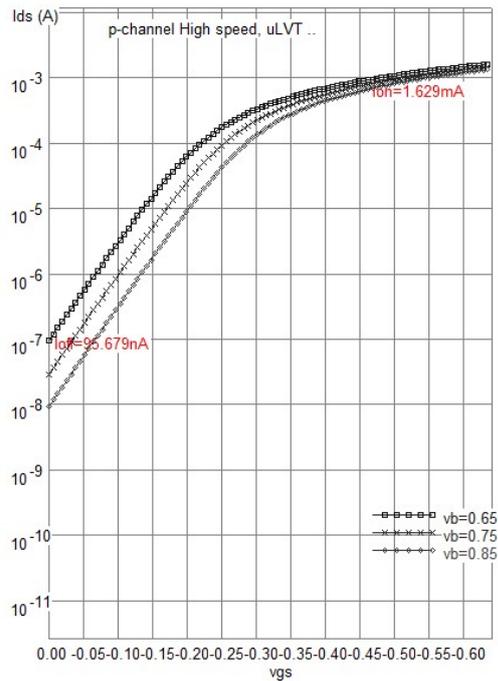
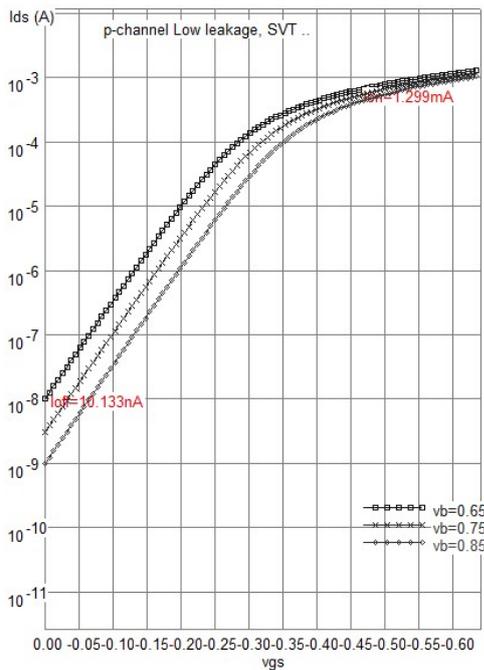


Figure 26: p-FinFET SVT :  $I_{on}=1.6mA$ ,  $I_{off}=14nA$ ; p-FinFET uLVT:  $I_{on}=1.6mA$ ,  $I_{off}=100nA$  @ 0.65 V

The previous figures may give the impression that  $I_d/V_d$  is a unique curve with limited variation. In reality, all model parameters may vary according to a statistic distribution, leading to a spread of performances instead of a unique curve, as shown in figure 27.

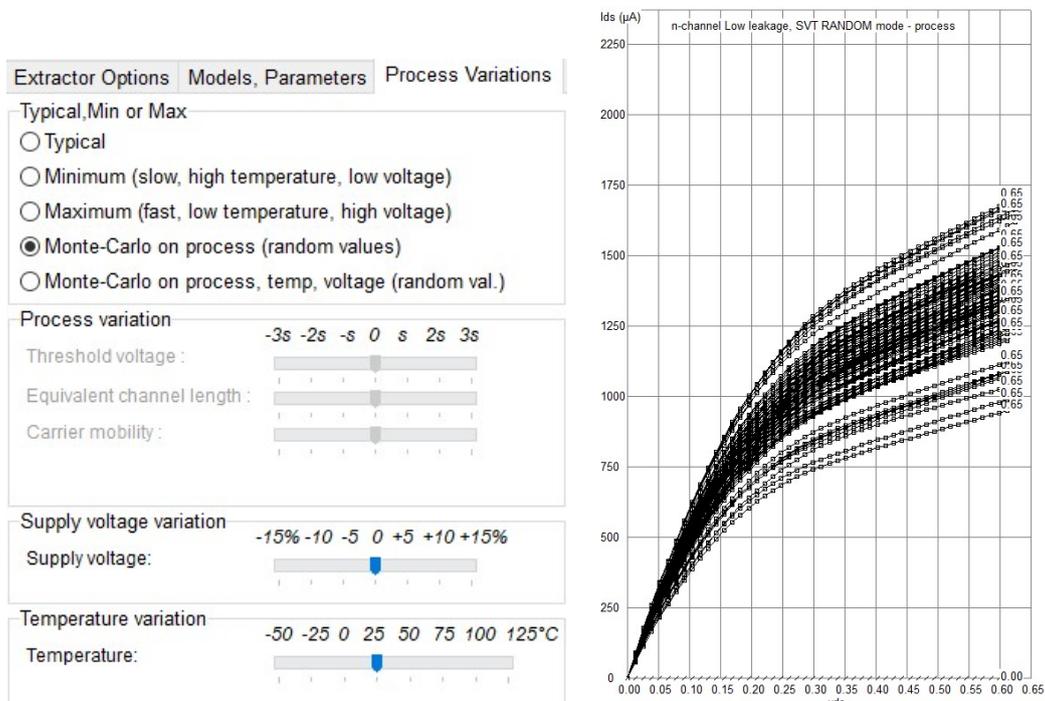


Figure 27: Plot of 100  $I_d/V_d$  with normal distribution of threshold voltage, effective width and channel mobility showing a spread in performances

## Summary of design rules

The table below summarizes the main characteristics of the 5-nm design rules implemented in Microwind.

<i>Design parameter</i>	<i>Unit</i>	<i>Code</i>	<i>Name in rule file</i>	<i>Value in 5-nm process</i>
<i>Lambda</i>	nm	$\lambda$	lambda	4.0
<i>Core supply</i>	V	VDD	Vdd	0.65
<i>Device type</i>		FinFET	finfet	1
<i>Fin Width</i>	$\lambda$	WF	R301	1
<i>Fin pitch</i>	$\lambda$	FP	R308	7
<i>Fin Height</i>	nm	HF	thdn	45
<i>Gate height</i>	nm	GH	thpoly	60
<i>Gate length</i>	$\lambda$	GL	R302	2
<i>Gate pitch</i>	nm	CGP		44
<i>Spacer width</i>	nm	SW		10
<i>Contact size</i>	$\lambda$	CS	R401	2
<i>EOT</i>	nm	EOT	b4toxe	0.85
<i>M1 width</i>	$\lambda$		R501	3
<i>M1 spacing</i>	$\lambda$		R502	3
<i>Metal Pitch</i>	nm	MP	R501+R502	24
<i>Rule file</i>				Cmos5nm.rul

Table 6: basic parameters of the 5nm process implemented in Microwind

## Interconnects

The 5-nm technology proposes up to 14 metal layers [Prasad 2019]. In Microwind, we limit the number of metal layers to 8, where metal1, metal2 are used for cells, metal3-metal4 for blocs, metal5-metal6 for macro-blocs and metal7-metal8 for the power grid (Figure 28). The parasitic resistance and capacitance of interconnects, also called *Back End of Line* (BEOL) should be considered when it comes to evaluate the circuit performance. In this section, we analyze the consequences of the metal pitch reduction on unit resistance and capacitance, from which accurate simulations of the propagation time and switching performances can be performed.

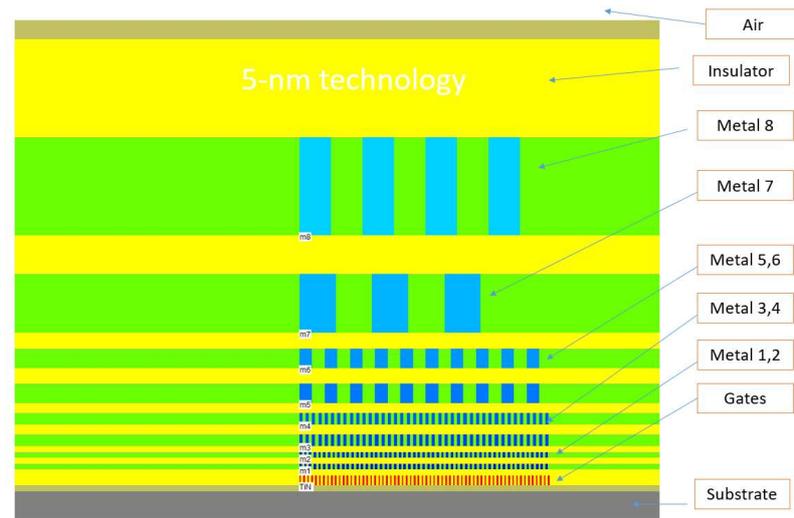


Figure 28: cross-section showing 8 metal layers (All metals 5nm.MSK)

## Resistance

The interconnect resistance has severely increased due to the reduction of metal section. As illustrated in figure 29, the usual metal1 width is 16 nm ( $4\lambda$ ) and the height is 30 nm. The exploding unit resistance (Figure 30) may be considered as one of the most important limiting factors of the scaling down, as it has reached unprecedented values in 5-nm, nearly 10 times higher than 32-nm process.

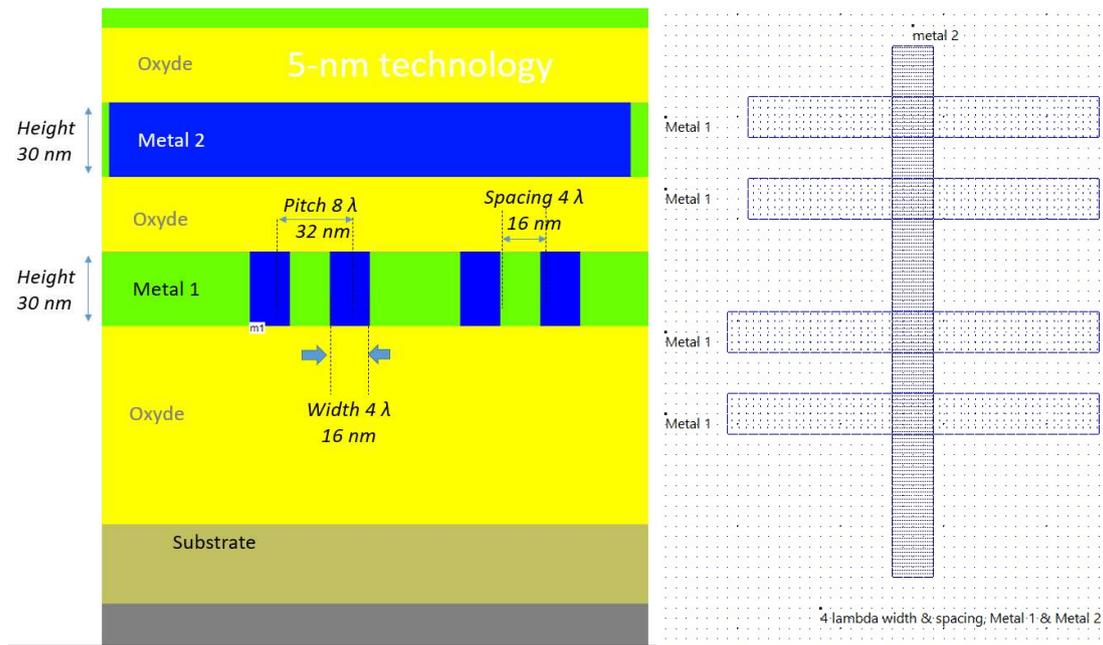


Figure 29: metal1, metal2 interconnect cross section & upper view, metal pitch  $8\lambda$  (32 nm)

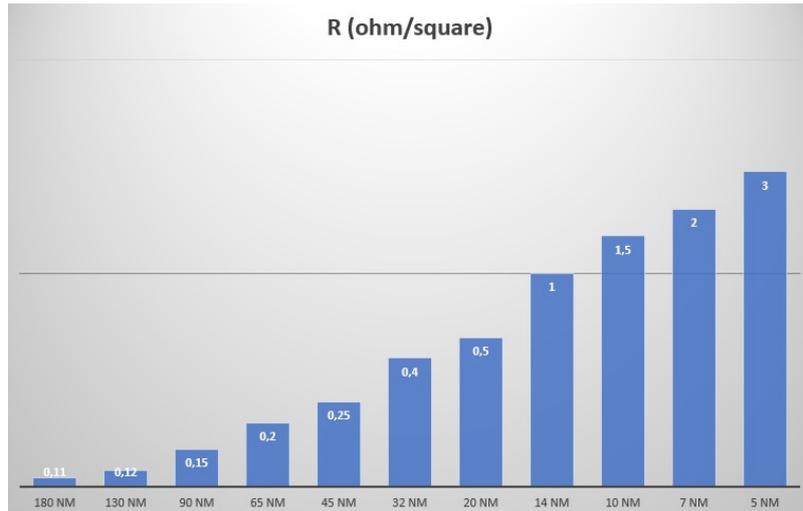


Figure 30: The resistance per square (log scale) of lower metal layers vs. technology

Design parameter	Unit	Code	Name in rule file	Value in 5-nm process
<i>Lambda</i>	nm	$\lambda$	lambda	4.0
<i>M1..2 width</i>	$\lambda$		R501, R701	3
<i>M1..2 spacing</i>	$\lambda$		R502, R702	3
<i>M1 Pitch</i>	nm	MP	R501+R502	24
<i>M2 Pitch</i>	nm		R701+R702	24
<i>M1..2 height</i>	nm		Thme, thm2	30
<i>Via1 height</i>	nm			25
<i>M1..2 Resistance</i>	$\Omega/\mu\text{m}$	Unit Res.	Reme, rem2	250
<i>M1..2 capacitance</i>	aF/ $\mu\text{m}$	Unit Capa.		300
<i>Rule file</i>				Cmos5nm.rul

Table 7: basic parameters of the 5nm process implemented in Microwind

The unit resistance  $250 \Omega/\mu\text{m}$  corresponds to  $3 \Omega/\text{square}$ , assuming the minimum width & spacing  $3 \lambda$ . We tune the Microwind RUL file using `reme = 3, rem2 = 3` (Table 7). The aspect ratio of metal1 & metal2 tracks at  $4 \lambda$  width,  $4 \lambda$  spacing (such as used in routing wires) is around 2, means that the height (30 nm) is more than twice the width (16 nm).

The interconnect is made of copper. Alternative metals such as Cobalt (Co) and Ruthenium (Ru) have been investigated in [Badaroglu 2017]. Surprisingly, the good old Aluminum (Al) in its dual damascene version is explored as a potential candidate to reduce by 50% wire and via resistance compared to Copper.

### Capacitance

The capacitance per unit length has not followed the exponential trend observed for resistance, fortunately. However, the shorter distance between tracks makes lateral coupling with adjacent interconnects more and more dominant. Based on [Yoon 2019] [Badaroglu 2017], we fix the unit capacitance for lower M1 & M2 to around  $300 \text{ aF}/\mu\text{m}$ , which corresponds to `cmobody = 100, cmelineic = 150`. Consequently, a  $1 \mu\text{m}$  metal1 interconnect is equivalent to a  $300 \text{ aF}$  capacitance. It also corresponds to a minor increase as compared to 7-nm ( $270 \text{ aF}/\mu\text{m}$ ) and 10-nm ( $250 \text{ aF}/\mu\text{m}$ ).

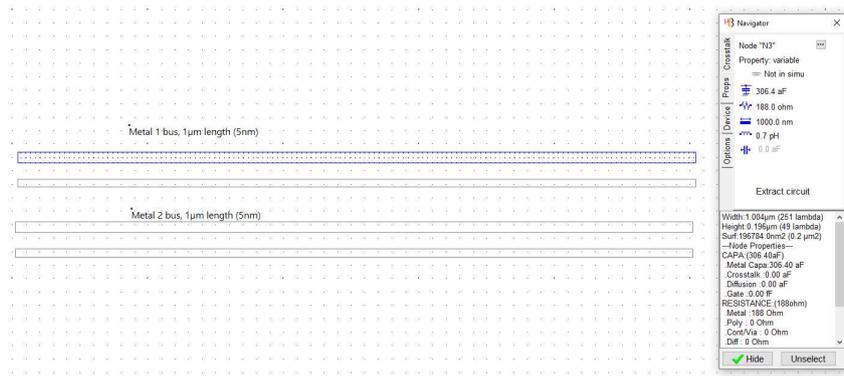


Figure 31: Extracting the R & C values from a metal 1 bus, minimum width & spacing, length 1µm (metal-1um.MSK).

One possibility to limit the rise of the interconnect capacitance consists in inserting an air-gap instead of low-k dielectric between interconnects, a solution which was discussed for the 14-nm technology by [Natarajan 2014].

## Nano-CMOS cell design

### Design for manufacturability

The EUV photolithographic process differs from the mainstream 193 nm immersion process in several ways, as described by [Wu2020]: shadowing effect, horizontal-vertical linewidth difference, mask 3D scattering effect, photon absorption stochastics, and aberration sensitivity. Patterning defectivity can cause line micro-bridges, broken lines, missing or merging contacts as shown in Fig. 32.

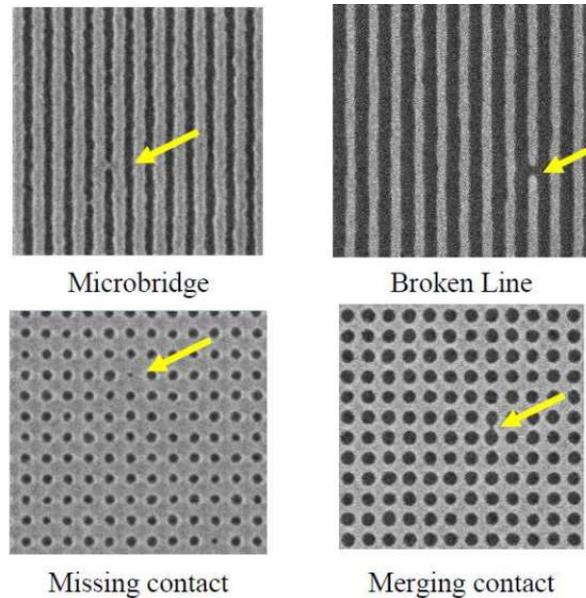


Figure 32: random failures observed from EUV resists after exposure and development [Wu 2020]

We need to match the fin alignment with very regular spacing following the fin pitch, but also keep active gates and dummy gates very regular following the gate pitch, and once connecting to the upper metal layer, comply with the metal routing pitch (Figure 33). In these conditions, the design is manufacturable. In Microwind, the command `Edit > Generate > Tracks` simplifies the task of generating fins (Fin pitch), gates (Contact pitch) and metal tracks (track pitch).

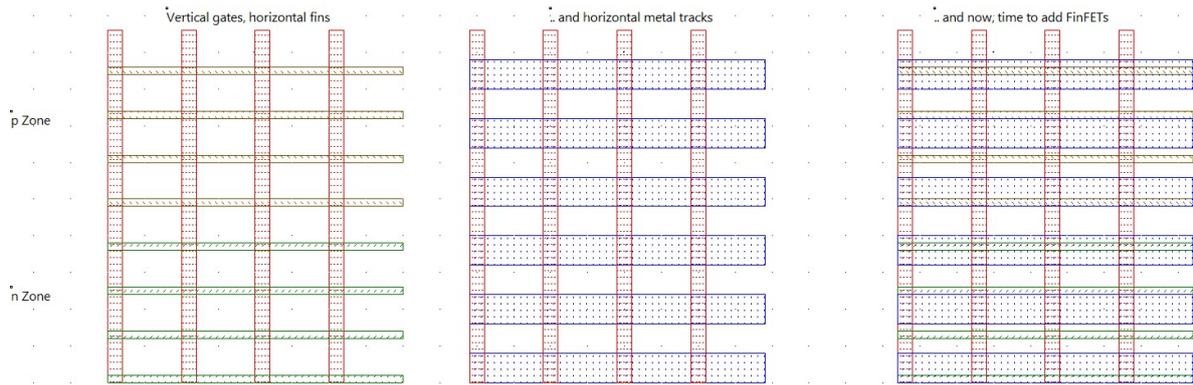


Figure 33: Complying with fin pitch, gate pitch & metal pitch to design a manufacturable device (routing grid.MSK)

In other words, we start with predefined fin tracks, gate tracks & metal track. The devices are placed on a grid driven by the gate pitch in horizontal axis, and the fin pitch in vertical axis (Fig. 26-left). The routing grid is defined by the metal pitch (Fig. 33) in Y and gate pitch in X. Design rules introduced by sophisticated multiple-patterning technologies and EUV lithography make the placement & routing scenarios much more rigid and difficult than before. An example of placement of 2-Fin & 3-Fin devices in n & p fin regions is reported in Fig. 34.

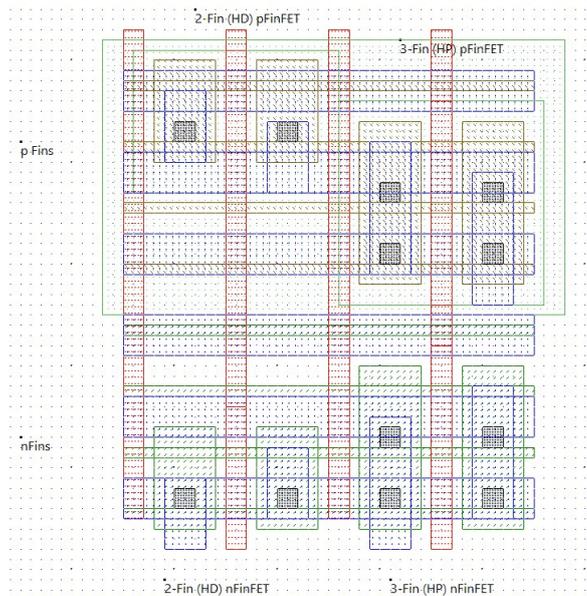


Figure 34: Adding FinFETs to the routing grid (routing grid finFets.MSK)

### Counting tracks

Logic cell libraries often refer to the « T-track » metrics, like « 8T – High performance » or « 6T – High density ». Values like 5T, 6.75T, 7.T may also be found in the literature. The number prior to « T » refers to the number of possible horizontal metal tracks that can be routed on top of the devices. In the 6-Track cell design, 5 tracks are used for signal, and 2 half-tracks are dedicated for power. The reason we only count ½ track per power is that power rails are usually shared between adjacent cells. The acronym 6T should not be confused with 6T-SRAM where “T” means transistor, that we shall analyze later in this paper.

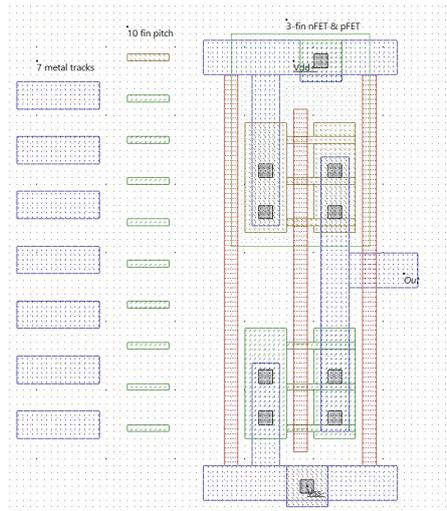


Figure 35: design of a high performance 3-fin inverter, 7 Track design (inv 3 fins.MSK)

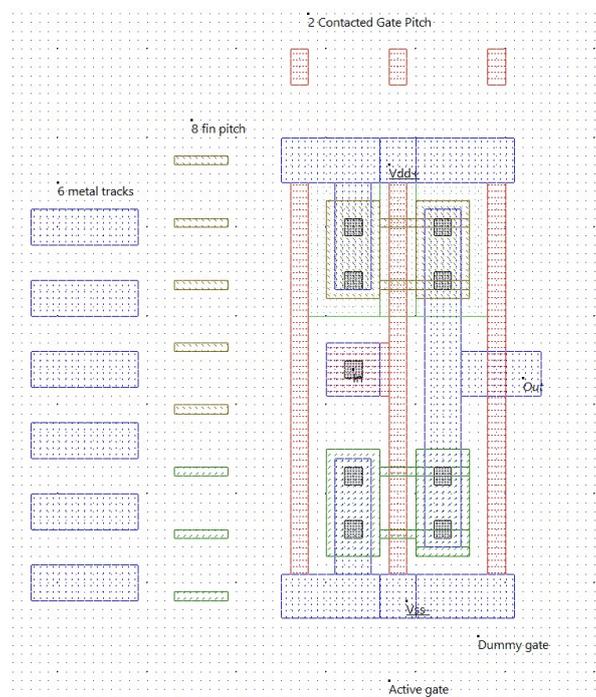


Figure 36: design of a high density 2-fin inverter using a 6-Track design (inv 2Fin.MSK)

If we use 3-fin devices (High performance) both for nFET & pFET, with a contact gate pitch of 42 nm and fin pitch of 28 nm, we obtain the “7.5 T” layout of Fig. 35. Seven horizontal tracks do not fit exactly in between the VDD/VSS supply area, which justifies 6.5T plus 2 half-tracks for power, that is 7.5 tracks.

Moving to the « high density » design style with 2-fin devices provides enough space for 5 horizontal metal tracks (plus half of the power tracks), which uses 20% less silicon area as compared to the previous design (Figure 35 vs figure 34). Further gains may consist in using only 1-fin devices (5-Tracks), as mentioned in [Badaroglu 2017], or even stacked nFET & pFET, a revolutionary 3D approach that could boost integration by a considerable factor in future nodes [Mokuta 2018].

## Performances

### Intrinsic delay

The intrinsic performances of a gate may be evaluated using the formulation provided by [Yoon 2019] inspired from [Na 2002]. Note that we replace  $2 \times I_{eff}$  included in the original formulation by  $I_{on}$ .

$$\text{Intrinsic Delay} = C_{gg} \frac{VDD}{I_{on}}$$

Where

- VDD is the power supply (0.65 V in 5nm) in V
- $I_{on}$  is the maximum current in A (0.3 mA for 2-fin LP)
- $C_{gg}$  is the total node capacitance (0.3 fF)

Concerning  $C_{gg}$ , values around 50-100 aF may be found in the literature for 2-fin FinFET used in 5-nm technology. If we consider 2 devices in a logic gate input (one n-FET, one p-FET), one input load corresponds to 100-200 aF. The output capacitance including BOEL and MOEL depends on the metal layer, contact and interconnect length, and may be estimated to 200 aF. As an example, the NOR2 output connected to one inverter input has an estimated equivalent capacitance around 0.3 fF (Fig. 36). Consequently, the intrinsic delay is around 0.65 ps.

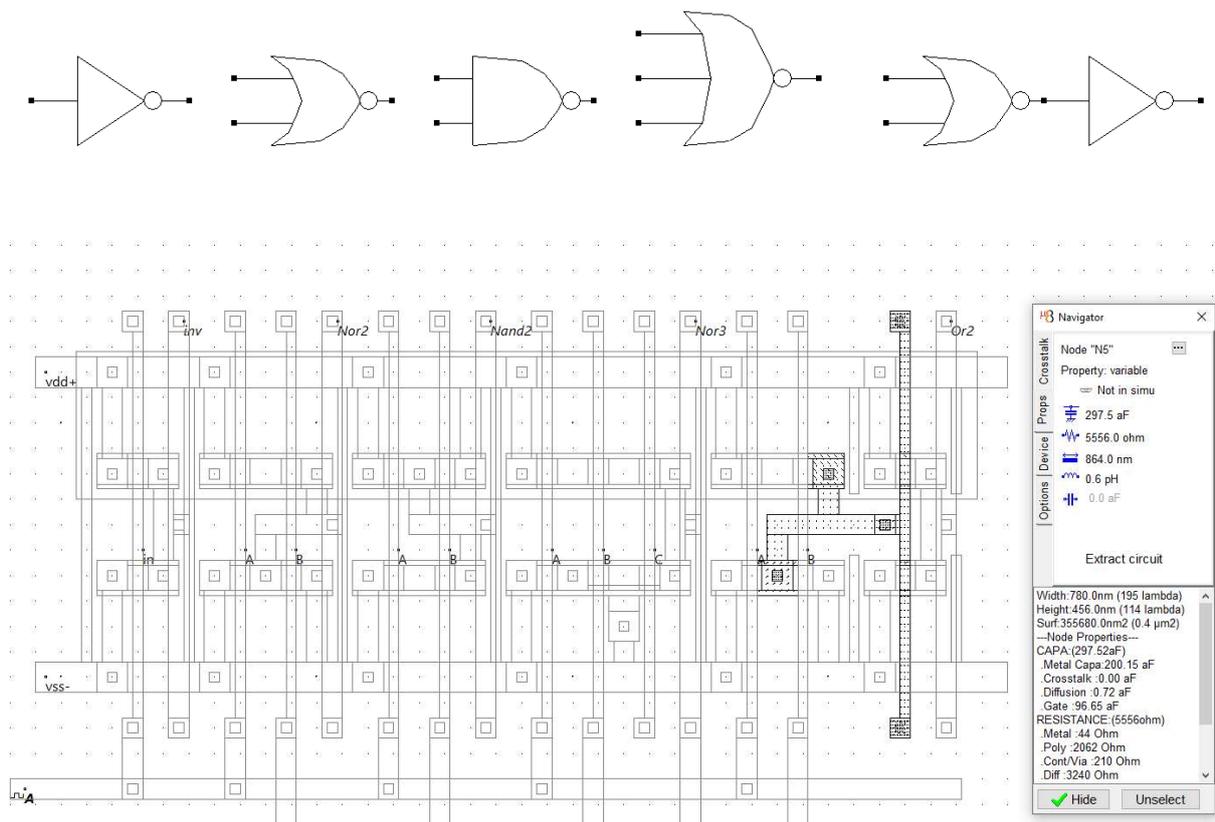


Figure 36: evaluation of the global net capacitance to extract the intrinsic delay (basic gates.MSK)

## Fan-out

The intrinsic delay extracted from the previous formulation (650 fF) do not represent the real-case operating conditions. Two important parameters should be considered: the loading (Fan-Out) and the interconnect delay (RC effect). The term “Fan-Out - FO” accounts for the number of gates connected to an output node.

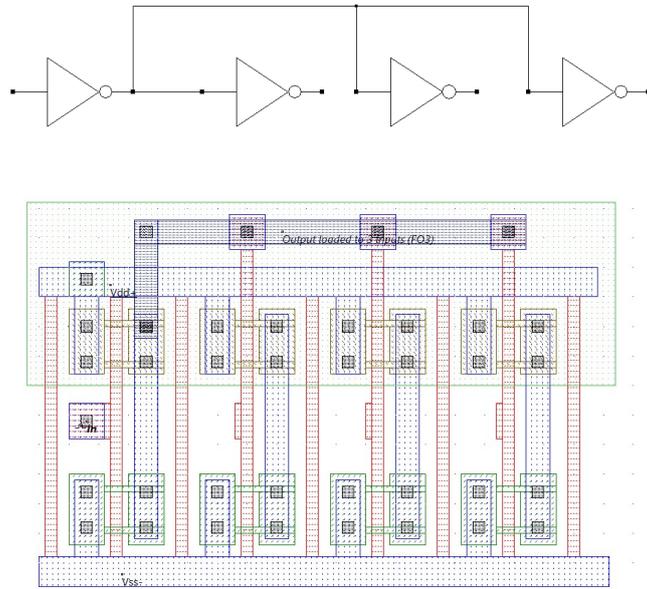


Figure 37: A 2-fin inverter with 3 inverter gates connected to its output (inv FO3.msk)

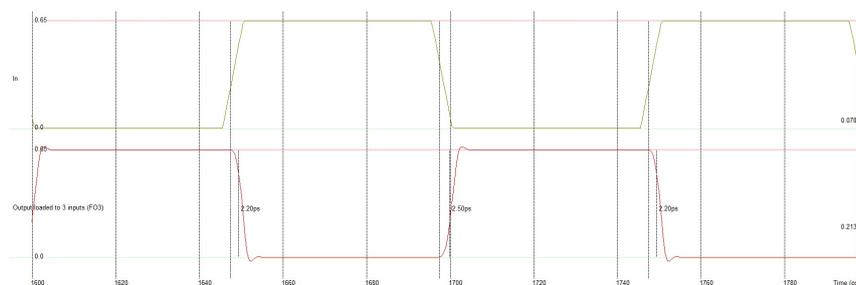


Figure 38 : Switching of a 2-fin inverter in FO3 loading conditions (inv FO3.msk)

For example, FO3 means that one gate output is connected to 3 gate inputs (Fig. 37). Two other acronyms are included in the figure: “MOL” (Middle-of-line) accounts for R & C parasitics linked to internal contacts & interconnects close to the gate, while “BEOL” (Back End-of-line) is dealing with metal interconnects which link the gate to the outside world. The immediate consequence of this load is to slow down the switching delay (measured between 50% in and 50% out), which is around 2.5 ps (Fig. 38).

## Ring-Oscillator performances

In figure 38, we consider 3 stages of inverters (RO3) loaded with 3 gates each (FO3). We use 2-fin FinFETs for n & p devices, for all stages, which is the common standard in 5-nm. The device option by default is low-power, around 2nA *I<sub>off</sub>* and 0.35mA *I<sub>on</sub>*. We use short to medium metal tracks to connect inverter stages.

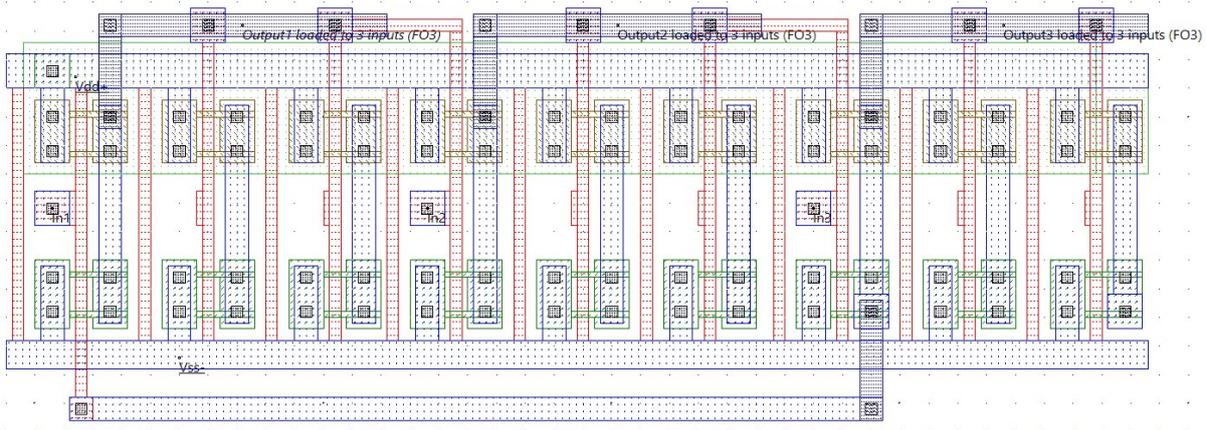
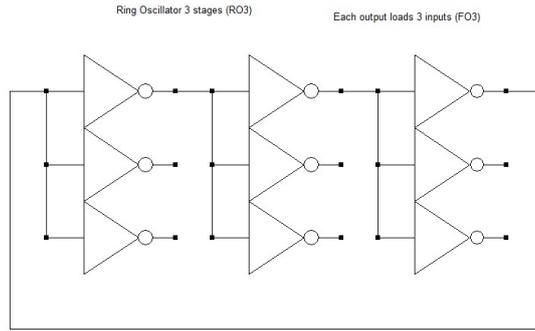


Figure 38: Design of Ring Oscillator, each stage with 3 inverter gates connected to its output, gate 2 fins, gate pitch 44 nm (RO3-FO3.MSK)

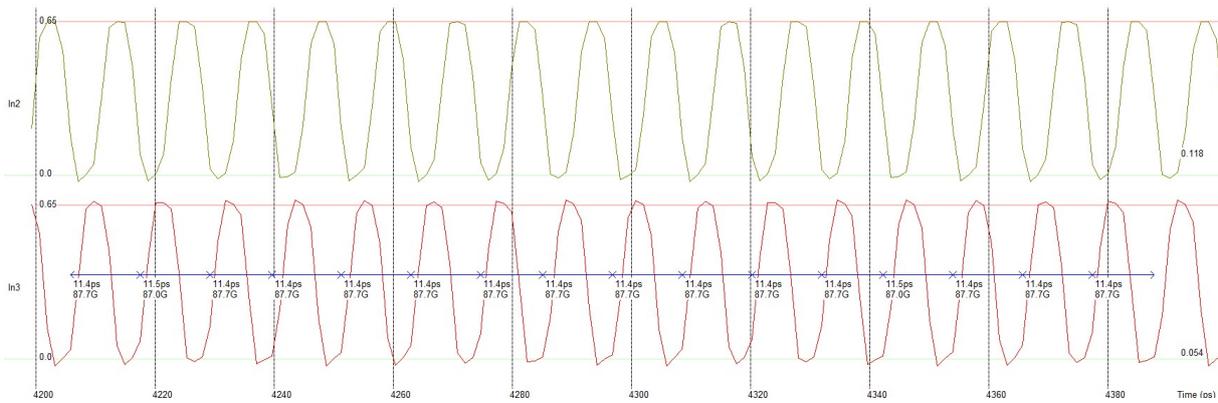


Figure 39: Simulation of the Ring Oscillator with FO3 (RO3-FO3.MSK) reaching 90 GHz

The simulation shows an oscillating frequency around 90 GHz ring for low-power version, and 115 GHz for high-performance version at nominal voltage 0.65 V. If we consider VDD ranging from 0.5 to 0.8V, we may evaluate the power dissipation per stage versus the ring oscillator frequency that we can compare with publications such as [Ryckaert 2019][Samavedam 2020]. The trend is to go faster while consuming less power (Fig. 40). The prospective performances of 3nm & 2nm are also shown, as published in [Samavedam 2020].

RO3, FO3,  $W_{eq}=188nm$ , 2-fin FinFET, loaded with BOEL & MOEL

Active power per stage ( $\mu W$ )

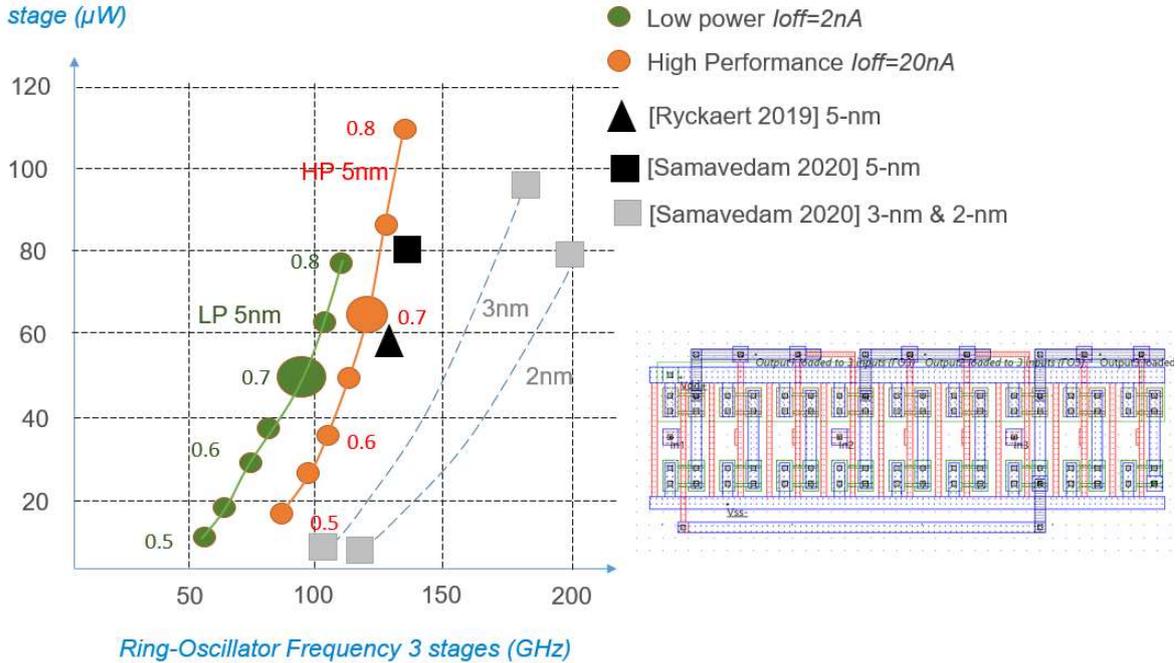


Figure 40: comparing active power per stage vs the ring oscillator frequency with 3 stages, for various VDD voltages in 5-nm

### Loading with long interconnects

Another strategy for performance characterization consists in loading the inverter outputs with a significant portion of interconnect, which is very common to connect cells together. In [Yoon 2019] a distinction is made between short, medium and long interconnects, based on the contacted gate pitch (CGP).

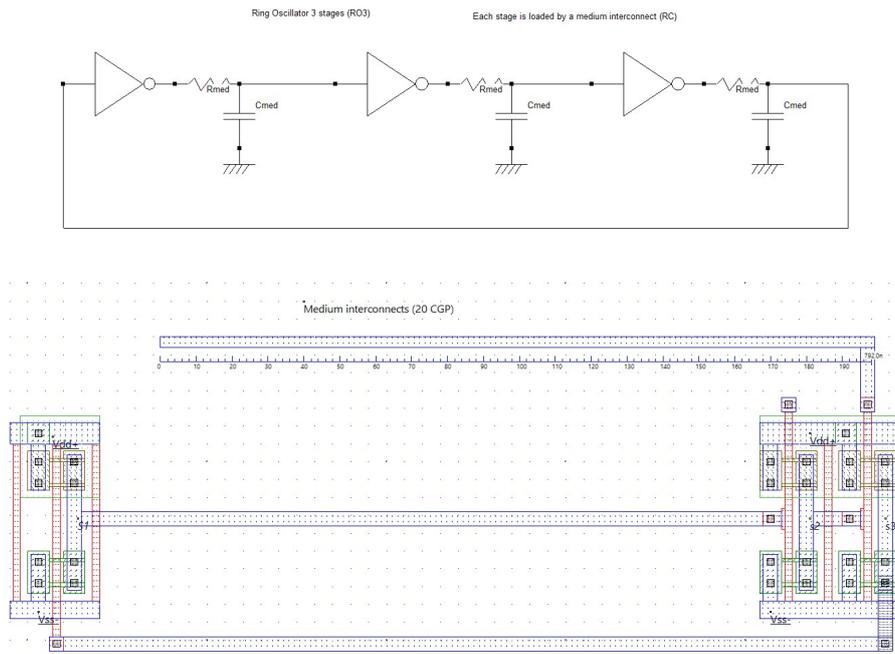


Figure 41: medium interconnects around 20 CGP (800 nm, RO3-FO1-Medium.MSK)

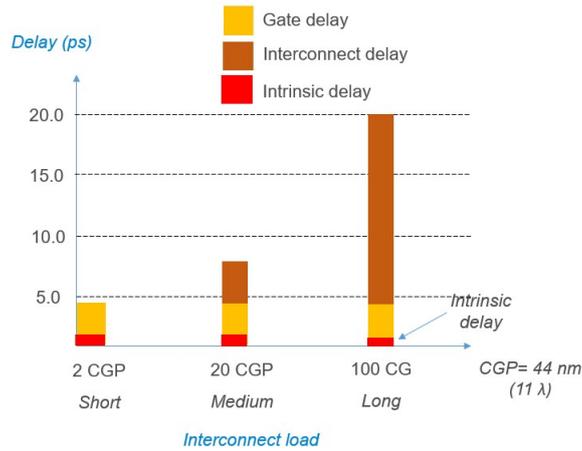


Figure 42: delay increase with interconnect length (metal1, 4 λ width)

Proposed values range from 2 CGP for short tracks (100 nm), medium tracks 20 CGP (1 μm) to 100 CGP (5 μm) for long interconnect wires. Short tracks are used within logic cells, medium tracks are used to connect cells and blocs together, while long tracks are commonly used for internal buses and at macro-bloc level.

Respective delays for long, medium and long interconnects are evaluated to 4ps, 7ps and 20 ps (Figure 41), close to the values published by [Yoon 2019]. Intrinsic gate delays are mainly due to the input and output capacitance for short interconnects, whereas interconnect RC parasitics are responsible of the important delay increase when connected to long interconnects.

## Design of logic cells

The cell compiler of Microwind is used to generate basic cells such as INV, NAND, NOR gates, but also any complex gate based on combinations of “&” (AND), “|” (OR) and “~” operators (Fig. 43). Figure 44 shows examples of basic gates with, from left to right: an inverter, a NOR2 gate, a NAND2 gate, a NOR3 gate and a OR2 gate. The order of magnitude of the cell delay is 1-2 ps, but the output are not loaded (Fan-Out 0) which leads to optimistic switching speed predictions.

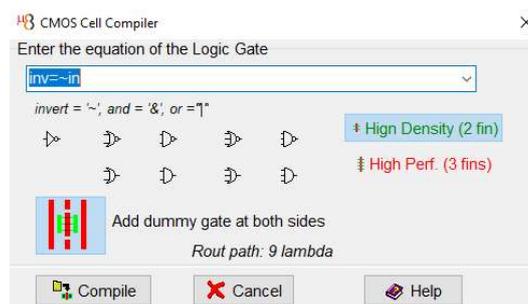
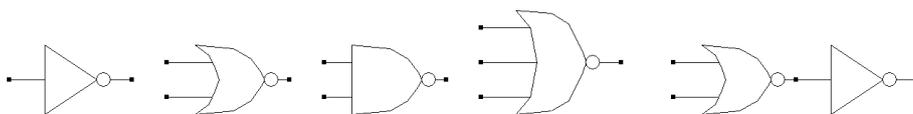


Figure 43: The cell compiler is used to generate cells automatically



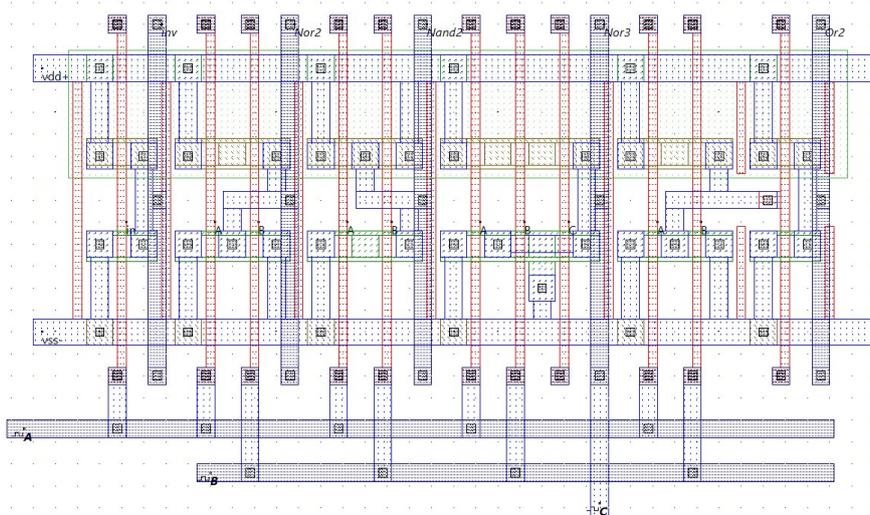


Figure 44: Examples of basic gates generated by the cell compiler (basic gates.MSK)

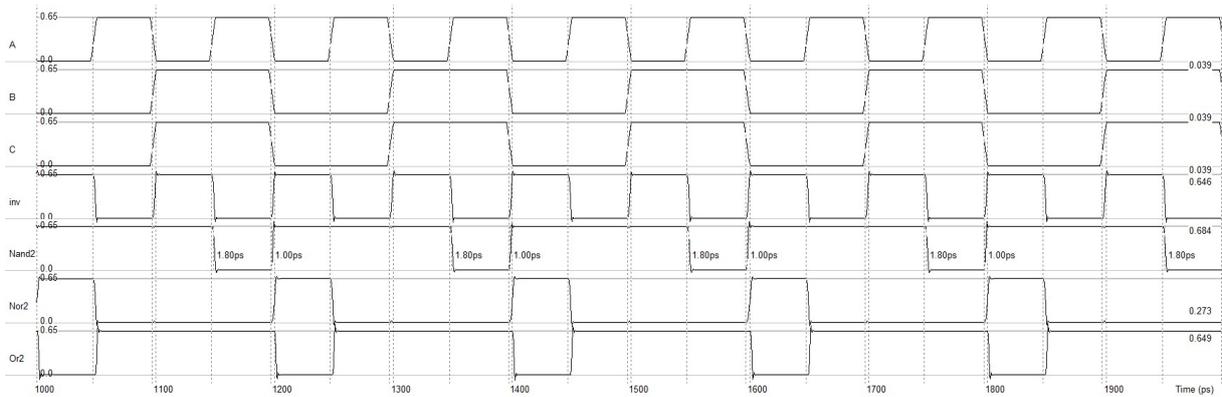
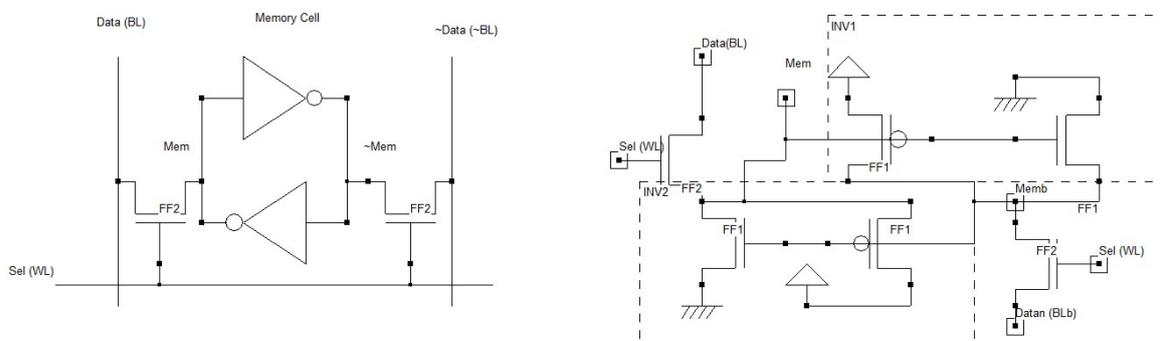


Figure 45: Simulation of basic gates generated by the cell compiler (basic gates.MSK)

## Design of a static memory

A 6-transistor (6T) static memory cell (SRAM) was disclosed by TSMC [Yeap 2019] with a cell size around  $0.021 \mu\text{m}^2$ , which enables the implementation of around 32 Mbyte of memory/ $\text{mm}^2$ . In our implementation of the 6T-SRAM with 2-fin access device and 1-fin memory inverters, we get a cell size of  $0.020 \mu\text{m}^2$  (Fig. 46).



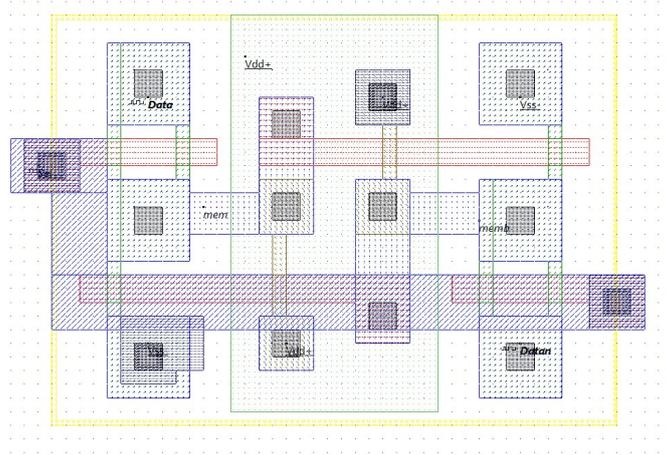


Figure 46: design of a 6T 2-fin static RAM (sram-6T-HD-5nm.msk)

According to [Yeap 2019], the SRAM operates at VDD as low as 0.3V. We simulate the read and write cycles with alternating 0 and 1 on *Data* (and inverted 1 and 0 on *Datan*). As shown in the chronograms of Figure 47, the memory is selected when *Sel*=1. At time 1.2, the memory stores 0, at time 2.0, the memory stores a 1, and at time 3.0, the memory stores again a 0. At time 4.0, *Data* and *Datan* are high impedance, so the memory is in Read mode. As there is no load, the delay is less than 0.2ps.

The same write & read cycles are simulated at VDD=0.25V. It can be seen that the write delay is significantly increased (15 ps for writing a 0, 6.5 ps for writing a 1), but the memory is still functional.

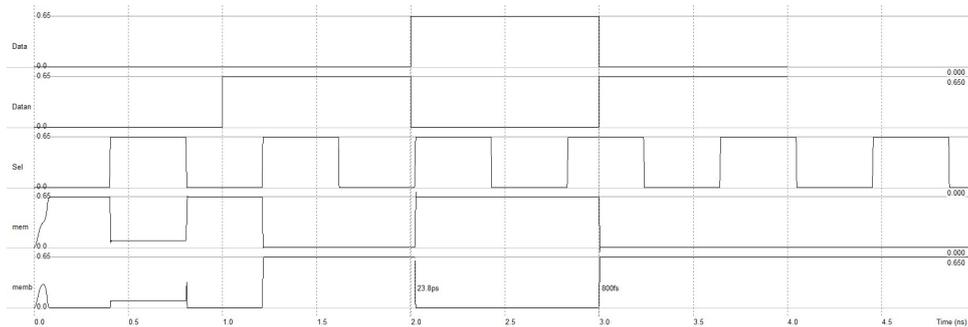


Figure 47: Write & Read cycles at nominal VDD 0.65 V

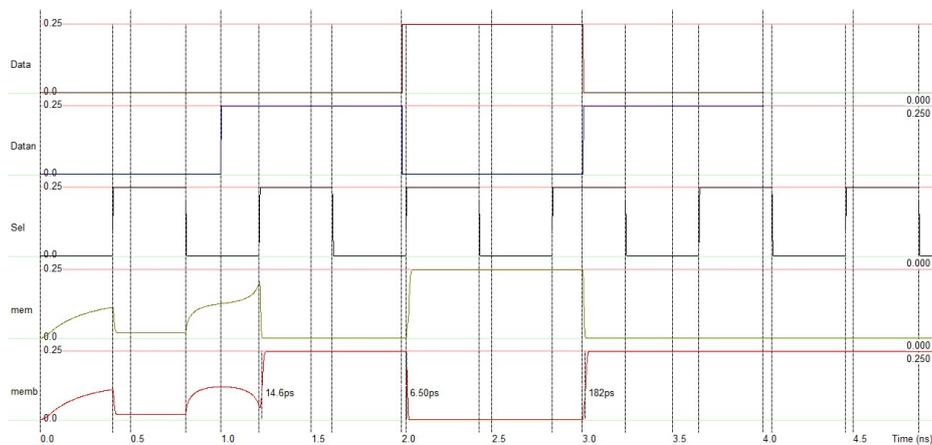


Figure 48: Write & Read cycles at VDD=0.25V

## Conclusion

This application note has described the implementation of the 5-nm technology in the educational tool Microwind, which appears to be very similar to the 7-nm process in terms of layout design rules and voltage supply. The 2-fin approach for FinFET design is a main trend at 5-nm technology, with little use of larger devices such as 4-fin FinFET previously available in 7-nm technology. Significant progresses have been made by introducing a new generation of FinFET device which improves the switching performances and enables interesting gains in terms of power consumption, as compared to previous nodes such as 14, 10 and 7nm. We discussed in this paper about the transistor characteristics, the performance tradeoff, the interconnect parasitic effects and the performances of basic cells such as logic gates, ring oscillators and memory cells.

For the first time however, the design unit “lambda” has been kept identical to the 7-nm node, and limited gains in terms of geometrical scale down are foreseen in future nodes, which is a major breakthrough in the general trends that have paved the way for the semiconductor history over the last 50 years. While the gate pitch and metal pitch in 3,2 and 1nm nodes should remain comparable to 7-5nm nodes, the cell size should be significantly reduced thanks to innovative approaches in the device architecture, power supply strategy and co-design of n/p devices, which would enable further benefits in terms of integration complexity and overall performances.

## Acknowledgements

We gratefully acknowledge Vinay Sharma for his valuable suggestions as well as the numerous students, researchers and engineers who have used our applications notes related to 32, 25, 14, 7 & 5-nm technologies, and published more than 600 scientific papers using Microwind. This motivates us to release new application notes dedicated to the nano-cmos technologies of the future.

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authored more than 80 journal and conference papers on research work including transport for ultra-scaled MOSFET with UTEOT high-k dielectrics on bulk and UTTB-FDSOI, on ReRAM modelling, STT-MRAM circuits, GaN SBD-GET and HEMT devices, TFET and FinFET based SRAM circuits, ULP-OTA design, hardware implementation of IA algorithm on FPGA. He currently works on IC design coupled with sensor and Harvester energy devices and to implement Artificial Neural Network based IC.

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