Analysis and Implementation of OVSF Address Decoders

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***Abstract*—Demand for Internet of Things (IoT) devices has generated interest in fault-tolerant address decoders. Address decoders affect the energy required to establish a data link and monitor a wireless channel through metrics such as detection probability and false alarm probability. This brief establishes a framework for calculating detection and false alarm probabilities and shows that limiting the number of correctable errors eliminates simultaneous false alarms, reduces the probability of false alarm, and reduces the maximum normalized power consumption of a sleep node due to false alarms by 16.9 dB. The probability expressions are formulated so that the detection probability, the false alarm probability, the energy to transmit, and the power to monitor a channel can be adjusted digitally, yielding a counter-based implementation that reduces the energy consumption of the address decoder to 1.3 pJ/bit for a data rate of 200 bps in 0.18 μm CMOS.**

***Index Terms*—Wake-up receiver, detection probability, false alarm probability, and OVSF.**

I. Introduction

The demand for long-lasting battery-powered Internet of Things (IoT) devices has accelerated research on wake-up receivers (WuRx) [1], which awaken devices on-demand. Energy savings are achieved by placing the main radio (illustrated in Fig. 1(a) as TX/RX) in sleep mode and enabling it occasionally with an always-on wake-up receiver that uses two orders of magnitude less power [2]. The selective awakening is achieved by post-processing the beacon in the baseband with a correlator circuit (also known as an address decoder) [3].

The correlator circuit compares the address embedded in the beacon with that of the node and turns on the node if a match is found. The correlator can be implemented with an analog circuit [4], or a digital circuit requiring synchronization [3], [5]-[6], oversampling [7]-[10], or bit-level duty cycling [11]-[12].

The synchronized correlators use a preamble and are less susceptible than oversampling correlators to false detection of a *non-existent* address (false positives) [3]. Furthermore, by encoding the address with error-tolerant codes such as orthogonal variable spreading factors (OVSF) [6], the detection probability (p_s)-the probability that a message from node k is detected by node i in Fig. 1(b)-is increased.

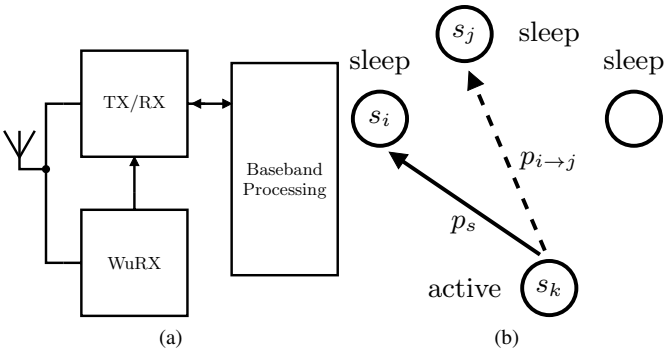


Fig. 1. (a) A block-level diagram of a wireless node assisted by a wake-up receiver (WuRX). TX/RX is the main radio. (b) Illustration of a detection that occurs when a wake-up packet is decoded correctly by a target node (i) and a false alarm that occurs when a node (e.g. j) is falsely awakened.

p_{fa} is the probability that a node is falsely awakened by a packet meant for another node. p_{fa} of an error-tolerant OVSF address decoder is different from that of a pseudo-noise (PN) address decoder discussed in [3]. p_{fa} is a function of the number of sleep nodes (N_S); the diverse bit error rate ($p_{b,ij}$); and $p_{i\to j}$, the probability that a node (in this case, i) is falsely awakened by another node (j). The p_{fa} derived in this brief differs from that discussed in [13] in three ways. First, p_{fa} is a function of N_S and $p_{b,ij}$. Second, $p_{i\to j}$ is derived by limiting the number of correctable errors. As a result, $p_{i\to j}$ is minimized, simultaneous false alarms are eliminated, and the maximum normalized power consumption of a sleep node due to false alarms is reduced by 16.9 dB. Finally, expressions for p_s and p_{fa} are formulated so that p_{fa}, p_s, and increases in the power consumption of the sleep nodes due to false alarms ($P_{t,fa}$) can be adjusted digitally, yielding a reconfigurable counter-based implementation that reduces the energy-per-bit of similar lengths and data rates in [8] and [12] by 2.96 times.

The rest of this brief is organized as follows. In Section II, we develop the definition of p_s and p_{fa} and their relationships to E_s and $P_{t,fa}$. We derive the equations for p_s and p_{fa} in Section III. We compare the calculations with the simulations, glean design insights from the results, and explore implementation issues in Section IV. Finally, we present our conclusions in Section V.

II. Mathematical Formulation

Figure 1(b) shows a set of wireless nodes operating in the active mode momentarily to conserve energy. Each node is identified by an L-bit address (e.g., s_k). The transmission starts when a packet, which includes a preamble and an address (e.g. s_i), is sent from an active node (i.e., node k) to one of the

N_S sleep nodes (i.e., node i). The remaining sections of this brief assume that the preamble has been detected and hence that p_s and p_{fa} are determined by the address decoder.

A. Detection

The detection probability (p_s) can be formulated mathematically as follows:

$$p_s = \sum_k \left[\sum_{i \neq k} p(k \to i|i) p(i) \right] p(k). \quad (1)$$

$p(k)$ represents the probability that one of the $N_S + 1$ nodes (e.g., k) is chosen to transmit a wake-up message. $p(k)$ is $1/(N_S + 1)$ if any node is just as likely as any other node to transmit a wake-up message. $p(i)$ is the probability that one of the N_S nodes in the sleep mode is chosen as the recipient. $p(i)$ is $1/N_S$ if any one of the N_S nodes is just as likely as any other N_S nodes to be designated as the recipient. $p(k \to i|i)$ represents the conditional probability that a wake-up message is detected successfully by node i once node i has been chosen by node k as the recipient. It can be shown that

$$\sum_{i \neq k} p(k \to i|i) p(i) = \frac{1}{N_S} \sum_{i \neq k} p(k \to i|i) = p(k \to i|i). \quad (2)$$

Therefore, for a given bit error rate (p_b) (or signal-noise-ratio (SNR)) and a set of identically constructed nodes, p_s is

$$p_s = p(k \to i|i). \quad (3)$$

p_s is not a function of N_S and can decrease significantly as the SNR of the receiver deteriorates. Using the approach in [14], the energy consumed by the source node to send a wake-up packet (E_S) after m attempts is

$$E_s = \frac{1 - (1 - p_s)^m}{p_s} E_{s0}, \quad (4)$$

where E_{s0} is the energy required to transmit a packet, toggle the main radio in the source node between TX mode and RX mode, and monitor the channel for acknowledgment. $(1-(1-p_s)^m)/p_s$ is the average number of retransmissions. Equation (4) shows that the energy consumed by a source node to send a packet increases when p_s (or SNR, and hence p_b) is reduced.

B. False Alarms

A false alarm occurs when a node is awakened by a wake-up packet meant for another target node. The false alarm probability (p_{fa}) is

$$p_{fa} = \sum_{i \neq k} \sum_{j \neq i, j \neq k} p(k \to j|k \to i) p(k \to i), \quad (5)$$

where $p(k \to i)$ is the probability that node k sends a message to node i. $p(k \to j|k \to i)$ is the probability that node j receives a message sent to node i by node k and is dependent on $p_{b,ij}$, the probability that a bit is flipped as it is transmitted from node k. $p(k \to j|k \to i)$ can be expressed as $\alpha_{ij} p_{i \to j}$, where $p_{i \to j}$ is $p(k \to j|k \to i)$ of a set of nodes with an identical p_b and where the diverse $p_{b,ij}$ is captured by α_{ij}.

$$p_{fa} = \sum_{i \neq k} \sum_{j \neq i, j \neq k} \alpha_{ij} p_{i \to j} p(k \to i) \quad (6)$$

As there are N_S nodes, $p(k \to i)$ is $1/N_S$. p_{fa} becomes

$$p_{fa} = (N_{S,eff} - 1) p_{i \to j}, \quad (7)$$

where $N_{S,eff} = \frac{1}{N_S} \sum_{i \neq k} \sum_{j \neq i, j \neq k} \alpha_{ij} + 1$. As $p_{b,ij}$ is not known *a priori*, α_{ij} is assumed to be 1. $p_{b,ij}$ and $N_{S,eff}$ become p_b and N_S, respectively. For a given p_b, p_{fa} is

$$p_{fa} = (N_S - 1) p_{i \to j}. \quad (8)$$

Unlike p_s, p_{fa} is a function of N_S, because a message intended for i can be received by $N_S - 1$ nodes other than i and k, whereas for p_s to be counted as a message received, a wake-up message can be received only by node i.

False alarms increase the power consumption of a sleep node ($P_{t,fa}$), which is approximately

$$P_{t,fa} \approx \lambda p_{fa} \frac{1 - (1 - p_s)^m}{p_s} E_{fa}, \quad (9)$$

where λ is the rate of packet traffic, m is the maximum number of retransmissions, and E_{fa} is the energy spent by the target node to transmit a false acknowledgment and switch the main radio from a transmit mode to a receive mode. $P_{t,fa}$ is proportional to p_{fa} and increases as p_b (and p_s) is reduced.

III. Analysis

A. Orthogonal Variable Spreading Factor Address Code

The OVSF code is used in 3G wireless communication to minimize interference between different wireless channels [15]. An OVSF sequence of length L can 1) support L distinct addresses, with each sequence separated from another by $L/2$ bits; 2) correct up to $\epsilon_{max} = L/4 - 1 - T$ bits, where T is an integer that can be adjusted digitally; and 3) be generated from an OVSF sequence of length $L/2$, as shown in (10).

$$[H_2] = \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix} \to [H_4] = \begin{bmatrix} H_2 H_2 \\ H_2 \overline{H_2} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix} \quad (10)$$

$\overline{H_2}$ is the inverse of H_2. The shaded entries in (10) represent the *non-distinguishable positions* (N_p) and are occupied by bits *shared* between two OVSF sequences. The non-shaded entries in (10) represent the *distinguishable positions* (D_p) and are occupied by bits that distinguish two OVSF sequences.

B. Detection Probability

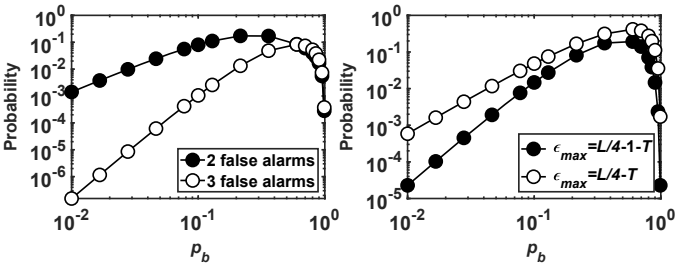
p_s is the probability that a wake-up message from node k is detected by node i:

$$p_s = \sum_{N_e=0}^{\frac{L}{4}-1-T} \binom{L}{N_e} p_e. \quad (11)$$

N_e is the total number of errors in a sequence. p_e is

$$p_e = p_b^{N_e} (1 - p_b)^{L - N_e}. \quad (12)$$

$\binom{L}{N_e}$ represents different ways to distribute N_e errors among L bits of a sequence. p_e is the probability that one of the $\binom{L}{N_e}$ sequences can occur. p_s is summed from N_e=0 to $N_e = \epsilon_{max}$, because OVSF sequences can correct up to ϵ_{max} errors.



(a) (b)

Fig. 2. (a) Probability of generating simultaneous false alarms. ϵ_{max} is $\frac{L}{4}-T$. (b) Probability of generating stand-alone false alarm as ϵ_{max} is increased. L and T are 8 and 0, respectively in (a) and (b).

C. False Alarms

1) Definitions: s_i, s_j and s_k are the addresses of node i, j, and k, respectively, in Fig. 1(b). s_i^* is s_i with N_e errors. N_{en} is the number of errors that s_i^* has in N_p (shaded elements in (10)) between s_i and s_j. N_{ed} is the number of errors that s_i^* has in D_p between s_i and s_j. $N_{e,ij}$ is the number of mismatched bits between s_i^* and s_j.

2) Observations: Firstly, $N_e = N_{en} + N_{ed}$. Secondly, by closely examining s_i, s_j, and s_i^*, it can be shown that

$$N_{e,ij} = N_{en} + \frac{L}{2} - N_{ed}. \tag{13}$$

Thirdly, a false alarm occurs when

$$N_{e,ij} \leq \frac{L}{4} - 1 - T. \tag{14}$$

Fourthly, s_i and s_j are different in D_p. $N_{e,ij}$ is minimized when the number of errors in D_p is maximized. Fifthly, assuming that N_e is fixed, moving an error from a D_p to an N_p increases $N_{e,ij}$ by two.

3) Simultaneous False Alarms: Increasing ϵ_{max} above $L/4-1-T$ produces simultaneous false alarms. This phenomenon can be demonstrated step-by-step as follows: **1**) Choose s_i and s_j from N_S sleep nodes. **2**) Set ϵ_{max} to $N_{en} - N_{ed} + \frac{L}{2}$. **3**) Determine N_{en} and N_{ed} using N_e. **4**) Identify $\binom{\frac{L}{2}}{N_{en}}\binom{\frac{L}{2}}{N_{ed}}$ instances of s_i^* that generate false alarms. **5**) Choose a different s_j from the remaining sleep nodes and repeat step 1 through step 4. **6**) Count the number of false alarms generated by each instance of s_i^*. **7**) Compute the probability of creating s_i^* for a given p_b.

No simultaneous false alarm is observed when ϵ_{max} is set to $L/4-1-T$. Figure 2(a) shows that multiple nodes can be falsely awakened simultaneously when setting ϵ_{max} to $L/4-T$. The probability of multiple nodes being falsely awakened increases as p_b is increased. Figure 2(b) shows that reducing ϵ_{max} from $\frac{L}{4}-T$ to $\frac{L}{4}-1-T$ leads to a lower probability of generating stand-alone false alarms, because sequences of s_i^* satisfying $N_{e,ij} = L/4$ can also generate stand-alone false alarms. The probability of generating a stand-alone false alarm increases as p_b is increased.

D. False Alarm Probability

$p_{i\to j}$ is the probability that node j will be awakened by a wake-up message intended for node i sent from node k.

$$p_{i\to j} = p_{ij,1} + p_{ij,2} + p_{ij,3}. \tag{15}$$

$p_{ij,1}$, $p_{ij,2}$, and $p_{ij,3}$ are derived below.

1) $\frac{L}{4}+1+T \leq N_e \leq \frac{L}{2}-1$: N_e is less than $L/2$. N_e errors can fit in some if not all $L/2$ D_p. $p_{ij,1}$ is

$$p_{ij,1} = \sum_{N_e=\frac{L}{4}+1+T}^{\frac{L}{2}-1} \sum_{N_{en}=0}^{\lfloor \frac{N_e-(\frac{L}{4}+1+T)}{2} \rfloor} \binom{L/2}{N_{en}}\binom{L/2}{N_e-N_{en}} p_e. \tag{16}$$

$\binom{L/2}{N_{en}}\binom{L/2}{N_e-N_{en}}$ describes the number of ways of introducing errors in N_p and D_p. The floor operator ($\lfloor\,\rfloor$) is used if $\frac{N_e-(L/4+1)}{2}$ is not an integer. The constraint on T is determined by forcing the maximum index of N_e to be equal to or greater than the minimum index of N_e, that is,

$$T \leq \frac{L}{4} - 2. \tag{17}$$

Therefore, T is less than or equal to 2 for $L = 16$.

2) $N_e = \frac{L}{2}$: With $N_e = \frac{L}{2}$, $p_{ij,2}$ is

$$p_{ij,2} = \sum_{N_{en}=0}^{\lfloor \frac{\frac{L}{4}-1-T}{2} \rfloor} \binom{L/2}{N_{en}}\binom{L/2}{N_{en}} p_e. \tag{18}$$

As $N_e = \frac{L}{2}$, $\binom{L/2}{N_e-N_{en}} = \binom{L/2}{N_{en}}$. $\binom{L/2}{N_{en}}\binom{L/2}{N_{en}}$ describes the number of ways of introducing errors in N_p and D_p. The maximum index of N_{en} is obtained by replacing the maximum index of N_{en} in (16) with $N_e = \frac{L}{2}$.

3) $L/2+1 \leq N_e \leq 3/4L-1-T$: Sequences with $\frac{L}{2} < N_e \leq \frac{3}{4}L-1$ do not have sufficient D_p to accommodate N_e errors. $p_{ij,3}$ is

$$p_{ij,3} = \sum_{N_e=\frac{L}{2}+1}^{\frac{3L}{4}-1-T} \sum_{N_{en}=N_e-\frac{L}{2}}^{\lfloor \frac{N_e-(\frac{L}{4}+1+T)}{2} \rfloor} \binom{L/2}{N_{en}}\binom{L/2}{N_e-N_{en}} p_e. \tag{19}$$

The minimum index of N_{en} is obtained by allowing errors to fill all of D_p. As $N_e > L/2$, the remaining error (i.e., $N_e - L/2$) must occupy N_p. The minimum index of N_{en} is therefore $N_e - L/2$. Equation (13) shows that $N_{e,ij} = N_{en}$ if all of the D_p are filled with errors to minimize $N_{e,ij}$. The maximum index of N_e is obtained by setting $N_{e,ij}$ equal to $N_e - L/2$ and applying the constraint in (14).

E. Comparison of p_{ij}

$\Delta p_{i\to j}$, defined as $p_{i\to j}$ (calculated using (15)) *subtracted from* $p_{i\to j}$ (calculated using [13]), is

$$\Delta p_{i\to j} = \sum_{m=0}^{4} \binom{8}{m}\binom{8}{m+4} p_e(N_e = 2m+4) \tag{20}$$

for $L = 16$. Figure 3 shows $\Delta p_{i\to j}/p_{i\to j}$ as a function of p_b and reveals that the $p_{i\to j}$ derived in [13] is higher than that calculated using (15), due to the assumption that ϵ_{max} is $\frac{L}{4}$.

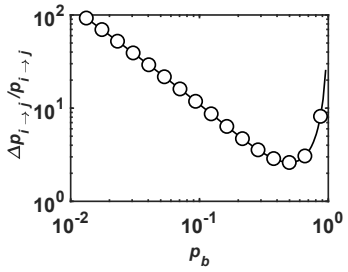


Fig. 3. $\Delta p_{i\to j}/p_{i\to j}$ as a function of p_b.

F. Sequences That Do Not Turn On Wake-up Receivers

Some sequences of s_i^* contribute to neither p_s nor $p_{i\to j}$. They have N_e within the following ranges.

1) $\frac{L}{4} - T \le N_e \le \frac{L}{4} + T$: N_e is less than the number of D_p. Therefore, all of the N_e occupy D_p.

2) $\frac{3}{4}L - T \le N_e \le L$: N_e is greater than the number of D_p. Therefore, some of the N_e occupy N_p.

In both cases, neither a detection nor a false alarm is generated because $N_{e,ij}$ and N_e are greater than ϵ_{max}.

IV. Results

A. Simulation Results

p_s and p_{fa} are determined using Xcelium simulation and Python post-processing. First, a target node (s_i) and a source node (s_k) are chosen. Then each sequence arriving at N_S decoders is classified as a detection, a false alarm, or an invalid sequence. With L equal to 16, there are 65,536 possible sequences. The Xcelium execution time is approximately 10 seconds. Finally, a python script post-processes the Xcelium log file and calculates p_s and p_{fa}.

Figure 4(a) shows close agreement between p_s calculated using (11) and the simulated p_s. Figure 4(b) shows the agreement between p_{fa} calculated using (8) and (15) and the simulated p_{fa}. The close agreement between simulation and calculation in Fig. 4(a) and Fig. 4(b) suggest that p_s and p_{fa} are accurately modeled by (11) and (8).

Figure 4(c) compares the normalized power consumption of a sleep node due to false alarms ($P_{t,fa}/(\lambda E_{fa})$) calculated using $\epsilon_{max}=\frac{L}{4}-1-T$ with that obtained from [13] and shows that the maximum $P_{t,fa}/(\lambda E_{fa})$ is reduced by 16.9 dB.

Figure 4(d) shows that T can be increased to improve p_{fa}. For a given p_b, p_s is reduced as T is increased. Figure 4(e) shows a slight increase in the normalized energy consumed by a source node in sending a wake-up packet as T is increased and p_s is reduced. For a given p_b, p_{fa} is reduced as T is increased. Figure 4(f) shows that the maximum $P_{t,fa}/(\lambda E_{fa})$ can be decreased by 16.08 dB by increasing T to reduce p_{fa}.

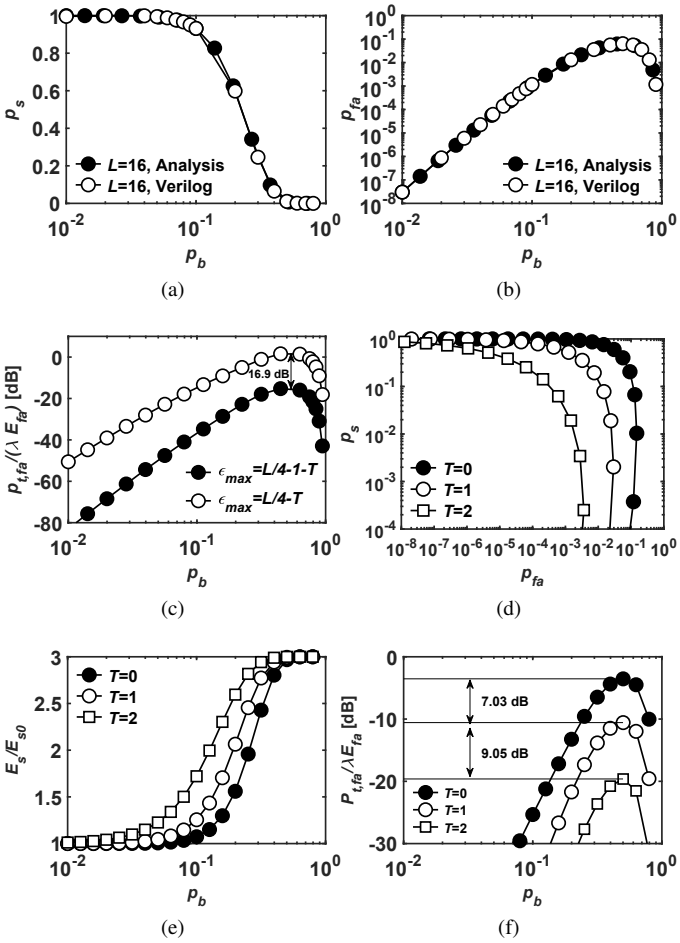


Fig. 4. L and T are 16 and 0, respectively. (a) Comparison of calculated and simulated p_s. (b) Comparison of calculated and simulated p_{fa}. N_S is 7. (c) The normalized power consumption of a sleep node due to false alarms as a function of p_b. N_S is 2. (d) p_s versus p_{fa}. (e) The normalized energy consumed by a source node to send a packet versus p_b. $m = 3$. (f) The normalized power consumption of a sleep node due to false alarms versus p_b. N_S is 15 for (d), (e), and (f).

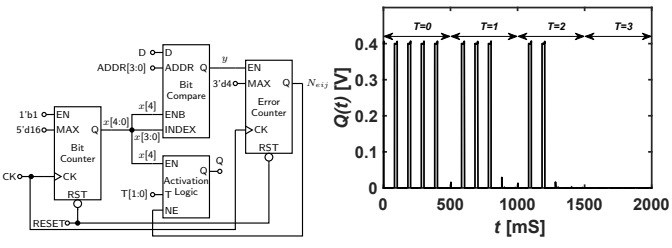


Fig. 5. (a) Counter-based implementation of an OVSF address decoder. (b) Post-layout simulation.

B. Implementation Issues

The address decoder is illustrated in Fig. 5(a). During the *error counting* phase, the Bit Compare is enabled while the Activation Logic is disabled. D is compared one bit at a time to ADDR[INDEX]. y is set to 1 and N_{eij} is incremented for a mismatch. y is set to 0 and N_{eij} is unchanged for a match. During the *evaluation* phase, the Bit Compare is disabled, the Error Counter is disabled, N_{eij} is not changed, and the Activation Logic is enabled. Q is set to 1 if $N_{eij} \le \frac{L}{4} - 1 - T$ and $T \le \frac{L}{4} - 2$. Otherwise, Q is set to 0.

[16] defines an equivalent logic gate as having four transistors. It is desirable to minimize uses of D flip-flops (DFFs), since each DFF uses as many as seven logic gates [16]. The counter-based implementation in Fig. 5(a) reduces the

equivalent gate count, area, and power consumption (P_D) by **1**) not shifting bits through DFFs as was done in [8] and [12] and **2**) not requiring oversampling (e.g. [8]) or logic gates for implementing asymmetry in error correction (e.g. [12]).

The OVSF address decoder is synthesized from its Verilog description as follows. **1**) A synthesized netlist is created using Genus with standard cells from a 0.18 μm TSMC design kit. **2**) The synthesized netlist is placed and routed using Innovus. **3**) The layout is exported to a GDS file and imported into Virtuoso. **4**) The parasitics are extracted with Quantus after checking the layout for DRC and LVS errors using Assura.

With a V_{DD} of 0.4 V, the subthreshold address decoder is simulated with the layout parasitics at 200 bps. Figure 5(b) shows the output $Q(t)$ of the decoder as the number of errors in sequences is increased incrementally from 0 to 4. Fig. 5(b) shows that **1**) as T is changed from 0 to 3, the number of interrupts is reduced. **2**) the address decoder can correct up to $L/4-1-T$ errors.

Table I shows the comparison with the state-of-the-art designs. The latency of the counter-based design is 80 ms for a data rate of 200 bps. The P_D is 0.26 nW, compared to 0.77 nW and 0.8 nW reported in [8] and [12]. The energy per bit for each address decoder is calculated at 200 bps. Table I shows that the energy-per-bit calculation for the counter-based design is 1.3 pJ/bit compared to 3.85 pJ/bit and 4.00 pJ/bit reported in [8] and [12].

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART DIGITAL CORRELATORS.

Ref	This Work	[8]	[12]
Architecture	Synchronized OVSF	Oversampling	Bit-level duty cycling
Tech.	CMOS	CMOS SOI	CMOS
Process (nm)	180	180	130
Implementation	Post-layout	Measured	Measured
V_{DD} (V)	0.4	0.4	0.6
P_D (nW)	0.26	0.77	0.8
L (bits)	16	16	16.5
Data rate (bps)	200	300	200
Gate count	126.5	543[1]	167[1]
Area (μm^2)	1,341	4,996[1]	1,748[1]
Latency (ms)	80	80	82.5
Energy/bit (pJ)	1.30	3.85[2]	4.00

[1] Determined from post-synthesis reports.
[2] Calculated at 200 bps using P_D reported in [8] since P_D is dominated by leakage power.

V. CONCLUSION

This brief establishes a framework for analyzing the detection and false alarm probabilities of OVSF address decoders. It also demonstrates that limiting the number of correctable errors reduces the false alarm probability, eliminates the simultaneous false alarms, and improves the maximum normalized power consumption of a sleep node due to false alarms by 16.9 dB. The mathematical expressions are presented so that the detection probability, the false alarm probability, and the normalized power consumption of a sleep node due to false alarms can be adjusted digitally, yielding a reconfigurable counter-based implementation that reduces the energy-per-bit of the address decoder by a factor of 2.96.

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