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Analog and Mixed-Signal Circuits simulation for product level EMMI analysis

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Abstract –. The goal of this work is to propose a new flow that integrates the analog and mixed signal simulation of the circuits to replicate the EMMI signals. This supports the fault localization process. We explore the emission typologies of the transistors, focusing the attention on the DMOS structure. First experimental results show the benefits of this approach.

1. Introduction

The fault isolation process is fundamental in every failure analysis, to address the physical analysis (PA). This step is becoming increasingly difficult to carry out. The cause is the increasing complexity of devices and applications, which implies a longer time for the fault isolation step. In a standard failure analysis (FA), the global fault isolation step is mainly performed using emission microscopy (EMMI). In general, this procedure takes a long time. In fact, the image comparison between golden and faulty sample is always necessary and time consuming. Furthermore, in safety applications, some activation of defects are not permitted by the device. It must prevent a critical state to be activated when a fail occurs. Consequently, the light emitted will only be the result of the consequences of the defect which cannot produce light. For this reason, the simulation of the circuit can make this step easier. Some solutions have been proposed, focusing mainly on the PICA emission tool [1], [2]. This tool provides the light emission spot with the timing associated. It is very powerful from the perspective of analysis, especially for digital electronics. Nevertheless, the integration of simulation in this application risks complicating the analysis considerably. In fact, for a modern mixed signal product, the emission activity is high. Inside a real FA case, the study of the timing for each spot would make the analysis longer than recommended. Moreover, each study reported above focused mainly on MOSFET structures. Omitting other types of devices does not allow complete knowledge of the circuit. Consequently, not even emission simulation will be available at product-level. Regarding the emission in static condition, an example of EMMI simulation for MOSFET was studied in [3]. In this case, the simulation used the substrate current [4] for the transistor in saturation and the density of current in diode configuration. These models have some limitations for those transistors without body pin, such as DMOS and FD-SOI. In these, in fact, the substrate current is inaccessible.

This paper overcomes these problems with a new method for product-level emission simulation. We name this solution Emitting Light Simulator (ELS), handling the EMMI of each device inside the circuit. This tool uses an emission model for MOSFETs without the need to know the substrate current. In this way, it is applicable for the first time to any MOS typology, any analog IP and products. For the other components like diodes and BJT, forward current model is used to simulate the light emitted. The second section presents the model to reproduce the light emission of the devices. The attention is focused on DMOS structure with transistor characterization. The third part is dedicated to the description of the simulation tool. Starting from the basic requirements, we will present the ELS algorithm. The fourth section deals with real-life failure analysis cases, in which the fault isolation phase is done by ELS. Finally, we will draw conclusions and hint future developments.

2. Emitting device models

This section is dedicated to the derivation of the fundamentals to rebuild the EMMI at product level. The basic models employed to derive the emission of each device are studied. In the first part, the attention is focused on the models used for the MOSFETs, bipolar transistors and diodes. The second describes the characterization and tuning process needed to achieve a correct simulation.

2.1. Light emission models

For MOSFET devices a light emission occurs when they operates in the saturation region [4]. In these conditions the light emitted is proportional to the substrate current (body pin current). Accordingly, the emission for CMOS transistors has been derived using this current, with satisfactory results [5]. Nevertheless, this is no longer possible for devices which substrate is not accessible. It is the case for DMOS in analog electronics and FD-SOI and FinFET in digital electronics. For this reason the model presented in [5] is considered in this work. In fact, it does not directly use the substrate current, instead it expresses the number of photons (Nph) as follows:

$$N_{ph} = \alpha\, I_d\left(V_{DS} - V_{DS_{sat}}\right) * e^{-\frac{\beta}{V_{DS}-V_{DS_{sat}}}} \qquad (1)$$

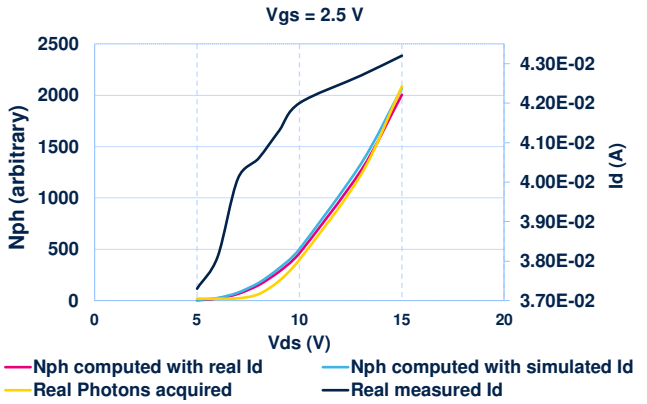

Fig. 1 Comparison of simulation data and real acquisition for the saturated MOSFET model.

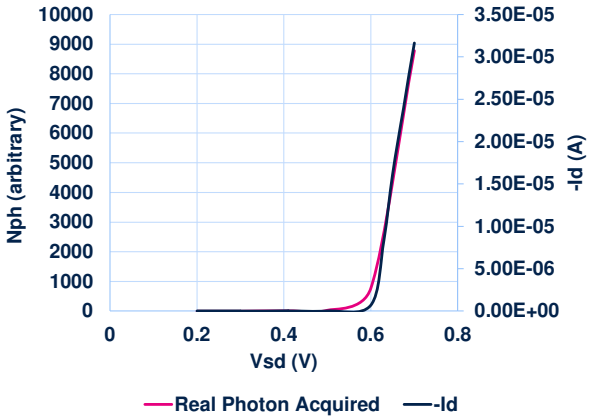

Fig. 2 Comparison of source current and number of photons acquired for a DMOS in diode configuration.

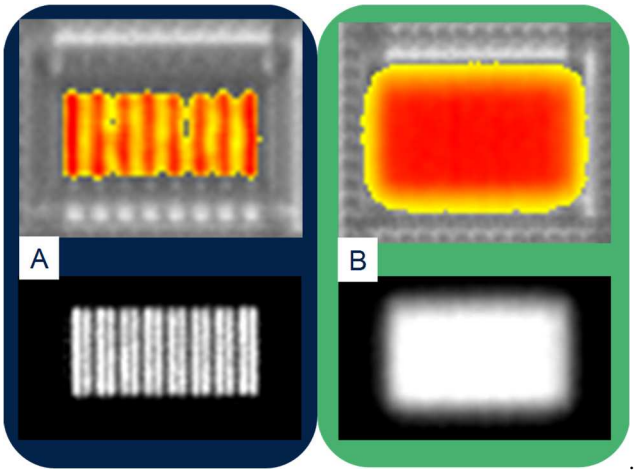

Fig. 3 On top: the emission images overlaid on the optical ones; on the bottom: the raw emission images for respectively: a) saturation mode and b) diode configuration.

where I_d is the drain current, V_{DS} and V_{DSsat} are respectively: the drain-source voltage and drain-source saturation voltage. The factor α is a scale factor, while β is dependent on the fabrication technology and the parameters of the device. The first part of equation (1) indicates a linear dependency of the emission on the current flowing on the channel. The rest is the probability of emission of each carrier. The gate-source voltage (V_{GS}) is used to determine the current I_d and the V_{DSsat}. The expression used for V_{DSsat} is reported in [6]. In the latter, the channel length of the transistor is also considered. All the parameters can be retrieved from the simulation results and netlist information, through the technology models. Concerning the scale factors, α is linear and is easily treated, while β requires particular attention, being the argument of the exponential. An eventual wrong approximation of that may cause an exponential error propagation. For this reason, we planned a characterization to extrapolate the β factor. It is described in the second part of this section, paying particular attention to the DMOS component. From our experience, we also noticed that this type of structure can emit in a particular voltage configuration, called diode configuration [7], [8]. In this case, the emission model finds a direct proportionality between the light emitted and the density of current flowing in the channel. An example is reported in the second part of this section.

The other emitting devices inside an integrated circuit are diodes and BJTs. The diodes emit when they are both in forward and reverse bias polarisation. In reverse bias, the emission is present when they are in the avalanche region. It is a common case for the Zener diodes, which work mainly in that state. For the forward bias, the emission occurs when the applied voltage is greater than the knee voltage. In both cases, the emission is derived from the current flowing in the junction. A similar reasoning can be made for BJTs, which are composed of two junctions. In this case, the emission is qualified by the collector current [9].

2.2. *Devices characterization*

For the extrapolation of the β parameter (see Eq. 1), we used the Meridian IV equipment, with an InGaAs camera to perform the acquisition in near-IR range. The measurements have been done in a steady state for the emission, using equal timing exposures of 1 second. We chose this interval so that it would faithfully approximate the measurements we make during a real FA. The equipment offers the possibility to quantify the emission reporting an average of the collected photons, during the acquisition interval. Therefore, the measurement of the number of photons will be on an arbitrary scale. Although this is not the exact number of photons, it is still a relevant indication for our work. The objective is to simulate the image coming from this instrument.

A wafer with single devices in BCD technology has been used for the measurements. This is the technology that we have more frequently for our FA cases. In this wafer all the structures have been studied, paying special attentions to DMOS. In this work are reported only some measurements executed in one of the many DMOS typologies present in the wafer. The considered transistor works at 30 V in nominal conditions, with a length of 500 nm.

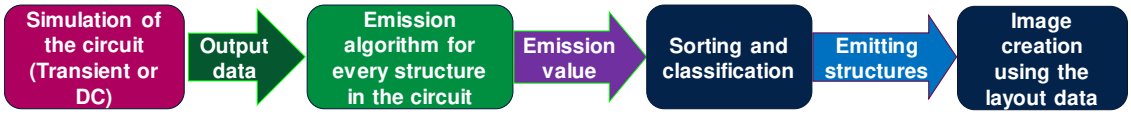

Fig. 4 Proposed flow for the simulation for product level EMMI

We first characterized the electrical parameters, by acquiring the drain current in saturation region (Fig. 1), keeping constant V_{GS} and choosing many V_{DS} steps. We then acquired the number of photons using the same conditions. The acquisition time was 1 second, repeated five times for each value of V_{DS}. The average of the five measurements was computed, giving the number of photons for each voltage (Fig. 1). β has been derived from the measured current, using Eq. 1 with a fixed value of α. This value was 21.3 for the considered structure and for the others DMOS it ranged from 20.0 to 25.0. The computed β was then inserted in Eq.1 to calculate the number of photons, using the results of spice simulations. Fig. 1 shows the results of the Nph computation using Eq.1. In particular it is a comparison between the real Nph, the results of the computation of that parameter using the real Id (measured on the device) and Id resulting from the simulation.

The same structure has been characterized also in the diode configuration, described in the previous section. In this case, it was applied $V_{GS} = 0$ V and V_{DS} negative, sweeping from 0V to -1 V. The results are presented in Fig. 2. The emission is significantly stronger for lower current values than when the device is operating in saturation mode. Moreover, the type of emission in diode configuration is visually recognizable (Fig. 3) if compared with the saturation one. In fact, in saturation the light emitted is localized in the drain area, while if the transistor is in diode configuration it appears diffused on its whole surface.

3. Product level simulation

3.1. Basic Requirements

Some data are required before starting the emission simulation. The design environment to build the whole circuit simulation or the IP level simulation are essentials. The former is less used due to its longer simulation time and complexity. It can be however employed to reproduce the golden devices, with a standard setup. The latter makes use of spice simulations, with a virtual test bench provided by design team with standard database. It reproduces exactly the electrical bench measurements of a golden device. This simulation type is faster, allowing a wider application domain (defect hypothesis validation and golden unit). Standard fault isolation techniques are used to identify the single IP to be simulated. Generally, it can be determined after the automatic test equipment (ATE) results. Scripts has been done to allow FA engineer to easily modify parameters of the simulation and fit the bench application trial. Concerning the digital circuits, this process is facilitated by the availability of the Fastkit tool [10], [11]. It is an automated software environment to manage the product database setup. It allows to generate the test sequences for the analysis and spice simulation of the cells.

The layout, netlist and schematics of the entire circuit are desirable. In this work we use Avalon by Synopsys, a software that offers a fully aligned environment for displaying the circuit. This is suitable but not necessary, because we use it for the image creation. We can still have the full accessibility of the ELS results, without this software, but lacking the image generation.

3.2. Emitting Light Simulator tool

The ELS software is written with Tool Command Language (TCL) and it is composed by two main scripts. The inputs are the nominal simulation netlist and the parameters file listing the coefficient extrapolated through the procedure described in section 2.2.

The first script is the main part of the program. It manages the input netlist to automatically add all the probes needed to apply the emission models. This step takes advantage of the regular expressions available on each simulator. In this sense, the netlist is managed differently, depending on the simulator for which it is designed (Eldo, Customsim or Spectre). It ensures the minimum number of probes to obtain the smallest possible results database. The simulation is then run and the output database converted into a text file. This is the input of the second script that is executed at this point.

The second script applies the emission models of each instance, reading the text results and the input netlist for the geometrical parameters (length and width).

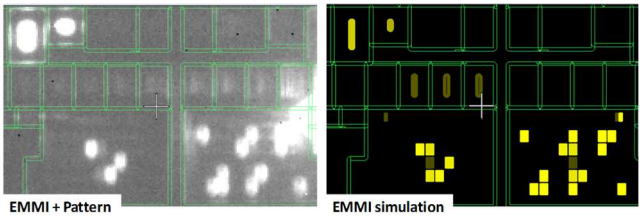

Fig. 5 On the left: a real EMMI on a golden unit; on the right: the EMMI simulation, the EMMI spots are in different yellow intensities.

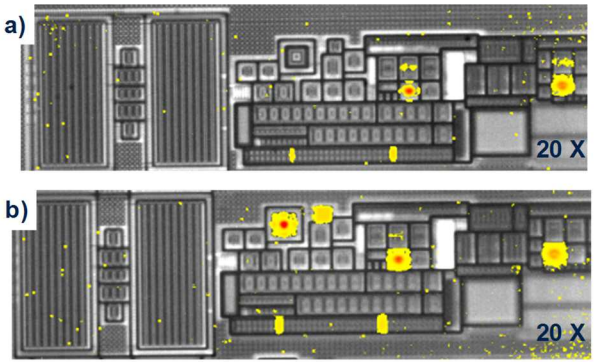

Fig. 7 EMMI image acquired during OFF state for: a) the golden sample; b) the failing unit.

The script has two different working modes in case the simulation is analog or digital. For the analog one, it considers the values of the instances at steady state. Regarding the transistors, it checks if they are in saturation, it applies the model of Eq.1 and assigns to the transistors an emission value (Nph). If they are in diode configuration, it computes the current density reporting the result inside the same parameter for Eq.1 (Nph). For diodes and BJTs collector, the value of the current is measured using current probes added in the test bench through the first script. Concerning the digital simulations, the procedure is the same but performed for each timing step. These values are stored into vectors, quantifying the emission for each instance in all the simulation timing period. Finally, the vectors elements are integrated to assign a unique emission value to each instance.

From here on, the script acts equally in both types of simulation. It reconstructs the top hierarchy for each instance. Subsequently, to each element is assigned a colour (red for transistor in diode configuration, yellow for all the others) and a transparency level. The transparency level will indicate the emission level of the instance in the image. The transparency is a value that varies from 0 (fully visible) to 100 (fully transparent). This parameter is assigned to each emitting element according to an exponential order of the emission value. The sorting is calculated only between instances of the same type and for which the same emission model has been used (e.g. transistor in diode configuration, BJTs, diodes). In the end an Avalon instance file is generated reporting all the information of each instance. The ELS image is then generated. The file is loaded in the layout, creating a visualization of the emission aligned with schematic and netlist. This software (Fig.4) can be used to reproduce a golden sample or to analyse the consequence of a fault injected in the simulation. An interesting feature is the possibility to perform the ELS in an inner block of the single IP test bench. The aim is to reproduce the use of higher magnification of the lens in EMMI. This gives a narrower view of a part of the IP, varying the intensity of the light spots (due to less interference between spots from distant areas).

A medium analog IP size, of about 2000 devices, can be simulated in 5 minutes, transferring the results into layout immediately and automatically. An example of ELS performed comparing with a golden sample for an analog IP is showed in Fig.5. The entire process for a standard digital cell can be faster than the analog approach, despite time step integration. This is a consequence of the digital simulation and export of the Spice net list at the cell level [10]. A digital application example is reported in Fig.6, where we chose the violet colour for the EMMI reproduction.

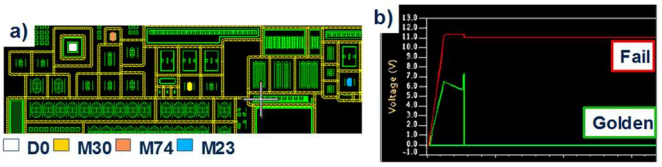

Fig. 8 a) Location in the layout of the most intense EMMI spots identified in Fig 7b. Under the figure there is the legend for the highlighted instances, to discriminate the simulated structures in Table I; b) Simulation for the fault injected in the hypothesized transistor in OFF state.

Fig. 9 a) ELS image of the golden sample; b) ELS image in consequence of the fault injection.

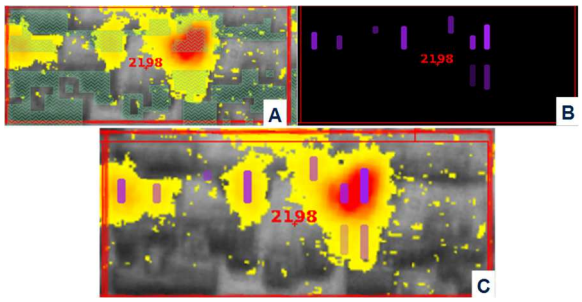

Fig. 6 a) real EMMI of a golden unit overlaid into layout on scan test of Flipflop ; b) ELS results in different violet intensities; c) both ELS and EMMI overlaid in layout.

4. Real Case Study

The FA cases that will be shown in this section deal with door zone devices. They are automotive devices with several functionalities to drive car door components. They are mixed signal products, with an analog-centric design.

4.1 FA case 1

The case presented here refers to a device with a problem in a voltage output value. In particular, the ATE measured a wrong voltage generation when the output was turned OFF. The electrical bench verification confirmed this behaviour. In the OFF state, the device reported 11V instead of 0V in a golden unit. In contrast to this, the value was equal to a golden unit when the output was driven high (12 V). To make the back-side analysis possible, the package was partially removed to access the silicon die.

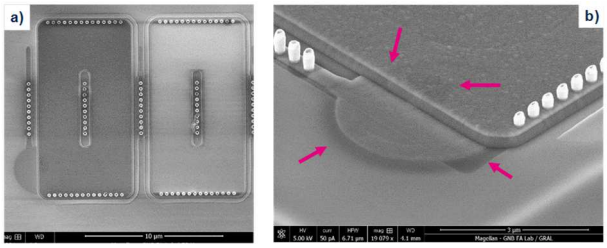

Fig. 10 Two SEM views of the physical defect on the suspected MOSFET: a) Passive voltage contrast; b) tilted view, with red arrows indicating the extra pattern at silicon active layer.

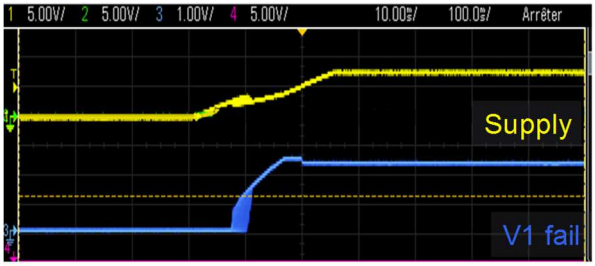

Fig. 11 . Electrical measurements of the failing device acquired in the bench. In blue the signal failing signal V1 at 2.8 V.

A laser stimulation inspection was performed, using the OBIRCH technique and monitoring the failing output. With this technique, it has not been possible to observe any single spot given a location of the defect. For this reason, we started the EMMI inspection, comparing the DUT with a golden unit for both output states. As expected, we did not notice any difference in the images acquired in the ON state. This meant that in that state even the internal behavior of the circuit was correct. From the comparison in the OFF state (Fig. 7), some consequences of the fail were observed. However, they were not sufficient to conclude on the defect localization. We identified the EMMI spot of the faulty device (Fig. 7b) within the circuit layout view (see Fig. 8a). Subsequently, using the schematic, we studied the connections of the various spots through their nets. Some commonalities were observed in a transistor that was not emitting. For this reason, we considered this structure as a hypothesis for the defect. A virtual test bench was then prepared, reproducing the real measurements environment. Afterwards, the ELS was performed in nominal conditions, reproducing the golden device image (Fig 9a). This ensured the correct preparation of the simulation. Finally, we injected a failure into the spice simulation in the hypothesized transistor. We performed many simulations sweeping the resistance values from 10 Ohms to 10 kOhms. The resistance value of 100 Ohms matched perfectly the failing signature (measure of the 11V at the output during the OFF state, see Fig 8b). Therefore, the simulation validated the hypothesis, by explaining the differences observed in the device (see Table I and Fig 9b). The physical analysis started focusing on that area. After the step by step de-layering, we revealed the defect at poly-silicon level (Fig. 10) in the area located by the fault isolation step. The defect was the presence of an extra pattern of silicon at active layer (Fig. 10b) causing a short circuit between the gate and the drain of the MOSFET, like our simulation.

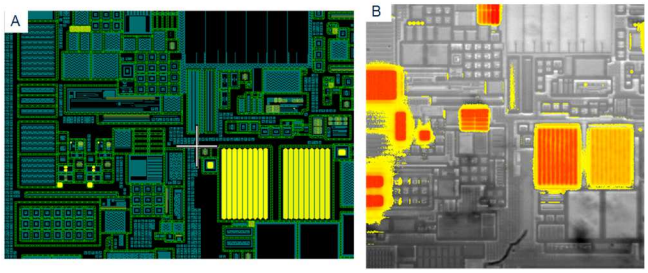

Fig. 12 a) ELS image of the golden device for the reference voltage generator IP; b) emission image from the failing sample acquired in the same area.

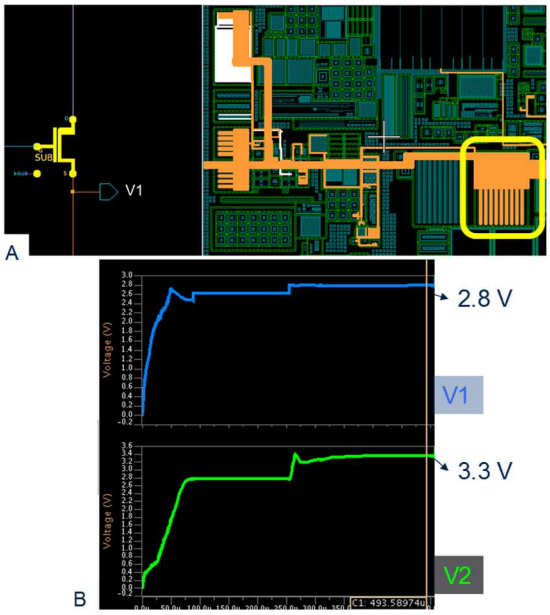

Fig. 13 a) Spots analysis. In orange and white the nets linking the spots of the EMMI. The yellow square indicates the failing transistor; b) Simulation results in consequence of the fault injection.

4.2 FA case 2

The second application case is a field return not starting. The device generates two reference voltages. One is for the digital circuit (here named V1), the other for analog circuit (V2). When one of the two references is not correct, the device enters into a safe state to avoid safety risks.

The ATE measurements found this problem at only one voltage (V1). This was confirmed by the measurements made in the electrical bench. The voltage V1 was measured at 2.8V instead of 3.3V while V2 was correctly measured at 3.3 V (see Fig. 11). Since the device did not start and the internal measurements were not accessible, the probability of success of the FA was low. Looking at the failure mode, we understood that the problem came from the voltage reference circuitry. This allowed us to start the nominal simulation before the sample preparation.

	Operative		Is (A)		Nph	
	Golden	DUT	Golden	DUT	Golden	DUT
3	SAT	SAT	2.18E-06	2.17E-06	1.52E+04	1.52E+04
0	SAT	SAT	2.03E-06	2.03E-06	1.62E+04	1.62E+04
0	OFF	DIODE	-1.07E-08	-3.01E-05	9.77E+02	2.96E+06
	OFF	AVAL	5E-10	-6.48E-06	-	-

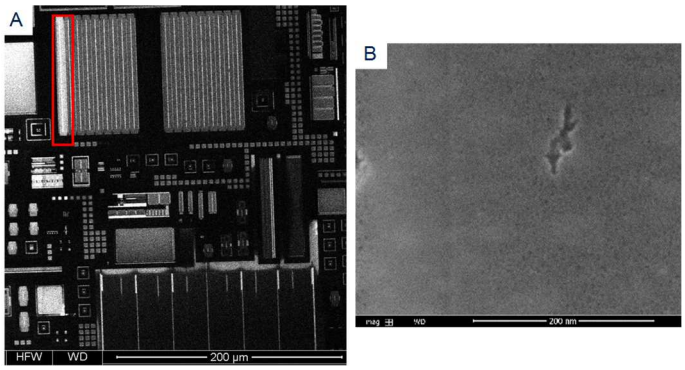

Fig. 15 a) Passive voltage contrast image at poly silicon layer. The red square indicates the abnormal contrast in the finger of the transistor; b) Greater magnification of the red squared area at active layer.

The circuit was prepared for backside analysis. The ELS image was then created and the emission analysis started on the failing sample. By comparing ELS image with the failing unit in the area of interest, a lot of differences were found (see Fig. 12). These were only consequences of the failing state, since the device switched to a safe one. For this reason, we performed an analysis of the nets that connected the spots in the failing device (see Fig. 13a). We found a common point in the output transistor of V1 voltage generator block (yellow square in Fig. 13a). This transistor was not emitting as expected in case of defect (light localized at the drain side). Therefore, only a leakage in one of its fingers could explain the defect in this structure.

We performed a fault injection between the gate and the source of this transistor. The failing behaviour in V1 was reproduced by a resistance of 2 kOhms. The results in fact had a perfect correlation with the failure mode (V1 2.8V and V2 at the correct voltage) (see Fig. 13b). With the same simulation, we ran the ELS, which returned an image (see Fig. 14) that was matching the failing one (Fig. 12b). This allowed to confirm the hypothesis for the defect, giving the right location. The PA started focusing on this area. The layer by layer inspection has been done. Using the passive voltage contrast technique with the SEM, an abnormal contrast was observed at poly silicon level (see Fig. 15a). This was in the same transistor found during the fault isolation (Fig. 13a). At the same location at the active layer, multiple defects were observed (Fig. 15b). They were traces of a typical gate oxide breakdown, involving only one of the multiple fingers in the transistor. This defect was produced by a leakage and explained why the transistor emitted light in the correct way even if it was damaged. Using the ELS, we found the physical defect at the correct location.

5. Conclusions

This paper shows how the integration of the simulation of analog and mixed signal devices can support the fault isolation step. The basic elements to build an emission simulation are shown, starting from the models and tools. The simulation tool is validated in two application cases of failure analysis. In both, the benefits of this approach emerged. These cases were difficult to be solved without simulation, not ensuring any success and causing a long cycle time with a low success rate. The ELS solves these problems. In the cases presented, fault isolation is faster and more accurate, finding defects with success. Moreover, this method improves the awareness of the operator in the circuit functionalities. In fact, it permits to make and confirm hypotheses, successfully completing the fault isolation.

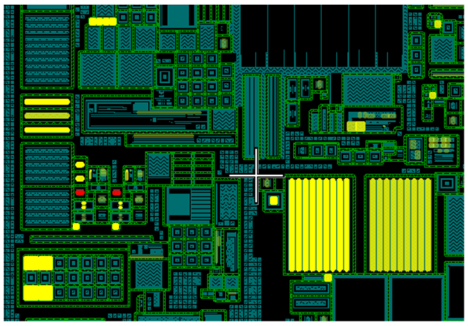
Fig. 14 ELS image in consequence of the fault injection inside the transistor identified in Fig.13a.

This approach is not limited only to analog but can be applied also to digital circuits. With the introduction of an algorithm for the integration of the results, the ELS tool has correctly produced the EMMI of digital circuits. Moreover, the model used for the transistor in saturation has been evaluated also in FinFET technology [12]. Future work will address this topic, with the application of ELS in more technology nodes.

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