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Dataflow Algorithm Architecture co-design of SKA pipeline for Exascale Radio Astronomy

Daniel Charlet**⁵ (IJCLab), Karol Desnos¹, Mickael Dardaillon³, André Ferrari⁴, Chiara Ferrari⁴, Nicolas Gac³, Jean-François Nezan¹, François Orioux³, Simon Prunet⁴, Martin Quinson², Frédéric Suter**² (IN2P3 Computing Center), Cyril Tasse**⁵ (GEPI), Cédric Viou⁵

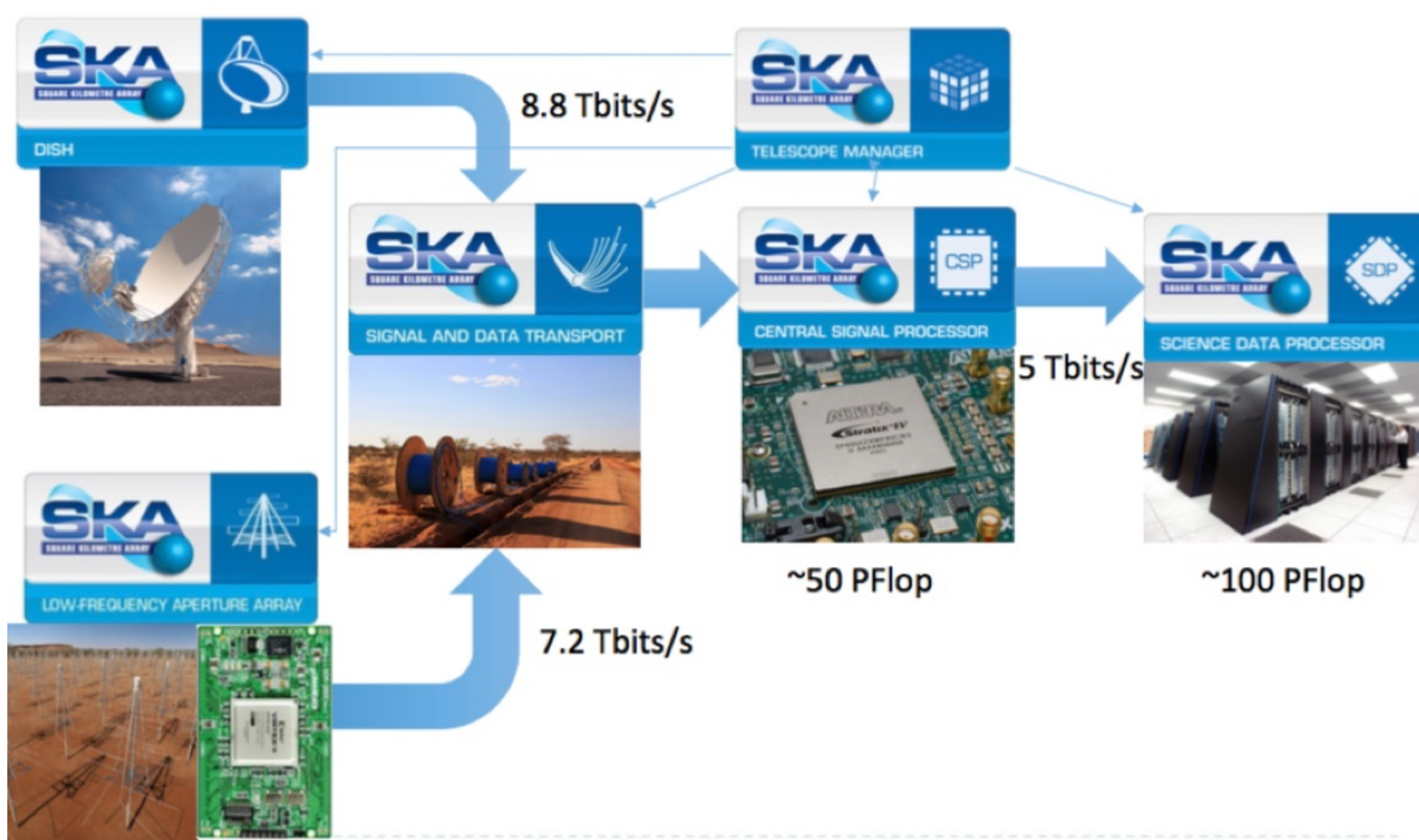
¹IETR (INSA), ²IRISA (ENS), ³L2S (CS), ⁴Lagrange (UCA), ⁵Nançay (Obs Paris)
 contact: nicolas.gac@l2s.centralesupelec.fr

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SKA computing, an HPC challenge

The **exascale radio telescope** Square Kilometre Array (SKA) [?] will require supercomputers with high technical demands. The Science Data Processor (SDP) pipeline in charge of producing the multidimensional images of the sky will have to execute in **realtime a complex algorithm chain** with data coming from telescopes at an incredible **rate of several Tb/s** and **limited storage possibilities**. The SDP will also have to be **as green as possible** with an energy budget of only 1 MWatt for 250 Petaflops.



The **SDP supercomputer** will be based on a standard HPC system combined with FPGA or application-specific architectures like GPU or the manycore Kalray Massively Parallel Processor Array (MPPA). One crucial challenge is to assess the performance both in time and energy of new complex scientific **dataflow algorithms** on not-yet-existing complex computing infrastructures. It will be hardly possible without efficient **co-design methods** and **rapid prototyping tools**.

Dark-Era, a 4-year project starting in 2021

The **consortium** gathers complementary skills in computer science, signal processing, and astronomy with twelve permanent members from the **SimGrid** [?] development Team at IRISA, the **PREESM** [?] development team at IETR, the **inverse problem** team at L2S, and two **radio astronomy** teams at Observatories of Paris and Côte d'Azur. Dark-Era has the support of SKA-France and works in collaboration with Atos-Bull.

The **PhD and PostDoc positions** within Dark-Era will be published on <https://dark-era.pages.centralesupelec.fr> :

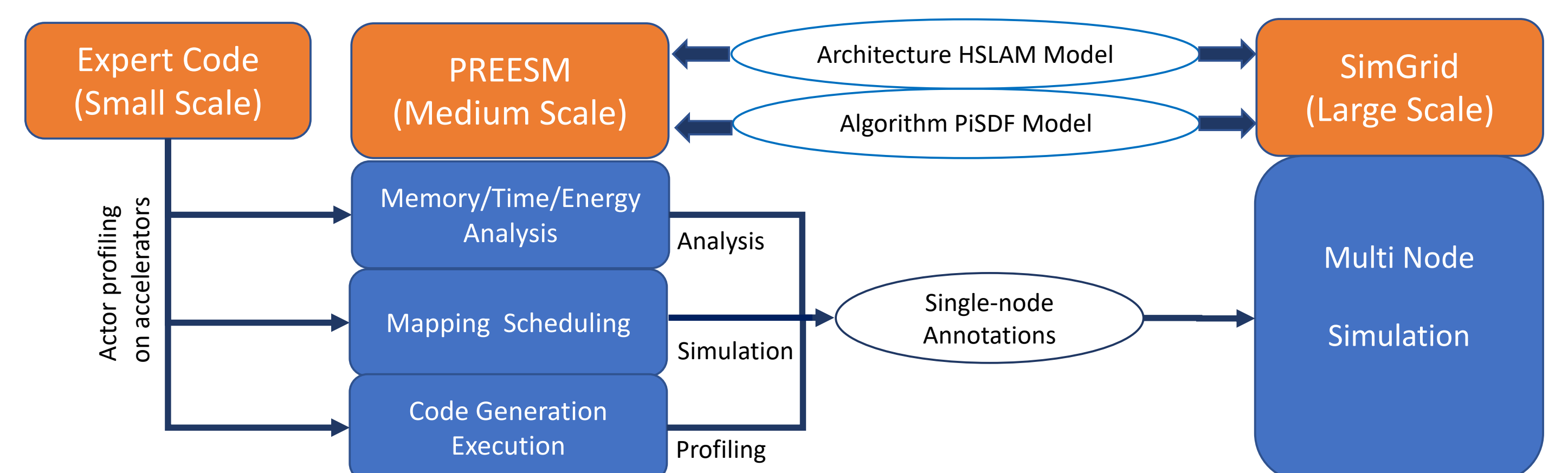
- ▶ One post-doc at LS2 on HLS FPGA prototype (autumn 2021)
- ▶ Two PhDs at IETR and IRISA respectively on PREESM and SimGrid extensions (autumn 2022)
- ▶ one post-doc at Lagrange on algorithm/architecture exploration for radioastronomy (spring 2024)

Dark-Era goals

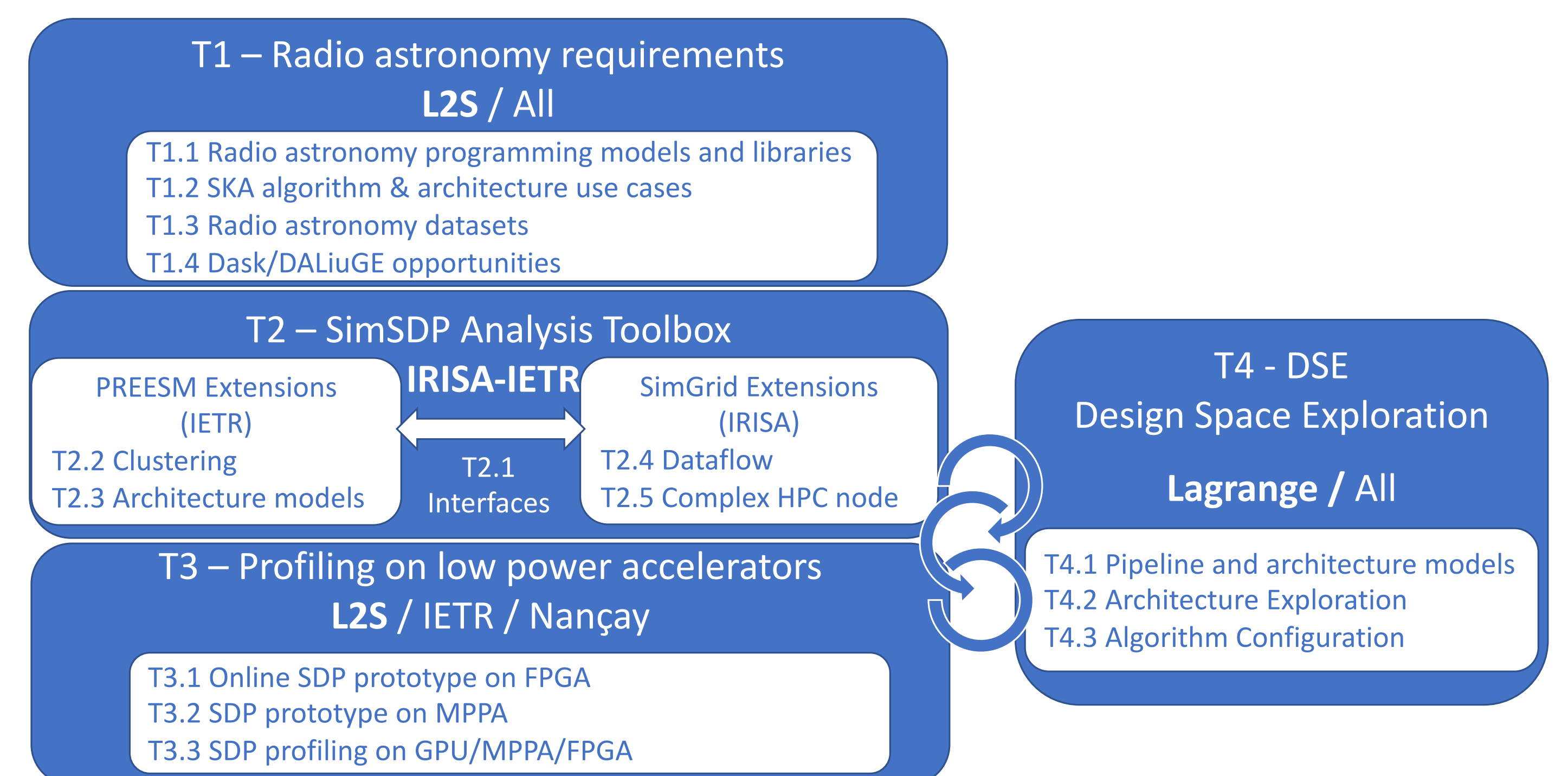
- 1 Building **SimSDP**, a rapid prototyping tool providing exascale simulations from dataflow algorithm descriptions.
- 2 Exploring **low power accelerators** like FPGA or Kalray MPPA as alternatives to mainstream GPU architecture.
- 3 Being source of proposals for SKA computing and promoting French contributions such as **ddfacet** [?].

SimSDP, an exascale simulation tool

SimSDP purpose is to provide **early analyses** in terms of memory usage, latency, throughput, and energy consumption through an original mixed approach based on execution and simulation. Following an Algorithm Architecture Matching (AAM) approach, SimSDP will rely on a dataflow model of the algorithm and a model of the target architecture. SimSDP will be based on two existing tools: PREESM and SimGrid. PREESM accurately evaluates **heterogeneous single node** performance; SimGrid accurately simulates **inter-node communications**. Their association will allow for reliable simulations of **large scale heterogeneous HPC systems**.



Dark-Era tasks



T1 will provide reference datasets and an SDP computing state of the art in terms of programming models, architectures and algorithms.

T2 is the core development task of the SimSDP rapid prototyping tool. New clustering and architecture model extensions in PREESM, and dataflow and complex HPC node extensions in SimGrid will be developed to improve the performance of both tools, enable seamless communication between them and, finally improve the quality of the large scale simulations.

In **T3**, SDP prototypes on MPPA and FPGA designed through High Level Synthesis (HLS) tools and will be developed and profiled on small scale datasets set up at the NenuFAR radio telescope. It will allow evaluating the potential of these low power accelerators. The SDP profiling feedbacks on GPU, MPPA and FPGA obtained will provide SimSDP with annotations on the dataflow graph.

In **T4**, algorithm and architecture spaces will be explored in the SKA context through the large scale simulations offered by SimSDP. The radio astronomy imaging pipelines will be described at a high-level of abstraction suitable for targeting any heterogeneous multinode HPC system SKA may choose in the future. Several SDP architecture configurations (number of nodes, type of accelerators) and several SDP algorithm configurations will be then explored.