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► **To cite this version:**

Faten Sahel, Pascal Guilbault, Farouk Vallette, Sylvain Feruglio. A Crosstalk Modelling Method between a Power Supply and a Nearby Signal in High-density Interconnection PCBs. 2021 22nd International Symposium on Quality Electronic Design (ISQED), Apr 2021, Santa Clara, CA, United States. pp.227-232, 10.1109/ISQED51717.2021.9424304 . hal-03225181

HAL Id: hal-03225181

<https://hal.science/hal-03225181v1>

Submitted on 12 May 2021

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A crosstalk modelling method between a power supply and a nearby signal in high-density interconnection PCBs

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Abstract

In this paper, we suggest a simulation method that allows the early detection of crosstalk noise, caused by power supplies on nearby sensitive signals, in high density mixed-signals boards. This paper focuses on the PCB and power supply modelling and discusses the accuracy of ground planes modelling in S-parameters modules, as current return paths in ground planes can be a major means of coupling. Our approach is based on, and validated with a comparative study between simulation results and measurements on a real case study board developed by Atos for HPC applications.

Keywords— signal and power integrity analysis, simulation flow, power supply induced crosstalk.

I. INTRODUCTION

To meet the expectations of the ever-evolving electronic technology, today's electronic systems are expected to be faster, smaller, and more efficient than ever. Consequently, Printed Circuit Boards (PCB) are increasingly multi-layered, denser, and cluttered with miniaturized components. They contain mixed-signals circuits, some of which operate at high currents, and links of various data rates. This encumbrance of the PCB results in a closeness between some disruptive elements and sensitive ones, which undergo some disturbances, such as crosstalk. The crosstalk phenomenon occurs when the signal propagating in a channel, called 'aggressor', unintentionally causes disturbances on another neighbouring channel, called 'victim'. The disturbances, commonly known as noise, can lead to errors in the transmitted data, and in the worst case, may result in a malfunctioning circuit.

Among the disruptive modules on the board, electromagnetic interferences from power supplies are the most critical; they not only hinge on the quality of the power supplies themselves, depending on their characteristics, their associated filtering and decoupling circuits, but also on their operating mode and the power they provide [1].

Power Distribution Network (PDN) provides the circuit with stable delivery and return paths of the supply voltage [2]. Robust PDNs and strict routing rules normally minimize the possible perturbations caused by the switching of power supplies on sensitive signals. But with High-Density Interconnect (HDI) technology, it becomes harder to maintain the proper spacing between sensitive signals and disruptive ones [3]. And as strict as the routing rules can be [4], it is unlikely for PCB designers to predict and prevent signal coupling every time, what with the parasitic effects induced by the switching transistors and those caused by the current return paths in ground planes [5,6].

Therefore, virtual prototyping is commonly used to verify the signals' behaviour in transmission lines, detect the parasitic effects on sensitive signals due to crosstalk, and thus allowing necessary adjustments to be made to reduce the noise, prior to first prototypes built.

There are several EDA tools that achieve virtual prototyping, using different solvers to model PCBs and the behaviour of the signals, though the accuracy of these tools depends on the modelling mode of their solvers. Finite Element Method (FEM) 3D solvers are the most appropriate for a thorough modelling, as they analyse every aspect and variation of the system to model (lines, power and ground planes, vias, packages and materials). They also include the current in the vias since the electromagnetic waves propagations are considered on the X, Y and Z axes, and thus provide accurate results.

However, FEM 3D solvers are memory resources-hungry and require very long simulation times. They are ideal for analysing small systems but would be too consequential if used for analysing crosstalk in ultra-dense PCBs. 2.5D solvers would be more fitting though, surface and density-wise, but their modelling mode is simpler and less precise than FEM 3D solvers, making the ensuing results less accurate [7].

Consequently, modelling complex and ultra-dense boards proves to be a challenging matter, as they are not easy to accommodate to present solver methods. The boards that Atos develop for the *BullSequana*TM Supercomputers range are destined for High Performance Computing (HPC) applications : they can reach 22 layers and have usually 2 processors functioning at very high currents (>200A) and low voltages, powered by fast switching power supplies, which creates coupling noise on nearby sensitive signals. We therefore aim to spot the coupling effects stirred by the power supplies on the neighbouring signals before the board manufacturing, rather than during the prototype testing. As there isn't currently a reasonable way to do so, our objective is to implement a simulation method, using existing EDA tools, that would allow us to visualize the disturbances that might occur on the sensitive signals near the power supplies.

In the remainder of this paper, we suggest a method consisting of a simulation flow using a 2.5D solver tool; *ADS SI/PI pro*TM from Keysight Technologies Inc.[®], applied to a board developed by Atos, that enables the detection of a coupling phenomenon between a power supply and a nearby sensitive signal. Firstly, we introduce our case study, then we detail the procedure that led to our established simulation flow, and finally we compare the obtained results to the measurements of the case study.

II. CASE STUDY

The printed circuit board we choose to develop and validate our methodology is a small mezzanine board called CZBS (Compute Mezzanine BXI Single NIC), used for interconnections between HPC boards. The Bull eXascale Interconnect (BXI) network is a performance booster for communications in HPC applications; it manages the communications independently from the CPUs, leaving them to be fully dedicated to computational tasks [8]. The BXI Network Interface Connector (NIC) is mounted on the mezzanine board, and interconnects with the mother board through a PCI Express interface.

The CZBS board (*Fig.1*) is a 118mm x 130mm x 2mm 12-layer PCB (*Fig.2*), made of 2 external layers, 4 internal routing layers, and 6 power and ground planes. It contains an Application-Specific Integrated Circuit (ASIC), mainly powered with a voltage of 0.9V, delivered by a buck converter from a 12V input voltage. The power supply,

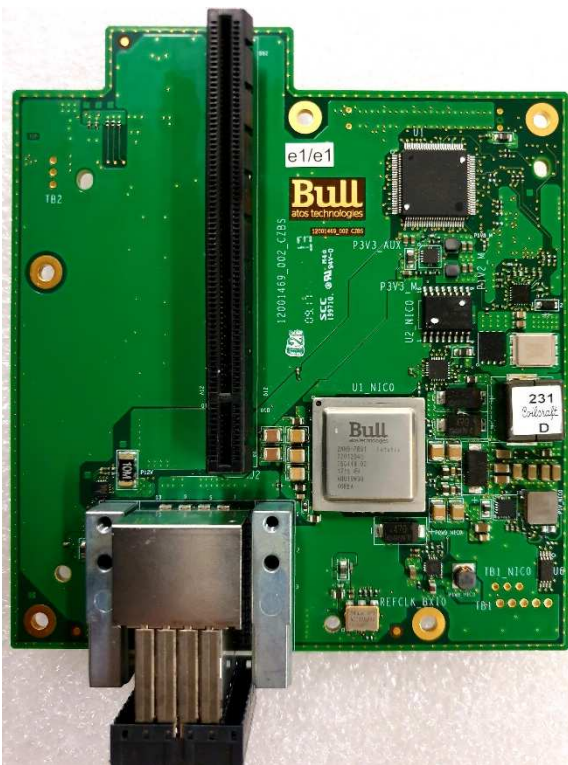


Fig. 1. Top view of the case study

placed on the *top* layer, causes disturbances on some neighbouring signals, especially on the enable signal of a clock buffer on the first routing layer (*L1*), right under the power supply. As we can see in *Fig.3*, this signal spreads under the transistors, the inductor, and near the switching node of the buck converter. For clarity purposes, only the elements involved in our case study appear in *Fig.3*, the other components, vias and layers are not shown.

The choice of this board as a case study is motivated by the presence of crosstalk between the power supply and the clock enable signal, while being small enough to allow a reasonably fast modelling in an EDA tool. The aim of our study is to be able to simulate the coupling effect and observe the disturbances on the victim signal, through a refined modelling of the studied system, and correlate to measurements on the actual board.

III. SIMULATION PROCESS

To achieve our goal, we aspire to reproduce the interaction between the power supply and the clock enable signal through simulation, using as precise a modelling of the case study as possible.

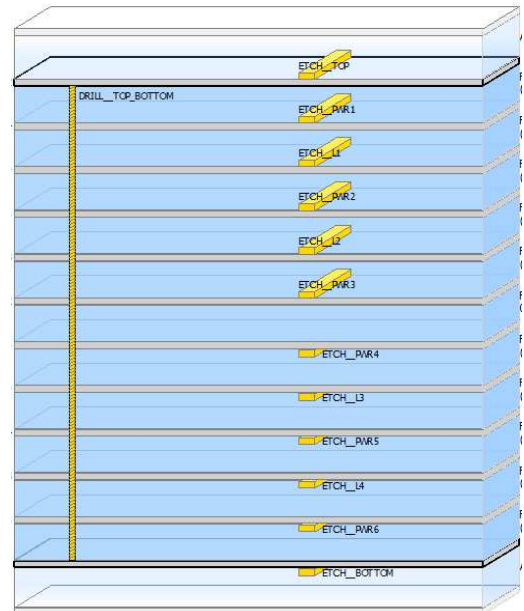


Fig. 2. Cross section of the case study

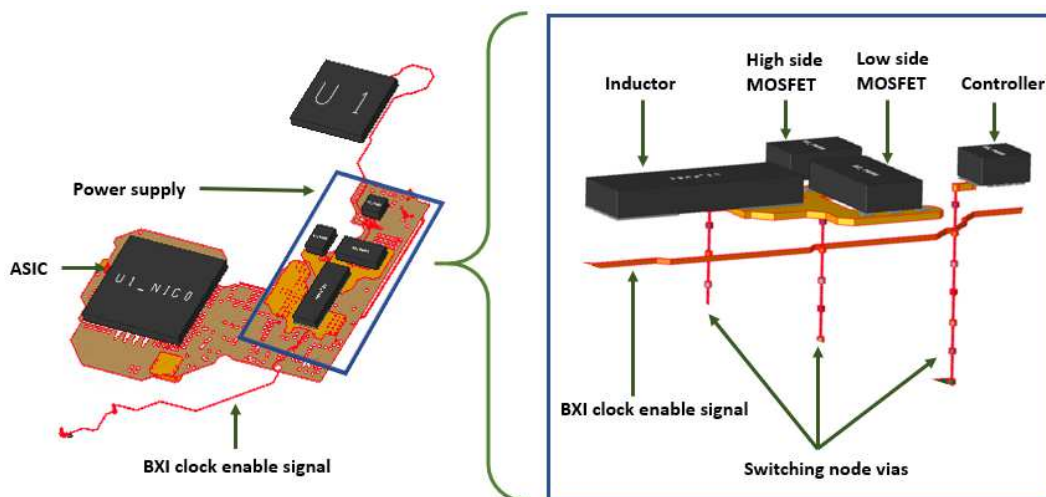


Fig. 3. 3D view of the case study's layout

A. Simulation overview

To ensure the accuracy of our depiction, we need to consider all the elements involved in the coupling phenomenon, meaning:

- The PCB layout, which contains the aggressor and victim signals, and whose properties greatly affect the quality of the signal transmission. The PCB is modelled using the ADS Signal Integrity (SI) simulation tool to extract the layout of the board, and therefore capture signals and power planes' behaviours in an S-parameters model.
- The power supply, which generates the perturbations on the victim signal, is emulated by its SPICE model.

Both models (PCB extraction and power supply models) are to be merged in a transient analysis.

B. Basic simulation method

Regarding the PCB modelling part, we run an SI analysis consisting of components' ports (the MOSFETs, inductor, decoupling capacitors, and load of the considered buck regulator, as illustrated in Fig.4), and nets involved in our case study (the required signals for the power supply functioning, and the clock enable signal). In *ADS SI/PI pro*TM, the nets are sorted into categories (ground, power, or signal), depending on their functions. We use a logarithmic analysis, with a 100Hz - 10GHz frequency range, and 100 points/decade. The extractor takes about a day to simulate our design in a 64GB machine and supplies the results in an S-parameters format, containing 48 ports.

Concerning the buck converter modelling, we use the SPICE electrical models of the driver and MOSFETs provided by their manufacturer. For more accurate results, we include a lumped model of the PDN, obtained from the above-mentioned SI simulation, in the SPICE analysis of the power supply. The PDN parasitic effects being included, their impact on the converter performance are thus considered in generating realistic gate command signals.

The transient simulation we launch includes the results of both the layout SI modelling and the power supply SPICE analysis. It contains the S-parameters model of the layout, the components involved in the case study, and the gates'

drive signals of the MOSFETs. Fig.5 displays the simulation flow in a detailed diagram.

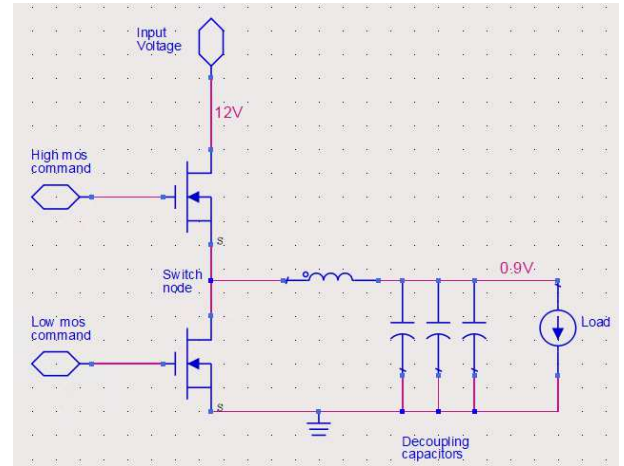


Fig. 4. Buck power supply circuit

C. Limits of the standard approach

The obtained results using the SI tool default setup relate to a very optimistic configuration, as the disturbances are barely apparent. We infer that the ground planes might be considered too ideal, and that the current return paths might not be modelled accurately enough. They indeed play a major role in our case study, as the power supply is isolated from the victim signal by a ground plane, which if deemed ideal, over-shields the two elements from the coupling between them. We therefore need to integrate the real behaviour of the ground planes to the PCB modelling, to get more accurate results.

The S-parameters block representing the PCB contains the ports of the components used in the modelling, and a reference node. Each port has a positive pin and a negative one, representing the positive and negative terminals of the components. However, as indicated in Fig.6-a, the negative pins are not accessible to the user [9]. The measurable voltages at the positive pins relate to $(V_{pn+}-V_{ref})$. The reference node is a mathematical node chosen amidst the ground planes, which form the reference planes in the analysis, and is connected to the circuit ground (node 0) [10].

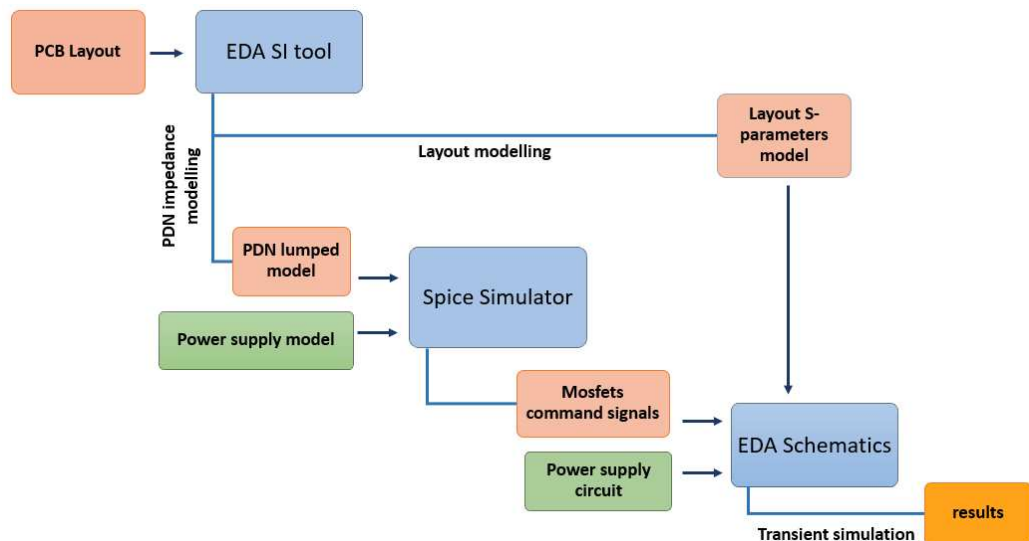


Fig. 5. Simulation flow diagram

We assume that the lack of crosstalk noise on our victim signal is due to the ground planes being assigned as reference, and hence indirectly connected to a perfect ground (node 0) through the reference node.

We therefore seek to verify the signals' behaviours at each components' terminal. To be able to observe them, we need an S-parameters structure that has a port for each terminal, as represented in *Fig.6-b*.

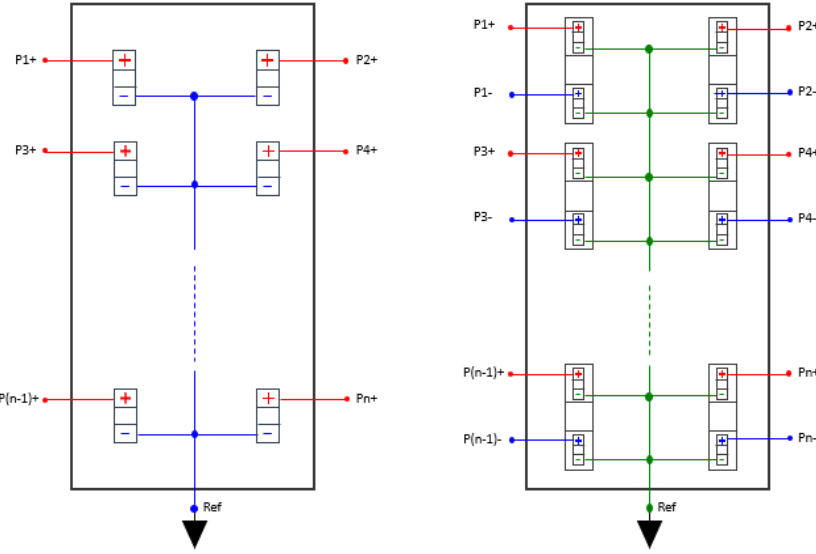


Fig. 6. a- Basic S-parameters structure b- Required S-parameters structure

D. Suggested solution

To do so, we proceed by creating an additional virtual layer, above the *bottom* layer, on which we place a ground plane. We consider this layer virtual because it doesn't exist on the board, it is added solely for analysis purposes, since it is mandatory for the analysis to use a ground net as reference.

We choose to place it above the *bottom* layer, so it doesn't disturb the studied system in any way, for it is as far away from the case study as possible. *Fig.7* shows the cross section of the modified layout, with the added virtual layer, between the sixth power plane and the *bottom* layer.

We describe this plane as the only GND plane for the analysis, thus the only one being connected to the ground pin reference of the S-parameters block. Consequently, since it is not directly connected to the components, they aren't affected by the supposed ideality of the reference. The real ground planes of our board are simply set as power planes, and thereby conserve their characteristics.

Through this procedure, the actual GND planes are more accurately modelled (since they are not connected to the reference ground), and the S-parameters block has now a port for each positive and negative pins of each component, allowing us to visualize the actual signals circulating in the circuit, by measuring the difference between the ports matching the positive and negative terminals of the components ($V_{p_{n+}} - V_{p_n}$). The new S-parameters structure contains 88 ports, since 40 ports out of

the 48 ones from the first structure have now ports representing their positive and negative pins (namely the decoupling capacitors, the load, the power sources and the low MOSFET). The 8 other ports correspond to components' pins that are not connected to the ground in our board.

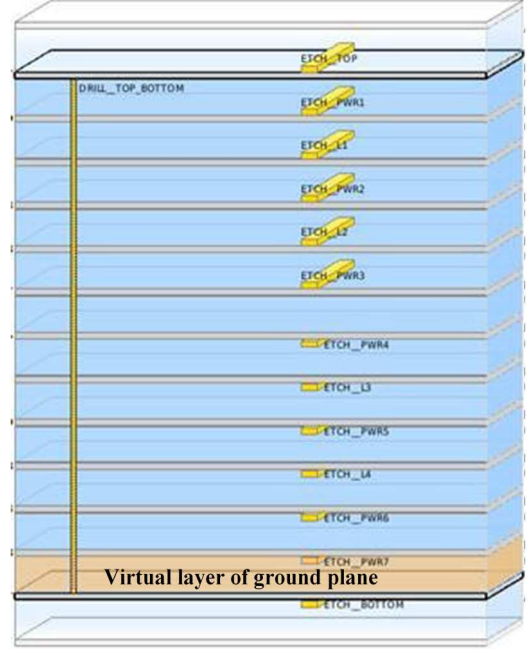


Fig. 7. Cross section of the modified design

IV. RESULTS

Fig.8 displays the evolution of the aggressor and victim signals of our case study. The aggressor (red), is the converter's switch signal, which presents a typical behaviour of a switch node, with a 7.5% duty cycle, and a 440kHz switching frequency. The victim (blue) is the clock enable signal, which should ideally be a 3.3V static signal. We can clearly see that the noise on the victim signal and the switching of the aggressor are synchronous.

The reference results in *Fig.8-a* are obtained by measurement with a 1GHz bandwidth oscilloscope, which ensures the crosstalk noise isn't filtered. *Fig.8-b* and *c-* are the simulation results from a transient analysis and represent the standard and revised simulation methods respectively.

As shown in *Fig.8-b*, the standard simulation does not cover the crosstalk modelling between the power supply and the victim signal, considering that we can hardly distinguish any noise on it at all. On the other hand, *Fig.8-c* shows that with our approach, the crosstalk disturbances are clearly visible, and match the measurements. A first order comparison indicates that the obtained disturbances indeed resemble the measured ones in shape, and in amplitude to a lesser extent.

Out of the possible reasons for this difference in amplitude, the aggressor's behaviour stands out. The switch node seems indeed to be stronger in simulation than in measurements, which could explain why the noise amplitude on the victim signal in the simulation is greater

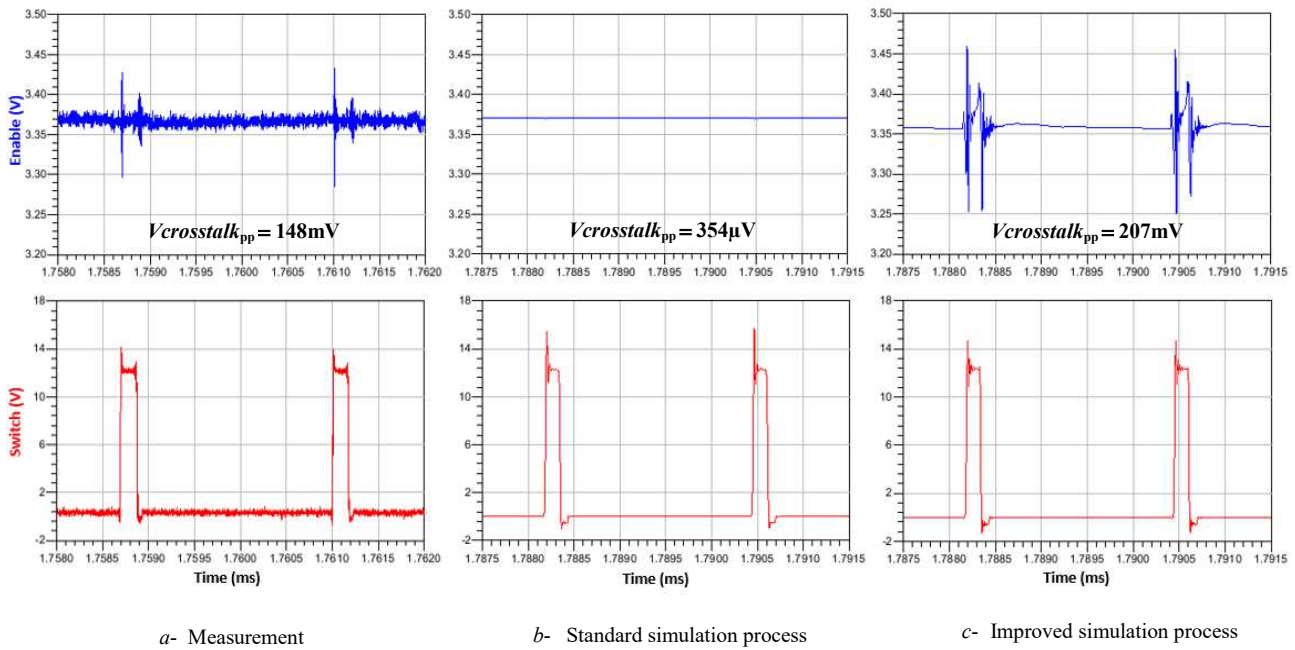


Fig. 8. Time-domain waveforms of aggressor and victim signals in initial case study board

than expected. However, our simulation method remains efficient, since we are now able to spot the crosstalk noise on the victim signal, in a dense PCB, using a 2.5D solver.

The crosstalk noise level on our case study seems a bit excessive, we therefore modify the board by adding more decoupling capacitors and a gate resistor to the power supply system, in order to reduce the coupling. We apply our simulation process to the altered design layout and compare the results to the measurements on the revised board, as shown in Fig.9. The aim of this step is not to correct the board per se, since the noise detected on the victim signal is not relevant to the functioning of the system, but to further corroborate the consistency of our simulation method.

Measurements in Fig.9-a reveal that the coupling is considerably reduced with the revised board, as we can barely distinguish the disturbances caused by the switching node from the random noise. Fig.9-b shows that similarly, the noise level in the simulation, is reduced in equal proportions.

The results from the revised board therefore validate the accuracy of our simulation flow and confirm the significance of its application in virtual prototyping. In our case study, our simulation method allows us to ensure that the modifications made to the board are indeed efficient, in reducing the coupling on the victim signal.

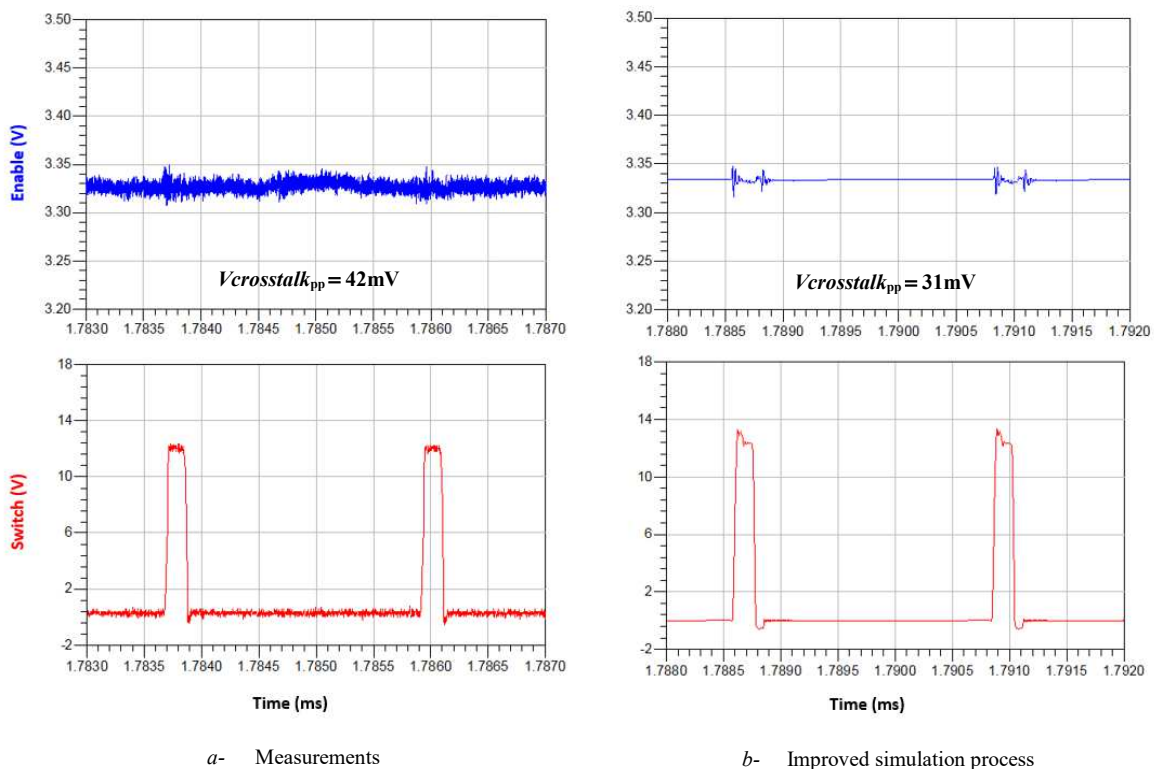


Fig. 9. Time-domain waveforms of aggressor and victim signals in revised case study board

V. CONCLUSION

A simulation method is proposed to improve the modelling of the coupling between a power supply and a neighbouring signal in a multi-layer PCB, and depict the crosstalk on the victim signal, by ensuring the current circulation in the ground planes is accurately represented.

A basic analysis doesn't allow the visualization of the coupling noise through ground planes on the victim signal because the extraction tool generates an S-parameter block whose reference is chosen amidst the ground planes assigned to the analysis. Consequently, the GND planes' behaviour described in the S-parameters model is not realistic and imparts an optimistic performance of the case study.

Our method involves adding a virtual ground plane to the design, set it as reference in the modelling tool, and consider the actual ground planes of the board as power planes, thus allowing the crosstalk noise on the victim signal to be fully observed. This simulation process is verified and validated by comparison between the simulation results and the measurements of a case study board bearing a coupling issue, and its revised version.

Our simulation method being validated on a small and rather simple case study, we aspire now to generalize it so we can apply it to all types of boards that Atos develop, which can be much more intricate than the CZBS. We are currently applying it to a larger, denser, and more complex compute board: a 532mm x 184mm x 2.38mm 18-layer PCB, containing 2 CPUs which require very high currents and very fast low voltage signals. The SVID (Serial Voltage Identification Debug) signals on this board present some coupling noise due to their nearness to the VRMs (Voltage Regulator Model) that power the CPUs. These properties make this design a perfect case for testing our simulation method and evaluating the resources it requires, in complex and ultra-dense boards.

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