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# ON-state reliability of GaN-on-Si Schottky Barrier Diodes: $\text{Si}_3\text{N}_4$ vs. $\text{Al}_2\text{O}_3/\text{SiO}_2$ GET dielectric

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**Abstract**—The degradation of Schottky Barrier Diodes (SBDs) with a Gated Edge Termination (GET) under on-state stress conditions is studied for a 650 V GaN-on-Si technology. Reliability metric techniques previously used in MOS-HEMTs are applied in this work due to similar MIS gate stack architecture in GET-SBDs. In these techniques, the density of traps ( $\Delta N_{\text{OT}}$ ) is analyzed in GET structures where the dielectric is either  $\text{Si}_3\text{N}_4$  (nitride-based) or a stack of  $\text{Al}_2\text{O}_3/\text{SiO}_2$  (oxide-based). Statistical analysis across both wafers indicates some systematic differences in turn-on voltage degradation ( $\Delta V_{\text{TON}}$ ) depending on wafer location, likely caused by process-related variations. Under 1000 s stress time and ON-state voltage, the number of trapped charges in nitride-based dielectric devices keeps increasing. This suggests an ongoing dielectric degradation. On the other hand,  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric devices with an Al-based interfacial layer (IL) exhibit less process-induced variability across the wafer along with a lower density of trapped charges compared with nitride-based dielectric diodes under the same stress conditions suggesting better reliability and process improvement.

**Index Terms**-- de-trapping, GaN, interfacial layer, nitride, on-state, oxide, trapping rate.

## I. INTRODUCTION

The rapid development of power electronics applications requires advanced devices to improve the efficiency and the power density of conversion systems. In the last years, devices based on gallium nitride (GaN) have been considered attractive and promising in this field due to their wide bandgap ( $\sim 3.4$  eV) and high values of breakdown voltage ( $\sim 3\text{MV}/\text{cm}$ ), saturation velocity, sheet carrier density, and electron mobility in the 2-D electron gas (2-DEG) quantum well formed at the AlGaIn/GaN heterojunction [1]. Despite the potential of this material, its widespread adoption in the power market is still limited due to reliability issues that are not yet fully understood. Several studies have been performed in different GaN-based structures to comprehend the degradation phenomena and to analyze long-term reliability [2], [3], [4].

However, the lack of consensus about the failure mechanisms needs more research on this topic.

Some of the requirements of GaN-based power diodes include high breakdown voltage ( $V_{\text{BD}}$ ) and low values of turn-ON voltage ( $V_{\text{TON}}$ ), specific ON-resistance ( $R_{\text{ON,sp}}$ ), and reverse leakage current. Therefore, several processing approaches have been implemented to improve the performance of GaN-on-Si rectifiers. One of these is the introduction of a  $\text{Si}_3\text{N}_4$  layer at the corner of the Schottky contact to create a gated edge termination (GET) that reduces the electric field peak in this corner and the reverse current [5]. Reliability improvements under OFF-state stress conditions have been obtained in this structure by thinning the passivation layer and by employing a more aggressive pre-clean process based on sulfuric acid and hydrogen peroxide mixture (SPM) and ammonia and hydrogen peroxide mixture (APM) [6]. This improved structure was fabricated in a 200-V GaN-on-Si platform and tested under ON-state stress conditions. The results demonstrated a recoverable behavior with better reliability and longer lifetime expectation compared to previous works in 200-V technology [7]. Although promising results were obtained, a clear method to link the process to the reliability in ON-state regime is missing. This makes the analysis highly dependent on the fabrication instead of physics mechanisms.

This paper aims to study the reliability of the aforementioned improved structure for 650V GaN technology. It is worth reminding that the GET resembles a metal-insulator-semiconductor structure bringing about material compatibility concerns at the semiconductor AlGaIn-barrier/dielectric interface. In-situ defects at this interface may be critical as in MOS-like devices (MOSFET or MOS-HEMT) [2], [8]. Therefore, it is reasonable to apply reliability techniques (e.g. positive bias temperature instability-PBTI) and metrics like the ones successfully applied to MOSFETs. By using these metrics, it is possible to assess the number of defect centers in the insulator/oxide layer or far from the interface. More specific estimation of interface defects require

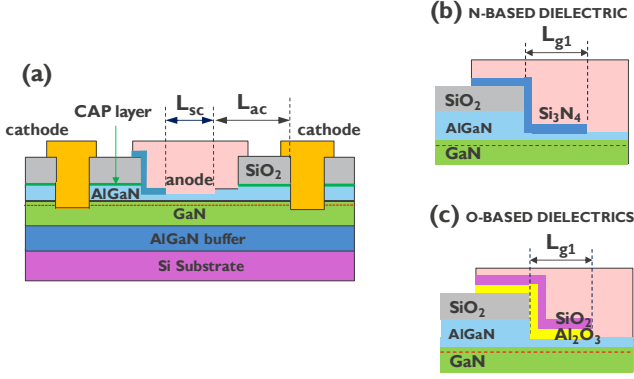


Fig. 1. Simplified schematics of (a) GET-SBDs used for ON-state stress analysis. Gate stack architecture with Si<sub>3</sub>N<sub>4</sub> (b) and Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> (c).

other techniques [9], [10], and are not included in this work. We also show a comparative study of this architecture by using a nitrogen-based dielectric made of 45 nm of Si<sub>3</sub>N<sub>4</sub> and an oxide-based dielectric made of 35 nm of SiO<sub>2</sub> deposited onto an interfacial layer of Al<sub>2</sub>O<sub>3</sub> (2.5 nm).

The remainder of this paper is organized as follows. Section II presents details of the devices under test. Section III explains the experimental procedure. ON-state stress results are discussed in Section IV. Finally, the conclusions of this paper are summarized in Section V.

## II. DEVICE FABRICATION

The schematic structure of the AlGaIn/GaN diodes studied in this paper is depicted in Fig. 1(a). The epitaxial stack is grown on a Si (111) substrate by means of metal-organic chemical vapour deposition (MOCVD). It features a thick superlattice buffer designed for a 650-V platform technology with a 300-nm-thick GaN channel, a 0.5-nm-thick AlN spacer, a 10-nm-thick Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier, and a 5-nm-thick SiN cap. The epitaxial stack is passivated with a SiO<sub>2</sub> layer using high-temperature oxide deposition.

In the anode region, the passivation layer is removed by dry etch and the barrier is recessed by about ~6nm using atomic layer etching. The GET reference structure has a nitrogen (N)-based dielectric, which is formed by depositing a 45-nm-thick Si<sub>3</sub>N<sub>4</sub> layer by means of plasma-enhanced atomic layer deposition (PEALD). A subsequent opening by dry etching in the central region defines the actual Schottky contact with a length L<sub>sc</sub> = 4 μm, an edge termination length L<sub>g1</sub> = 2 μm and an anode-to-cathode distance L<sub>ac</sub> = 16 μm as illustrated in Fig. 1(b). An Au-free TiN-based metal stack is then deposited and etched to form the Schottky contact at the anode region [5]. Finally, the ohmic contacts are processed using a Ti/Al-based metal stack with an alloying temperature of 565 °C.

For this comparative study, a second wafer was fabricated with a bilayer in the GET region, which includes an oxide (O)-based dielectric as shown in Fig. 1(c). For this structure, a 2.5-nm-thick interfacial layer (IL) of Al<sub>2</sub>O<sub>3</sub> was deposited by atomic layer deposition followed by a 35-nm-thick layer of SiO<sub>2</sub> deposited by means of plasma-enhanced chemical vapour deposition (PECVD).

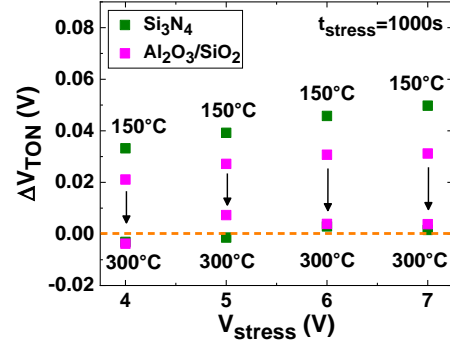


Fig. 2. Total ΔV<sub>TON</sub> after 1000s of stress at 150°C and the recovery of the initial state after a thermal de-trapping (TD) process at 300°C in Si<sub>3</sub>N<sub>4</sub> and Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> dielectric devices.

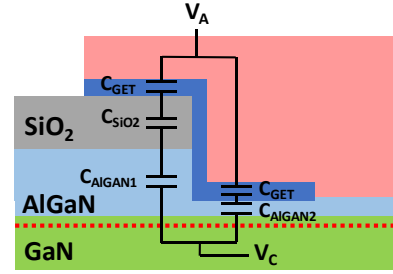


Fig. 3. Schematic model to obtain C<sub>eff</sub> which is 0.18 μF/cm<sup>2</sup> and 0.13 μF/cm<sup>2</sup> for Si<sub>3</sub>N<sub>4</sub> and Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub>, respectively.

## III. EXPERIMENTAL PROCEDURE

The technique to assess the dielectric reliability for GET-SBDs starts with an initial stabilization phase in which a voltage (6V) is applied at high temperature (150 °C) followed by a thermal de-trapping (TD) with floating contacts at 300 °C. This procedure releases charges originally trapped in defect centers within the GET dielectric and captures the real degradation under the stress conditions. It is worth noting that the I-V curves almost overlap the fresh I-V curves (not shown for the sake of brevity) after the stabilization for the Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> devices, which indicates lower amount of initially trapped charges. Subsequently, during the stress phase, the devices are biased with a positive anode-to-cathode stress voltage (V<sub>stress</sub>) ranging between 4 V and 7 V. To capture the degradation, the stress was interrupted at fixed time intervals (Measure-Stress-Measure technique MSM) up to 1000 s. An I-V curve was measured and compared with the fresh (reference) one obtained in the stabilization phase to calculate the ON-state threshold voltage shift (ΔV<sub>TON</sub>), which for these structures is always positive indicating an electron trapping process. Finally, the thermal-de-trapping process (300 °C) is applied again to release the trapped charges during the stress and to prepare devices for subsequent experiments. It is worth highlighting that after the thermal de-trapping (TD) process following the stress phase, the diodes can almost completely recover from the stress-induced degradation during the experiments. A small non zero ΔV<sub>TON</sub> is observed in Fig. 2 and could be explained by a permanent component residue. This procedure was performed in 64 diodes across the wafers.

The ΔV<sub>TON</sub> is directly related to the trapped charge density ΔN<sub>OT</sub> through:

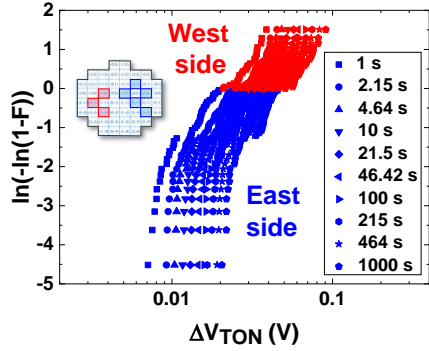


Fig. 4. Weibull distributions of  $\Delta V_{TON}$  at  $V_{stress}=6V$  and  $T=150^\circ C$  in  $Si_3N_4$  dielectric devices. Two trends are observed depending on the wafer location.

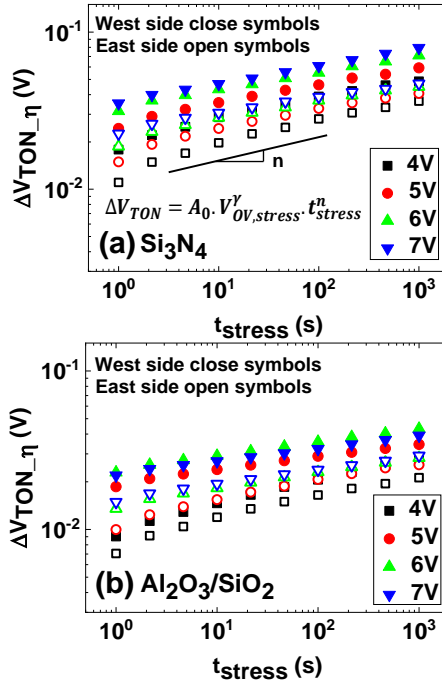


Fig. 5. Weibull scale parameter of  $\Delta V_{TON}$  ( $\Delta V_{TON,\eta}$ ) obtained under different stress voltages as function of the stress time for (a)  $Si_3N_4$  and (b)  $Al_2O_3/SiO_2$  diodes, respectively. These measurements were performed at  $150^\circ C$

$$\Delta N_{OT} = (C_{eff} * \Delta V_{TON})/q \quad (1)$$

where  $C_{eff}$  is the effective capacitance per unit area that has been obtained with the electrical model in Fig. 3 and  $q$  is the elementary charge. This model focuses on the region around  $V_{TON}$  where the capacitance remains fixed [11].

#### IV. RESULTS AND DISCUSSION

The degradation results under ON-state stress show two different probability trends according to the wafer location. An approximately twice higher degradation is observed on the west side compared to the east side of the wafer, which can be attributed to process-induced or systematic variability under large forward stress. Indeed, stress voltages from 4V to 7V were applied to the anode-cathode contact which is well above the usual operating forward voltage for these devices, namely  $V_F=1.83 V$  and  $1.74V$  for the N-based and O-based dielectric devices, respectively. More explanation about this observation was reported in our previous work [7]. In both cases, a Weibull distribution is found to fit well the data. Fig. 4 shows

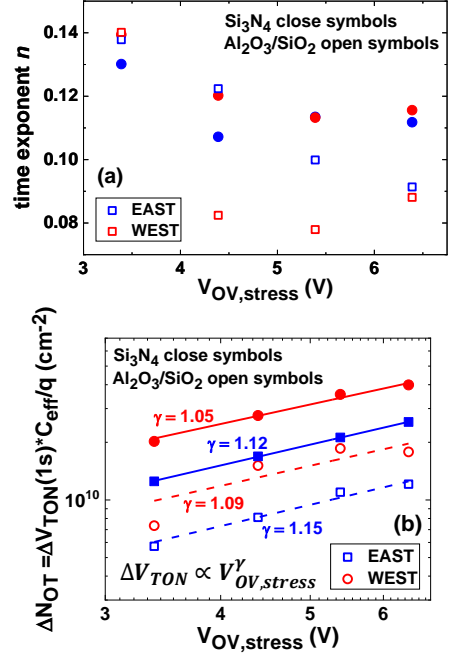


Fig. 4. (a) Time exponent  $n$  and (b)  $\Delta N_{OT}$  as a function of the  $V_{OV,stress}$ .

an example for a stress voltage  $V_{stress}=6V$ . Similar results were obtained for all experiments.

##### A. Nonlinear dependence model

From the Weibull distributions, the scale parameter ( $\eta$ ) is plotted vs. stress time in Fig. 5 ( $\Delta V_{TON,\eta}$ ) for different stress conditions. Large forward stress in the ON-state regime produces  $\Delta V_{TON}$  shifts in the range from 5 to 100 mV.  $\Delta V_{TON,\eta}$  was observed to follow a power law of the stress time and stress overdrive voltage and the data fit well with the model proposed in [8]:

$$\Delta V_{TON,\eta} = A_0 \cdot V_{OV,stress}^\gamma \cdot t_{stress}^n \quad (2)$$

where  $A_0$  is the prefactor,  $n$  is the time exponent,  $\gamma$  is the voltage dependence exponent and  $V_{OV,stress}$  is the difference between the stress voltage and the initial measured  $V_{TON}$ :

$$(V_{OV,stress} = |V_{stress} - V_{TON_{initial}}|). \quad (3)$$

As depicted in Fig. 6 (a), the extracted time exponent  $n$  exhibits a decreasing behavior with  $V_{OV,stress}$  independently of the GET dielectric  $Si_3N_4$  or  $Al_2O_3/SiO_2$ . Moreover, its range agree with BTI reports in different technologies [8], [12], [13].

The trapped charge density  $\Delta N_{OT}$  is extracted after 1-s stress in Fig 6 (b), by using (1). The value of the voltage dependence exponent  $\gamma$  about 1 (east side) and 1.15 (west side) suggests the existence of a wide distribution of defect levels centered around the channel Fermi level [8]. This indicates similar accessibility to the dielectric defects in both types of GET dielectrics.

It is worth mentioning that  $\Delta V_{TON}$  evolution during the stress can also be expressed by using a semi empirical model [13]:

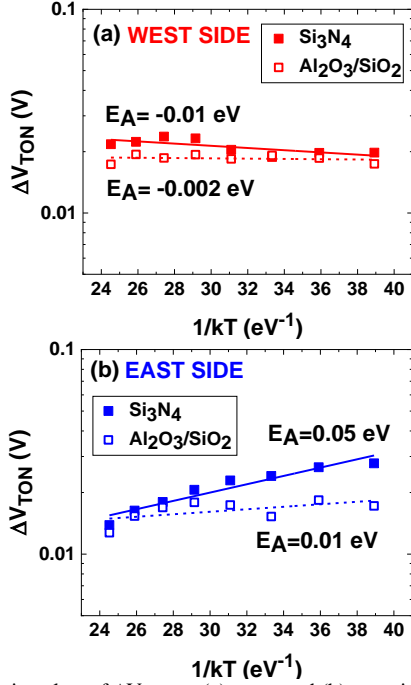


Fig. 7. Arrhenius plots of  $\Delta V_{TON}$  on (a) west- and (b) east-side devices. The  $\Delta V_{TON}$  values were extrapolated when the devices were stressed at 4V for 1s.

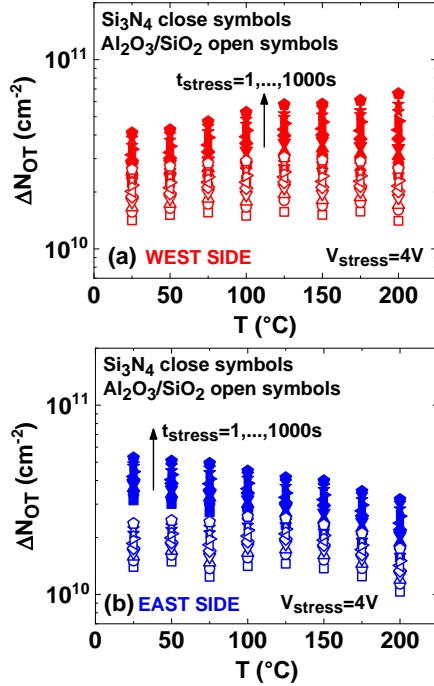


Fig. 8.  $\Delta N_{OT}$  as a function of temperature on (a) west- and (b) east-side devices.

$$\Delta V_{TON,n} \approx \exp(-E_A/k_B T) (V_{OV, stress}/t_{ox})^y t_{stress}^n \quad (4)$$

The apparent  $\Delta V_{TON}$  activation energies are extracted by fitting an exponential trend in the Arrhenius plots as depicted in Fig. 7. To assess the mean activation energy of the charge capture process, it is necessary to consider the time to reach a given  $\Delta V_{TON}$ . Therefore, the apparent activation energy is divided for the time exponent  $n$ . The mean activation energies

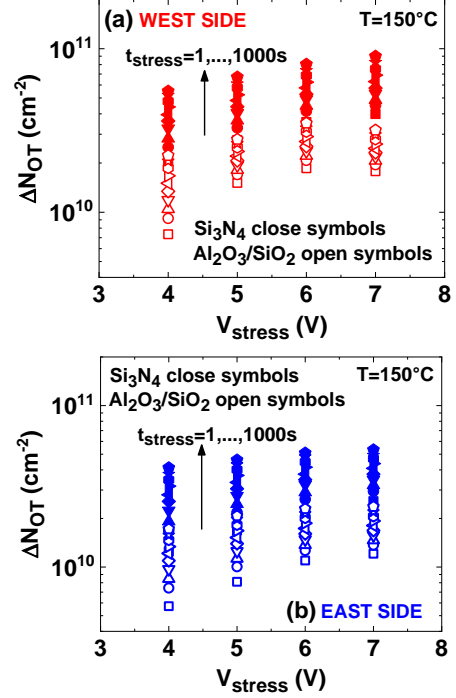


Fig. 9.  $\Delta N_{OT}$  as a function of stress voltage on (a) west- and (b) east-side devices.

in west-side devices were estimated to be  $-0.072/-0.014$  eV ( $n$  is  $0.139/0.140$ ) for  $\text{Si}_3\text{N}_4$  and  $\text{Al}_2\text{O}_3/\text{SiO}_2$  GET dielectrics, respectively. In the case of east-side devices, the values were  $0.384/0.073$  eV ( $n$  is  $0.130/0.138$ ).

By considering the database of the deep levels in GaN- and AlGaN-based devices [14], such low values can be ascribed to nitrogen vacancies. The relatively high value of  $0.384$  eV in  $\text{Si}_3\text{N}_4$  devices in the east side can be possibly related to AlGaN surface.

Temperature and stress voltage conditions in Fig. 8 and 9, respectively, show different reliabilities and variabilities depending on the GET dielectric. For the  $\text{Si}_3\text{N}_4$  GET-SBDs,  $\Delta N_{OT}$  is lowered for the east-side devices suggesting a de-trapping phenomenon enhanced by temperature while the west-side devices show the opposite trend. On the other hand, the temperature has a low influence in the trapping and de-trapping process in  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric independently of the side of the wafer. As a result, the  $\text{Si}_3\text{N}_4$  dielectric produces more trapping phenomena with larger variability than  $\text{Al}_2\text{O}_3/\text{SiO}_2$  devices under the same stress conditions (Fig. 8 and 9), yet with similar activation energies as previously shown in Fig. 7.

### B. Trapping rate parameter analysis

To gain insight into the  $\Delta V_{TON}$  behavior for these different devices, the time exponent  $n$  is evaluated as a function of the stress time:

$$n(t_{stress}) = b = \partial \log \Delta V_{TON} / \partial \log t_{stress} \quad (5)$$

where  $b$  is the so-called *trapping rate* or *b-parameter* [2].

The  $b$ -parameter measures the evolution of the ratio between the trapping and de-trapping mechanisms under

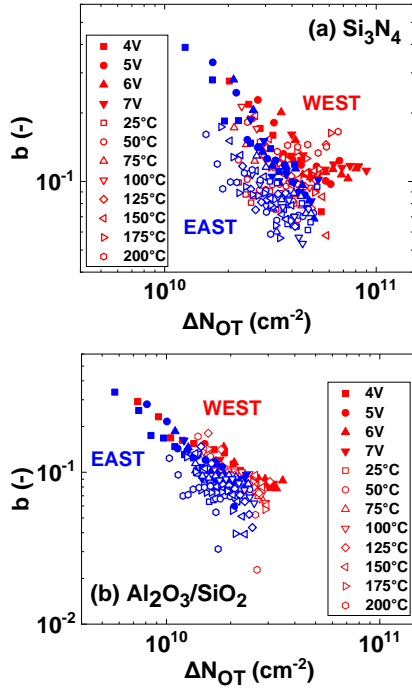


Fig. 10.  $b$ -parameter as a function of the  $\Delta N_{OT}$  in (a)  $\text{Si}_3\text{N}_4$  and (b)  $\text{Al}_2\text{O}_3/\text{SiO}_2$  GET-SBDs. Stress voltage and stress temperature experiments were performed at 150 °C and 4V, respectively.

given stress voltage and temperature conditions. This parameter is plotted in Fig. 10 as a function of the defect density ( $\Delta N_{OT}$ ) for all stress conditions. As illustrated in Fig. 10 (a), the  $\text{Si}_3\text{N}_4$  devices have a significant variability across the wafer. The west-side devices exhibit larger trapping density compared to the east side (maximum of around  $4.10^{10} \text{ cm}^{-2}$ ) and this density even increases with larger stress voltages (6-7V) and temperatures, which indicates further trapping of charges under these stress conditions. This different behavior between east- and west-side devices confirms the variability of the wafer observed in the first place.

For  $\text{Al}_2\text{O}_3/\text{SiO}_2$  devices, Fig. 10 (b) shows much more uniformity or less variability across the wafer. The  $\Delta N_{OT}$  is limited to a fixed value of about  $2\text{-}3.10^{10} \text{ cm}^{-2}$ . A somewhat lower density of traps is reached for the east-side devices.

It is important to mention that an important  $\Delta N_{OT}$  increase (kink) under harsh stress conditions, especially in  $\text{Si}_3\text{N}_4$ -devices located on the west side, is observed in Fig. 10 (a). This indicates that the amount of trapping keeps increasing with the stress time, voltage, and temperature. In this case, this ongoing increase could suggest either deeper trapping in the dielectric material or creation of defects at the dielectric interface or within the dielectric. Although the devices exhibit an apparent recoverable behavior, where the creation of defects is not conceived, we cannot discard the possibility of a permanent degradation component that under high temperature (from 300 °C) of the thermal de-trapping process can be reversed or “baked away” [15].

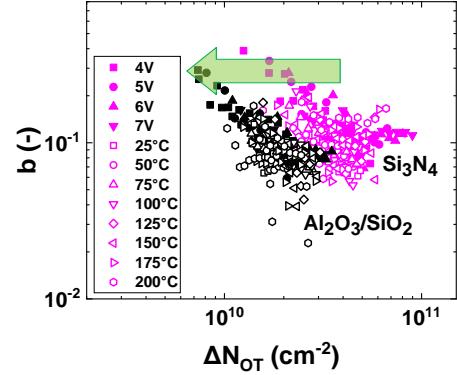


Fig. 11.  $\Delta N_{OT}$  comparison between wafer sides under stress voltage conditions between  $\text{Si}_3\text{N}_4$  and  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric GET-SBDs. Lower density of traps and variability are observed for the metal-oxide bilayer.

On the contrary, for the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  devices on the west side, the  $\Delta N_{OT}$  kink is less prominent suggesting that the deep trapping in the oxide is limited by the temperature de-trapping process which is more efficient than for the  $\text{Si}_3\text{N}_4$  devices (Fig. 8 (a)).

In the east-side devices independently of the GET dielectric,  $\Delta N_{OT}$  saturates at high-stress voltages and decreases at high temperatures (Fig. 8 and 9). Therefore, it is possible to say that pre-existing defects at the interface/dielectric can be saturated with electrons. The longer the stress time applied, the larger the number of trapped charges. At some point, the dielectric interface cannot trap any more electrons due to the de-trapping process enhanced by temperature or trapped electrons that prevent further trapping of charges within or at the border of the dielectric [16], [17].

Fig. 11 proposes a metric summarizing the specificity of the two different dielectric materials: stress voltage dependence, trapping/de-trapping rate and interface quality. It shows important correlations between the  $\Delta N_{OT}$  increase, the trapping rate, and the variability across the wafer. For the same  $b$ -parameter values,  $\Delta N_{OT}$  is lower for  $\text{Al}_2\text{O}_3/\text{SiO}_2$  compared to  $\text{Si}_3\text{N}_4$  GET dielectric. From low to large stress conditions, it can be noted that the variability is increased as demonstrated by the increased data scattering for large  $\Delta N_{OT}$ , especially for the  $\text{Si}_3\text{N}_4$  dielectric. Also, and more importantly, under larger stress voltage (7V), the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  devices do not increase  $\Delta N_{OT}$  as it is the case of the  $\text{Si}_3\text{N}_4$  devices, especially in west-side devices. It is worth mentioning that the amount of trapping for both dielectrics remains low: even for the  $\text{Si}_3\text{N}_4$  with larger variability,  $\Delta N_{OT}$  stays below  $10^{11}/\text{cm}^2$  under large forward stress voltage.

For both types of dielectrics, we assume that the defects are mostly located at the dielectric /AlGaN interface. Indeed, we can suggest that the increase of trapped electrons indicates deeper trapping in the dielectric or a generation of defects that must be located in a region of the gate dielectric which exhibits weak atomic bonds. This can be a material defect where the atomic compatibility is not fully ensured. For instance, the trapped electrons on the interface could build a



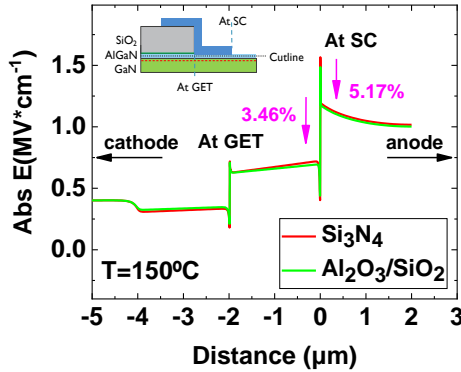


Fig. 12. Line profile of the absolute electric field within the AlGaIn barrier (3 nm below the top surface in the recessed portion) for N-based and O-based dielectric GET-SBDs. The IL helps reducing the electric field at the gate.

potential barrier preventing deep trapping inside the dielectric. Therefore, we can also speculate that a constant increase of the amount of defects is present at the bottom of the gate dielectric (namely the interface with the AlGaIn Barrier). Although these defects may be located at the interface between two materials, they are still considered as bulk or dielectric defects since they are far from the place where the current (AlGaIn/GaN) is flowing. In the case of an oxide-base dielectric, an interfacial layer (IL) of  $\text{Al}_2\text{O}_3$  is deposited on the AlGaIn. Based on the reliability results in Fig. 11, we speculate that the  $\text{Al}_2\text{O}_3$  IL deposited before the  $\text{SiO}_2$  may enable better compatibility between the  $\text{SiO}_2$  and the AlGaIn barrier, and this is likely related to the use of Al. This explains again why for large stress voltages, there is almost no generation of defects or deeper dielectric trapping at the  $\text{Al}_2\text{O}_3/\text{AlGaIn}$  interface compared to the  $\text{Si}_3\text{N}_4/\text{AlGaIn}$  one.

Finally, the use of O-based IL seems also to reduce the peak of the electric field intensity at the AlGaIn barrier according to the TCAD simulation as shown in Fig. 12. It may somewhat also improve the b-parameter reduction under large stress voltage. This can also be related to the use of higher-k value IL as suggested in the case of MOS-HEMTs [18].

## V. CONCLUSIONS

In this paper, we have presented the results of ON-state stress degradation in AlGaIn/GaN SBDs fabricated in a 650 V technology with either N-based or O-based GET dielectrics. A nonlinear dependence model and the change in density of traps ( $\Delta N_{\text{OT}}$ ) are used as reliability metrics in this work. The choice of the GET dielectric and the resulting properties of the GET dielectric/AlGaIn interface are proven to be critical. Results suggest that the GET dielectric region is where the generation of defects or deeper charge trapping under high voltage stress conditions could take place. A reduced  $\Delta N_{\text{OT}}$  for the process involving the O-based dielectric with  $\text{Al}_2\text{O}_3$  IL is observed compared to the N-based dielectric. Better uniformity of the results across the wafer and a more stable maximum of  $\Delta N_{\text{OT}}$  for large stress voltage (up to 7V) are also observed. Therefore,  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric yields better

reliability and lower variability across the wafer suggesting a better quality of the AlGaIn-barrier/dielectric interface and more uniform process control than with  $\text{Si}_3\text{N}_4$  dielectric. It makes ALD  $\text{Al}_2\text{O}_3/\text{PECVD SiO}_2$  dielectric a more attractive option for the 650V AlGaIn/GaN SBDs technology.

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