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Design of Integrated Laser Diode Driver for 3D-Depth Sensing Applications

Romain [a,b], [a], [b] and [a]

[a] University of Lyon, University Claude Bernard Lyon 1, INSA Lyon, CNRS, Ampère, F-69621, Villeurbanne, France
[b] STMicroelectronics, Analog, MEMS & Sensors Group, 12 Rue Jules Horowitz, 38019, Grenoble B.P. 217, France

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ABSTRACT

This paper presents the design and comparison of two integrated CMOS Laser Diode Drivers (LDD) intended for 3D-depth sensing applications used in mobile phones and based on the indirect Time-of-Flight (iToF) measurement. Architectures are based on known driver topologies where a standard DC/DC converter is connected to a switching element either in series or parallel to provide pulses. Two LDD prototypes have been implemented on-chip using a 130nm CMOS technology from STMicroelectronics. Both prototypes are able to generate current pulses up to 3A with a 2.5ns pulse width at a maximum 200MHz Pulse Repetition Frequency (PRF) under a 3.6V supply voltage. In these conditions, measurement results report an average output electrical power of 4.5W with an electrical efficiency of 58% and 62% for series and shunt configuration respectively.

1. Introduction

Nowadays, emerging applications such as facial recognition, gesture control or Augmented Reality (AR) are in great demands in consumer electronics [1]. Developing a 3D image sensor able to map the surrounding area in three dimensions would benefit these applications. The indirect Time-of-Flight (iToF) measurement technique offers the advantage of a straightforward, robust and low cost implementation for mobile applications by using a laser transmitter and an image sensor [2][3]. Its operating principle is to calculate a depth by measuring the phase shift between a modulated infrared laser signal and the optical signal received by the sensor after reflection on an object from the scene. The block diagram of a typical iToF-based image sensor is illustrated in Figure.

Generally, laser pulses with a duty cycle close to 50% are sent through the scene as the modulated signal, corresponding to the Continuous Wave (CW) modulation [4]. A high optical power of laser pulses as well as a high Pulse Repetition Frequency (PRF) are desired to improve the depth resolution σ_z in iToF systems, as defined by

$$\sigma_z \propto \frac{c}{4\sqrt{2}\pi f} \cdot \frac{\sqrt{P_{OPT}}}{P_{OPT}} \tag{1}$$

where c is the speed of light, f is the PRF and P_{OPT} is the peak optical power at the laser emitter level [5]. Moreover, multiple frequencies are needed to extend the maximum unambiguous range, due to the phase shift wrapping every 2π, without impacting the measurement accuracy [6].

Depending on the maximum targeting depth, lighting conditions, object reflectivity, sensor efficiency, the choice of the laser diode and eye-safety standards, current pulses up to few Amps at a frequency from tens to hundreds of MHz

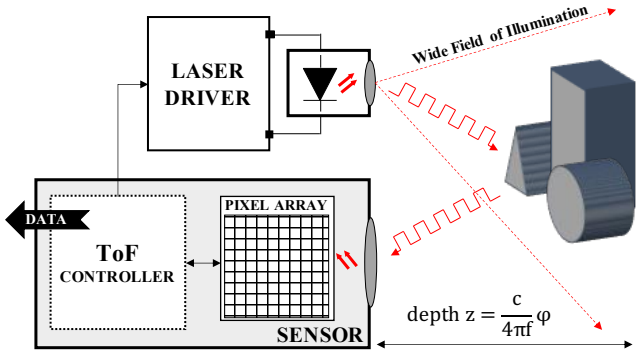

Figure 1: Block diagram of a typical iToF-based image sensor. The depth formula is indicated, where φ is the phase shift, f is the modulation frequency and c is the speed of light.

are required to reach a millimeter depth accuracy at few meters of distance. However, short pulse trains are needed to avoid thermal dissipation issues and human eye damages according to laser safety standard [7].

These specifications introduce new challenges in the design of a compact, low-cost and efficient Laser Diode Driver (LDD). Main concerns are the high level of current and the shaping of short-duration pulse at high repetition frequency because of the parasitic elements in passive components and PCB interconnections. In addition, mobile applications bring strong constraints in design choices such as dealing with the restricted available space and accommodating the limited input voltage range of a battery (2.5-4.8V). Finally, a high efficiency in the chip is critical for saving the battery lifetime and minimizing any self-heating.

This paper focuses on the design and comparison of two known driver topologies: series and shunt what means the laser diode is connected either in series or parallel with a switching element in order to provide current pulses. In addition, a standard DC/DC converter is used for controlling the current through the laser diode with a high efficiency.

romain.david@etu.univ-lyon1.fr (R. David)
ORCID(s): 0000-0001-9946-7791 (R. David)

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The novelty here concerns the feasibility of integrating the whole solution (except laser diode and passive components). Current pulses can be configurable up to 3A peak for a PRF from 50MHz to 200MHz with a 50% duty cycle under typical conditions. Section 2 provides a quick review on various circuits from the literature. Section 3 explains the operating principle of the proposed architectures for the LDD. Section 3 describes the on-chip implementation of the two integrated LDD prototypes. Experimental results performed on both prototypes with a laser diode are reported in Section 4. Finally, last section discusses future works and concludes the paper.

2. LDD Topology Background

Several works have been published presenting LDDs for ToF applications with various current, pulse width and PRF specifications. Drivers may be divided into two major classes according to the classification described in [8]. The classification depends on how the pulse is controlled. There are resonant capacitive discharge drivers and rectangular pulse drivers.

2.1. Resonant capacitive discharge drivers

Although several configurations can be distinguished from circuits in [9][10][11][12][13], they are based on the same operating principle firstly proposed by Kilpelä et al. in [14]. A schematic is shown in Figure 2 in a basic version. This type of drivers rely on a capacitive discharge through a switch and laser diode to generate a pulse by triggering the rising edge only.

This topology has a relatively simple design accepting the stray inductance into its operation. The laser pulse energy is well controlled, thus eliminating thermal runaway and providing an improved pulse-to-pulse repeatability [8]. However, a major drawback concerns the pulse width that depends on the capacitor and stray inductance, which are fixed for a given design, while the pulse amplitude depends on the supply voltage and the capacitor too [10]. Therefore, it is impossible to control the pulse width and amplitude separately. Another issue is the long time needed to charge the capacitor thus limiting the PRF. Moreover, a relatively high supply voltage may be required to achieve a high peak current what may increase the design complexity, cost and space needed by the whole circuit.

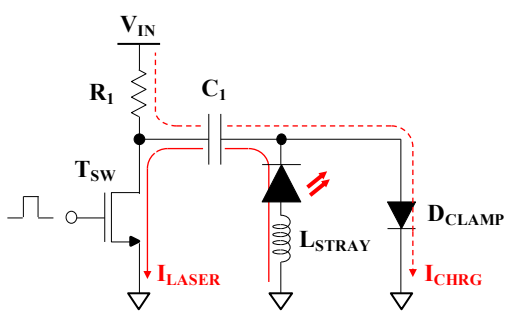


Figure 2: Simplified schematic of the resonant capacitive discharge driver topology.

2.2. Rectangular pulse drivers

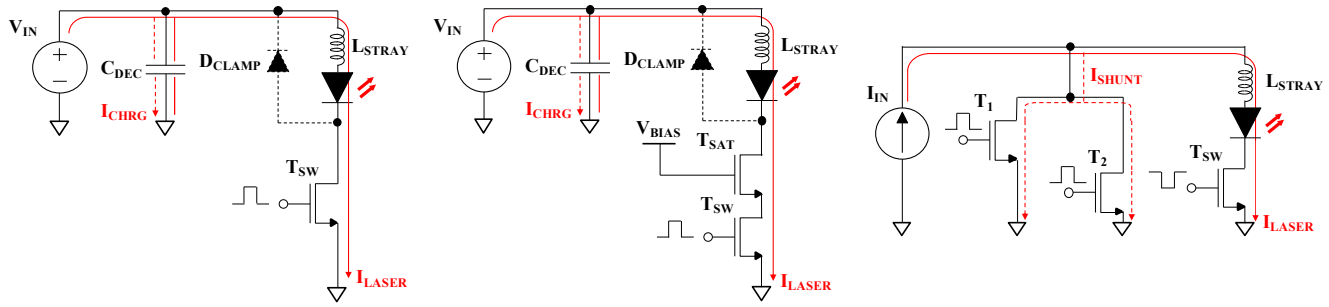
Rectangular pulse drivers generates current pulses by triggering both the rising and falling edges. Then, two types of driving mode can be distinguished for controlling the laser diode biasing: the voltage-mode driver based on a voltage source or the current-mode driver based on a current source.

Driver circuits presented in [13][15] are considered here as voltage-mode drivers using a series configuration, as illustrated in a basic version in Figure 3a. A voltage source is connected in series to a laser diode and a switch. This topology benefits from a control of the pulse width and a high PRF can be reached due to the use of a relatively large decoupling capacitor [8]. Moreover, the peak current is independent of the pulse-width setting and only a control of the laser diode biasing voltage is required to adjust its value. These features allows flexible pulse sequences. However, the supply voltage needs to be high enough to overcome the stray inductance. Furthermore, control loops may be required to ensure pulse-to-pulse repeatability due to temperature and voltage variations [15].

Other circuits reported in [16][17] are considered here as current-mode drivers using a current source configuration, as illustrated in a basic version in Figure 3b. A laser diode is connected in series to a low-side current source and a switch, thus acting as a switched current generator. A voltage source is still used to provide a constant voltage to the laser diode. Even if flexible pulse sequences can be achieved with a high PRF, a major limitation concerns the relatively high dissipated power through the switched current generator when turned on due to the sufficient voltage headroom required for its proper biasing [16].

An alternative approach developed in [18] is considered here as a current-mode driver using a shunt configuration, as illustrated in a basic version in Figure 3c. A current source is connected to a laser diode and an assembly of three switches to provide current pulses by shunting the current from the laser diode to the ground. As for previous configurations, flexible pulse sequences with a high PRF can be considered. Nevertheless, whereas several switches are used allowing a more precise control of the current pulse width, it contributes to increase the power consumption and chip size due to additional gate drive circuits.

The circuits considered in this short review are mostly intended for LiDAR applications where constraints in term of power losses are more flexible than for mobile applications and the technologies used might also be specific and incompatible with a low cost requirement, such as GaN FET in [13][15], BCD in [17] or LDMOS in [18]. However, the voltage-mode driver topology in series configuration as well as the current-mode driver topology in shunt configuration seem to be good candidates for developing a low-cost integrated driver in standard 130nm CMOS technology able to generate short and high current pulses at a high PRF while operating at a low input voltage range and considering the power efficiency as a leading requirement.



(a) Voltage-mode driver in series configuration.

(b) Current-mode driver in current source configuration.

(c) Current-mode driver in shunt configuration.

Figure 3: Simplified schematic of the rectangular pulse driver topologies.

3. Driver Architectures and Operating Principle

3.1. Voltage-mode Driver in Series Configuration

A simplified schematic of the proposed architecture for the voltage-mode driver in series configuration is illustrated in Figure 4. It consists of a buck-boost DC/DC converter and a switch connected in series to the laser diode. This DC/DC converter acts as a current-controlled voltage source for biasing the laser diode by adjusting the output voltage according to the input voltage and the desired current. The switch is triggered by a modulation signal in order to generate current pulses. The current-control loop actually monitors the average current I_{avg} through the laser diode while the peak current value I_{peak} is controlled by the duty cycle α of the modulation signal, approximated as

$$I_{peak} = \frac{I_{avg}}{\alpha} \tag{2}$$

The switching frequency of the converter can be selected sufficiently low (<10MHz) compared to the PRF (50MHz-200MHz) in order to benefit from relatively low switching losses and some flexibility for implementing the feedback loop. The output voltage provided by the converter is thus seen relatively constant during the pulse duration leading to a stable current pulse. A power inductor with low value (L_{OUT} ~ hundreds of nH) and an output capacitor with high value (C_{OUT} ~ µF) can be selected to ensure a low output voltage ripple.

3.2. Current-mode Driver in Shunt Configuration

A simplified schematic of the proposed architecture for the current-mode driver in shunt configuration is illustrated in Figure 5. It consists of a modified buck DC/DC converter and a switch connected in parallel to the laser diode. This buck DC/DC converter is used without output capacitor. It thus acts as a current-controlled current source for biasing the laser diode by adjusting the output current according to the input voltage and the desired current. The switch is triggered by a modulation signal in order to shunt the current to the ground thus generating current pulses. In contrast to the previous voltage-mode driver architecture, the current-control loop monitors the average current through the inductor which corresponds to the peak current through the laser diode. The switching frequency of the converter can be selected sufficiently low (<10MHz) compared to the PRF (50MHz-200MHz) in order to benefit from relatively low switching losses and some flexibility for implementing the feedback loop. The output current provided by the converter is thus seen relatively constant during the pulse duration leading to a stable current pulse. A relatively high value for the power inductor (L_{OUT} ~ µH) is also necessary to maintain a low inductor current ripple.

4. IC Implementation

This section details the design and implementation of two integrated LDD prototypes based on the architectures previously described. An integrated solution is essential in order

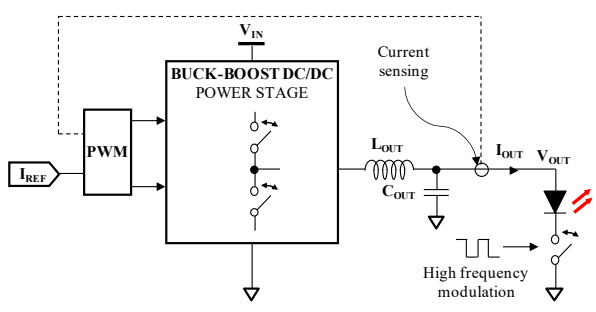


Figure 4: Simplified schematic of the voltage-mode driver topology in series configuration.

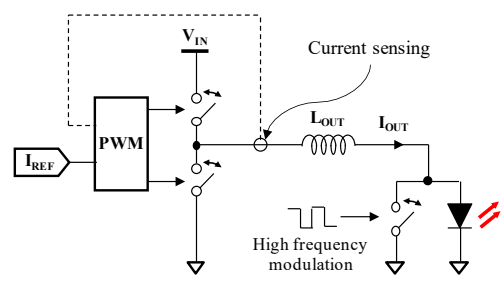
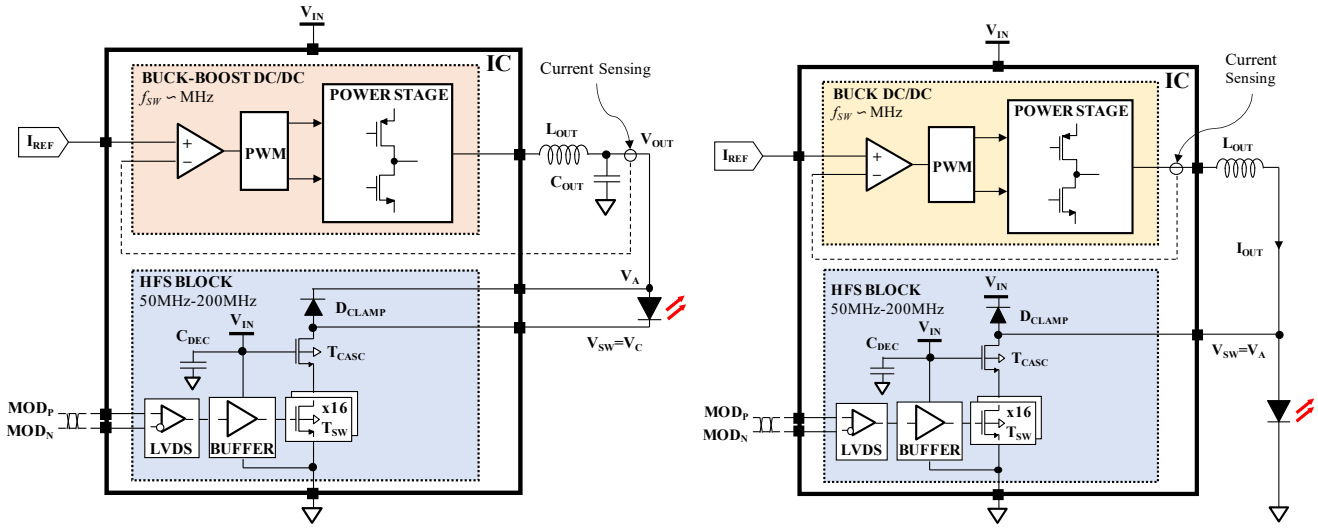


Figure 5: Simplified schematic of the current-mode driver topology in shunt configuration.



(a) Voltage-mode driver IC. (b) Current-mode driver IC.

Figure 6: Simplified block diagram of the two driver ICs. The current-control loops are inherent to the DC/DC converters.

to develop a compact, fast and low cost system. Indeed, it allows to overcome parasitic elements due to packages and interconnections thus improving transient performances, reducing losses and saving PCB footprint compared to a discrete approach. The selected 130nm CMOS technology employed here is inexpensive and well adapted to embed analog, digital and power features into a single chip.

Figures 6a and 6b show a block diagram of both voltage-mode and current-mode drivers. In order to save time and design resources, a non-inverting buck-boost DC/DC converter has been reused from previous developments to implement the DC/DC converter required by the voltage-mode driver topology. Although made of a specific architecture, it can be seen as a block able to step up or step down the output voltage according to the desired current. A more standard buck DC/DC converter, without output capacitor, has been reused as well to implement the DC/DC converter required by the current-mode driver topology. Both converters employ a standard Pulse Width Modulation (PWM) method using a current-control loop in order to adjust the output voltage according to the desired current value set by a current-level reference, as described in [19]. The converter architectures and their operating principles are not detailed here. The main contribution of this work concerns the design of the High Frequency Switching (HFS for short) block which aims to switch the current through the laser diode at a high frequency. Furthermore, only one HFS block has been designed since it has similar specifications for both drivers.

4.1. HFS Block

A thick oxide n-channel MOSFET transistor (NMOS), named T_{SW}, ensures the current switching at high frequency. It withstands voltages up to 4.8V. Since the peak current (up to 3A) and the PRF (50MHz-200MHz) are flexible, the gate width of the power transistor T_{SW} has been made programmable and divided into 16 equal parts for optimizing both conduction and switching losses. It is configurable here from 5.4mm to 86.4mm by step of 5.4mm. This transistor is driven by an external differential modulation signal through an appropriate driving circuitry. It consists of a simple tapered buffer and a Low Voltage Differential Signal (LVDS) receiver used to convert the fast differential signal (MOD_P and MOD_N inputs) into a single-ended modulation signal. A cascode transistor, named T_{CASC}, as well as a clamping diode are used to protect devices at the switching node V_{SW} from high voltage spikes due to parasitic inductances occurring during fast transient currents. Transistor T_{CASC} has been implemented using a thick oxide NMOS device with a 24mm gate width sized by considering a trade-off between its on-resistance and output capacitance. The additional clamping diode D_{CLAMP} is a typical P-N junction and has been sized large (458x71μm^2) enough to evacuate the residual energy from parasitic inductances.

4.2. Layout Considerations

Some layout considerations have been employed such as using isolation wells and guard rings in order to isolate the bulk of power devices from the substrate. It helps to reduce substrate coupling and minimize latch-up susceptibility due to carrier injection during fast transients. A dedicated power supply path with an assigned pin for each analog, digital and power domains has been used for minimizing the impact of noise between each block. Higher levels of metal with a large number of Vertical Interconnect Access (VIAs) in parallel are used for power routing. An integrated Metal-Insulator-Metal (MIM) capacitance, named C_{DEC}, has been implemented in the remaining silicon area for an effective decoupling of the buffer power supply, thus reducing the voltage ripple. For easy readability, only the physical layout of the HFS block (without the clamping diode because lo-

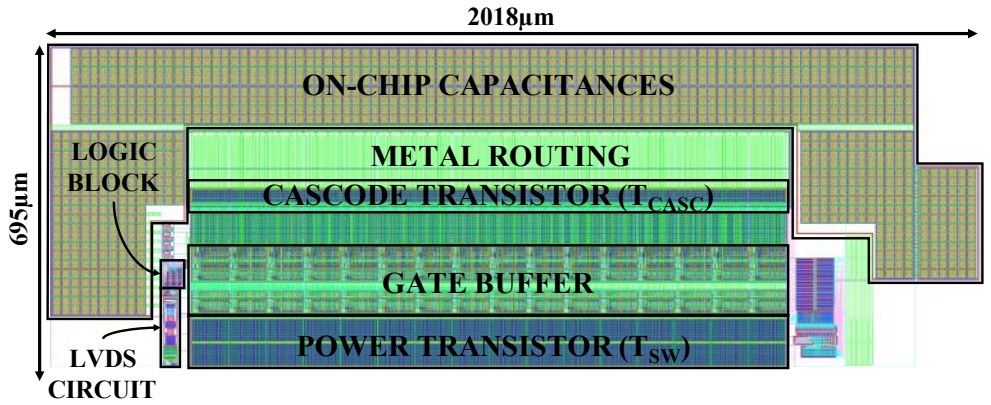


Figure 7: Physical layout of the HFS block.

Table 1
Main electro-optical characteristics of the VCSEL diode at 25°C.

Parameter	Value
Wavelength	940nm
Peak optical power (under pulsed conditions)	2.4W
Threshold current	300mA
Series resistance	400mΩ
Nominal current (under pulsed conditions)	3A
Forward voltage	2.7V
Slope efficiency	90%
Power Conversion Efficiency	28%

cated further in the chip) is illustrated in Figure 7. The overall silicon area for the voltage-mode and current-mode LDD prototypes are around 7.25mm^2 and 6mm^2 respectively.

Table 2
Post-layout simulation results for a 3A peak current with a 2.5ns pulse width at 200MHz under typical conditions.

Parameter	Value	
Driver	Voltage-mode	Current-mode
Pulse width (50%)	2.6ns	2.5ns
Rising time (10%-90%)	1.9ns	1.0ns
Falling time (90%-10%)	900ps	2.2ns
Peak current	3.5A	3.7A
Average current	1.5A	1.8A
Output voltage	5.0V	-
Voltage spike at V_{SW}	7.8V	7.9V
Output power	4.2W	4.9W
Driver input power	6.8W	8.2W
Dissipated power in IC	2.6W	2.8W
Electrical efficiency	62%	60%

5. Simulation Results

Post-layout simulations with parasitic models of package and PCB have been carried out with a SPICE simulator to validate the circuit implementation and to evaluate performances of the LDD prototypes. A Vertical-Cavity Surface Emitting Laser (VCSEL) array diode module has been chosen as load with respect to specifications. Main electro-optical characteristics are summarized in Table 1. The Power Conversion Efficiency (PCE) is defined as the output optical power over input electrical power ratio of the VCSEL module. The slope efficiency is defined as the output optical power over input current ratio of the VCSEL module. These parameters are only given at 25°C room temperature due to lack of data from VCSEL suppliers.

An electrical SPICE-based diode model is considered for simulation, stating a 2.7V forward voltage for reaching a 3A peak current. The equivalent stray inductance in the laser diode and HFS block current paths has been evaluated at 1.5nH for the voltage-mode driver (as a series configuration is employed). For the current-mode driver, the stray inductance has been evaluated at 800pH through the laser diode current path and 700pH through the HFS block current path (as a shunt configuration is employed).

Results for a 3A peak current with a 2.5ns pulse width at 200MHz under typical conditions (typ. process, 3.6V input voltage, 25°C room temperature) are summarized in Table 2. The output power accounts for the average power provided by the driver to the laser diode module during several modulation periods in steady-state while the input power is the average power provided by the power supply to the chip during the same time period. The electrical efficiency is the output power over input power ratio. The dissipated power in IC accounts for total losses due to the integrated circuit only, not including off-chip passive components. The gate width of transistor T_{SW} has been properly chosen for minimizing total losses. Transient waveforms of interest are illustrated in Figure 8 and 9 for the voltage-mode and current-mode drivers respectively.

Although a proper gate signal is provided to the power transistor T_{SW}, a strong distortion on the laser diode current is noticed. It is caused by the strong parasitic inductances, where the rising time is slower than the falling time for the voltage-mode driver while this is the opposite for the

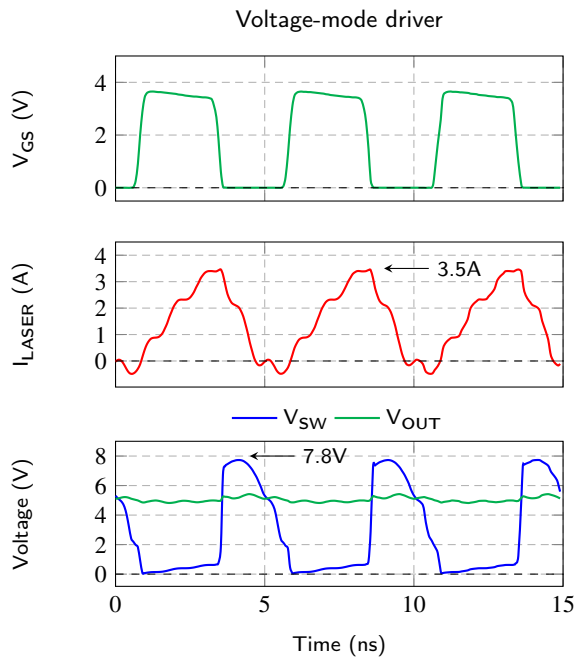


Figure 8: Simulation transient waveforms for the voltage-mode driver: gate-source voltage of transistor T_{SW} (top), laser diode current I_{LASER} (middle), switching node voltage V_{SW} (bottom, blue) and output voltage V_{OUT} (bottom, green) for a 3A peak current with a 2.5ns pulse width at 200MHz under typical conditions.

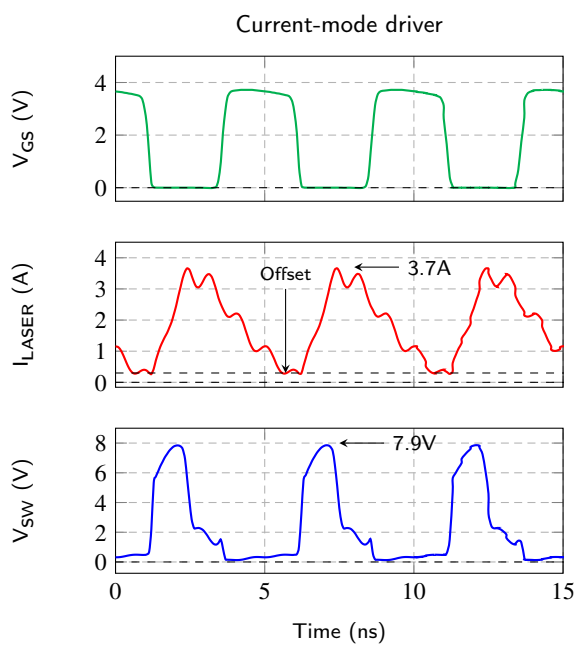


Figure 9: Simulation transient waveforms for the current-mode driver: gate-source voltage of transistor T_{SW} (top), laser diode current I_{LASER} (middle) and switching node voltage V_{SW} (bottom) for a 3A peak current with a 2.5ns pulse width at 200MHz under typical conditions.

current-mode driver. This particularly impacts the current-mode driver where the current is not totally shunted at the end of a pulse bringing an offset that causes the average current through the laser diode to increase, as noticed in Table 2. The average current regulation for the voltage-mode driver is disturbed as well, leading to a higher peak current (3.5A) than expected, what is explained by the clamping diode inducing a low reverse current.

Voltage spikes are noticed at the switching node in each case, what seems to be clamped to some extent by the clamping diode. Even if over voltages above 4.8V are reported, the cascode transistor T_2 still ensures a protection for the power transistor. It can also be noticed that a 5V output voltage against a 3.6V input voltage is required for the voltage-mode driver to reach the desired current, confirming that a buck-boost structure is essential for this kind of driver topology with respect to specifications.

Finally, whereas efficiency values around 60% are reported, the figures seem reasonable in typical conditions at first order. In addition, although parasitic inductances have a strong impact on transient performances, simulation results validate the circuit implementation, proving that both drivers are able to generate high current pulses at high frequency. The equivalent stray inductance could be reduced with a proper PCB design.

6. Experimental Results

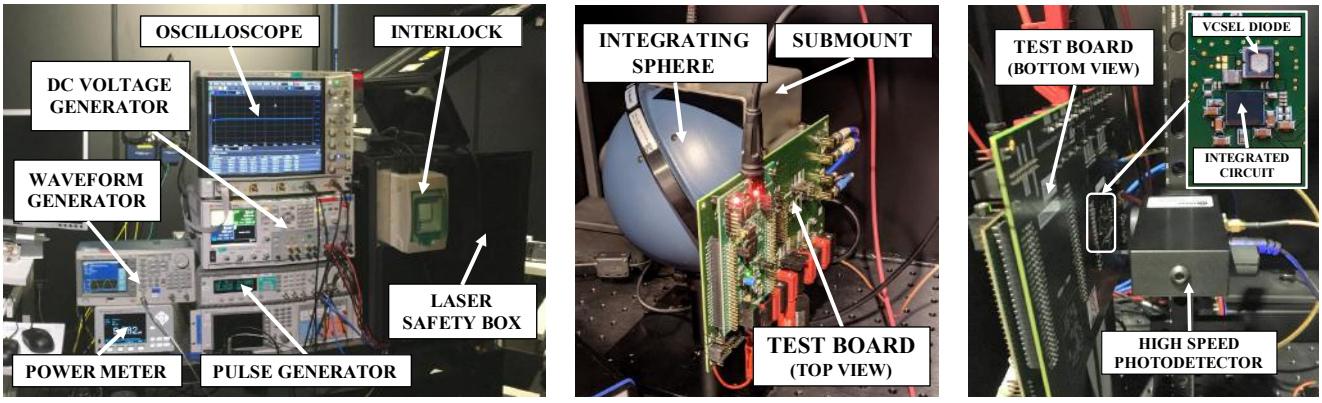
6.1. Measurement setup

A test bench has been set up for performing electrical and optical measurements, as shown in Figure 10. The VCSEL module and each LDD prototype were assembled on a test board with optimized interconnections for easy configuration and improved measurements.

Figure 10a shows a Keysight N6705B DC power analyzer to generate the power supply, and a Agilent 81110A pulse generator as well as a Keysight 33600A waveform generator to respectively generate the differential signal (LVDS) and an envelope signal providing pulse trains. Figure 10b shows a Newport 819D-SL-5.3-CAL2 integrating sphere. Associated with a Newport 918D-SL-OD1R optical power detector and a Newport 1936-R optical power meter, this setup has been used for measuring average values of the optical power associated with a pulse train. The peak optical power P_{PEAK} of pulses is determined knowing the duty cycle α of the laser signal, such as

$$P_{PEAK} = \frac{P_{AVG}}{\alpha} \tag{3}$$

where P_{AVG} is the average optical power over a pulse train. Figure 10c shows a iCHaus ic212 high-speed free-space photodetector with a 1.4GHz bandwidth to acquire the laser pulse shape. Signals are measured with a Keysight MSOS-254A 2.5GHz mixed-signal oscilloscope. A short illumination pattern has been set to reduce self-heating effects as much as possible. Finally, a STM32F407 microcontroller from STMicroelectronics has been used for configuring the integrated circuit.



(a) Full test bench.

(b) Test board mounted on integrating sphere (viewed from inside the box).

(c) Test board with LDD prototype coupled to photodetector (viewed from inside the box, a zoom presents the IC, VCSEL diode and passive components).

Figure 10: Test bench for performing electrical and optical measurements. Due to laser safety standards, measurements have been performed in a laser safety box protected with an interlock.

6.2. Primary results and EMI issues

Primary electrical results have reported some interferences on an analog block within the chip while the current is switching (during a pulse train). This block is a bandgap voltage reference providing a fixed voltage of 1.22V used for the current-control loop. The bandgap voltage has been directly measured through a dedicated output pin for both the voltage-mode and current-mode drivers for various desired peak current and frequencies under typical conditions (3.6V input voltage, 25°C room temperature).

Results, presented in Figure 11, show that the bandgap voltage decreases as the peak current and frequency increase thus impacting the current regulation. The bandgap voltage drops down to 1.15V and 1.08V for the voltage-mode and current-mode drivers respectively while a 1.22V voltage level is expected. These interferences are probably due to a ground coupling between the HFS block and the bandgap circuit that may arise from interconnections through the substrate of the chip, metallization, PCB tracks and/or ground plane. Despite these EMI issues, the circuit can still be used in an open-loop manner by adjusting the desired peak current value. Following performance results are thus obtained in open-loop.

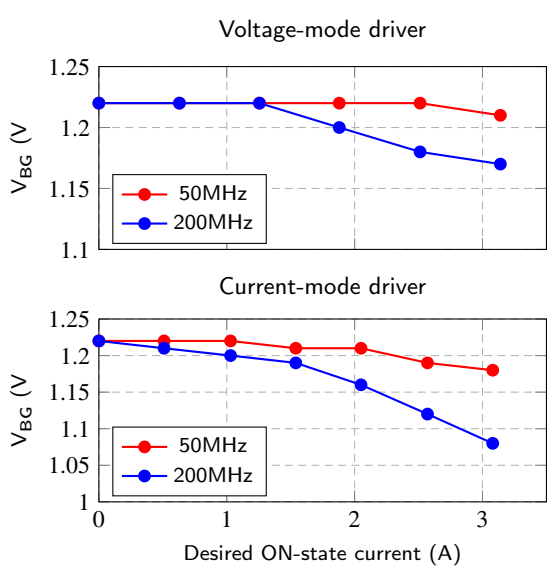


Figure 11: Measured bandgap voltage vs. desired peak current for both drivers and at various frequencies under typical conditions.

6.3. Performance results and comparison

Both prototypes have been measured using similar conditions in order to make a fair comparison. Since the current regulation may be disturbed due to EMI issues on the bandgap circuit, the peak current value was swept until reaching a desired peak optical power. The pulse width of the external differential modulation signal has been finely tuned to face a potential laser signal distortion. A 50% modulation duty cycle on the laser pulse shape was targeted. Then, transient performances such as rising and falling times, and electrical efficiency have been measured for comparison. The electrical efficiency is defined as

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{4}$$

where P_{IN} is the driver input power and P_{OUT} is the average electrical output power provided by the driver to the VCSEL module during a pulse train. Since the output current cannot be measured, P_{OUT} has been estimated from optical power measurements using the VCSEL PCE (see Table 1). The peak current value has been estimated using the VCSEL slope efficiency (see Table 1).

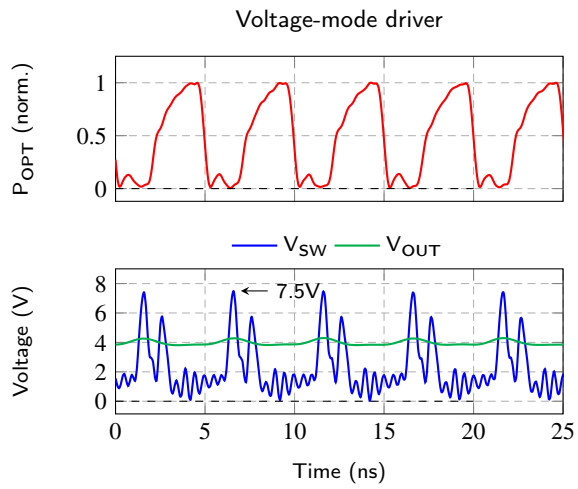


Figure 12: Transient measurement waveforms for the voltage-mode driver for a 2.5W peak optical power with a 2.5ns pulse width at 200MHz under typical conditions. The laser pulse shape is normalized on y-axis according to its maximum value. Important: electrical and optical waveforms are not in phase.

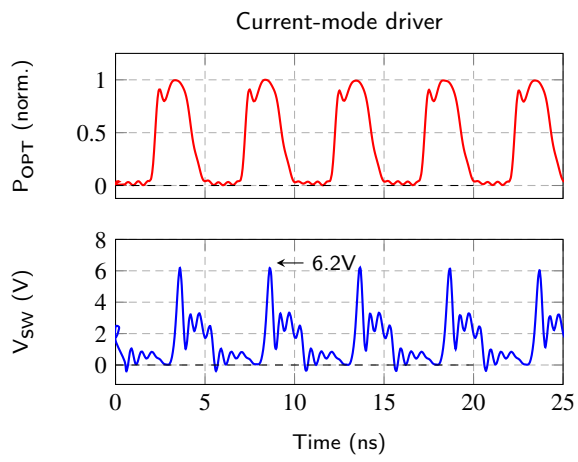


Figure 13: Transient measurement waveforms for the current-mode driver for a 2.5W peak optical power with a 2.5ns pulse width at 200MHz under typical conditions. The laser pulse shape is normalized on y-axis according to its maximum value. Important: electrical and optical waveforms are not in phase.

Transient measurement waveforms including the laser pulse shape are shown in Figure 12 and Figure 13 for the voltage-mode and current-mode LDD prototypes respectively. They are obtained while operating under typical conditions (3.6V input voltage, 25°C room temperature) for a targeted 2.5W peak optical power with a 2.5ns pulse width at 200MHz. The gate width of the power transistor has been properly chosen to minimize losses. Performance results are summarized in Table 3.

It can be noticed that both prototypes are able to generate laser pulses. A 4.1V output voltage is reported for the voltage-mode driver, indicating that a buck-boost structure is essential for this kind of topology with respect to the specifications. Slight voltage bounces are however observed on the output voltage which are mostly due to ESL of decoupling capacitors. Nevertheless, a voltage spike of around 7V has been observed on the switching node for both prototypes suggesting that the clamping diode is less efficient than expected.

Table 3
Results summary for both drivers for a 2.5W peak optical power with a 2.5ns pulse width at 200MHz under typical conditions.

Parameter	Value	
Driver	Voltage-mode	Current-mode
Peak optical power	2.47W	2.51W
Peak current	3.05A	3.09A
Output power	4.50W	4.49W
Driver input power	7.71W	7.25W
Electrical efficiency	58%	62%
Pulse width at 50%	2.6ns	2.5ns
Rising time at 10%-90%	1.6ns	460ps
Falling time at 90%-10%	410ps	1.2ns

Moreover, even if a pulse width of around 2.5ns is obtained for both prototypes, it can be seen that the pulse shape is slightly distorted. Falling time is slower for the current-mode prototype than for the voltage-mode prototype while it is the opposite for the rising time, confirming simulation results. This is due to parasitic elements and mainly parasitic inductances. In addition, a very short secondary laser pulse occurs when the pulse is cut off for the voltage-mode driver. It might be caused by the strong voltage ringing at the switching node during transient which faded sufficiently to let a reactivation of the laser diode. A slight overshoot is also noticed on the laser signal when the pulse is turning on in the current-mode driver. This might be caused by the strong voltage ringing at the switching node.

For 2.5W peak optical power, it has been evaluated a 62% and 58% electrical efficiency for the current-mode and voltage-mode driver prototypes respectively. It suggests that the current-mode driver in shunt configuration could be more efficient than the voltage-mode driver in series configuration in the proposed measurement conditions. However, no strict conclusion can be safely drawn as some issues have to be solved, such as EMI issues.

7. Future Works and Conclusion

Two integrated laser diode driver prototypes based on different driver topologies have been developed and implemented on-chip using a 130nm CMOS technology. A test bench has been set up for performing electrical and optical measurements. It has been shown that both drivers are capable of generating laser pulses for a 2.5W peak optical power with a 2.5ns pulse width at 200MHz under typical conditions (3.6V input voltage, 25°C room temperature). In these conditions, a relatively high efficiency is noticed which is quite satisfying in the context of mobile applications. Unfortunately it may not be compared to the state-of-art circuits as efficiency values are rarely mentioned. Indeed, they are mostly

intended for LiDAR applications where constraints in term of power losses are more flexible than for mobile applications.

However, experimental results do not fully demonstrate the feasibility of integrating these kinds of driver architecture on a single chip taking into account mobile phone constraints. Further investigations are required, such as investigating EMI issues and performing more measurements while sweeping a wide range of parameters (frequency, peak optical power, input voltage, temperature) to get exhaustive results. This calls for additional PCBs and a second set of IC prototypes. The experimental setup could be consolidated as well to ease the measurement procedure and improve accuracy wherever it is possible. Validating the IC prototypes at system level by considering a typical Time-of-Flight application is also essential in order to demonstrate optical performances of the two different driver topologies.

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The authors also invite to review the role of scientific researchers and engineers by fully re-considering environmental, social and ethical requirements in the development of a concept, a product or a service.

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