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A Flexible Low-Cost Discrete-Time Wake-up Receiver for LoRaWAN applications

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Abstract—This paper presents the design of an innovative discrete-time (DT) wake-up receiver (WuRx) for short-range wireless sensor networks. A switched-capacitor architecture was adopted to implement a digital filter providing some adjustment of the receiver parameters. The inherent aliasing susceptibility of the digital filter is opposed by the current sampler structure as it performs an anti-aliasing function at the input without the typical external bandpass filter solution. The circuit designed for on-off keying (OOK) modulation at 900 MHz and a data rate of 100 kbps is implemented in 180 nm CMOS. Extracted post-layout simulation results show a sensitivity of -70 dBm and current consumption of 27.7 μ A from a 1.2 V supply.

Index Terms—Wake-up Receiver, Discrete-time filter, wireless sensor network.

I. INTRODUCTION

Battery-powered devices in wireless sensor network applications offer flexibility and a ready-to-use deployment option. However, the cost of battery replacements could hinder the operation itself [1]. The LoRaWAN protocol is designed to solve this power issue by extending the battery lifetime through a highly efficient use of the radio hardware.

LoRaWAN devices feature power management modules with different operation modes: receiver mode (30 mA), standby mode (1.6 mA), and deep-sleep mode (less 10 μ A) [2]. The power consumption reduction comes from an intermittent use of the receiver hardware, this method have good results when the communication is started by the end device. Nevertheless, messages sent by the base station to the end device requires a radio front end being responsive all the time [3]. Thus, one may find advantageous to have two RF receivers: (a) the main receiver module with high performance, and (b) an auxiliary low-power receiver unit. The main receiver should be activated only for short periods to execute the data communication, while the auxiliary one is always actively waiting for an ambient event to occur. The latter receiver is commonly referred as a wake-up receiver (WuRx).

Recently, mobile radios have been exploring discrete time (DT) architectures as an alternative to a continuous time. This strategy provides scalability and programmability as its operation is based on the relation between capacitors and the sampling frequency. These parameters can be precisely defined and have low variability against process mismatch [4], [5].

This paper explores the DT signal processing to implement a 900 MHz low power WuRx, for an event-driven 100 kHz bandwidth radio signal, targeting LoRaWAN communication. The proposed DT-WuRx uses a current sampling and a passive charge-sharing filter stages, designed using a system-level approach in 180 nm TSMC technology. Post-layout simulation results are presented as Monte Carlo analysis to validate the proposal at 33.33 μ W of power consumption and a sensitivity of -70 dBm.

The paper is organized as follows. Section II covers the entire architecture of the system and the discrete-time concepts involved. The design concerns are analyzed and post layout simulation results are shown in Sec. III. Finally, conclusions are drawn.

II. PROPOSED DT-WURX ARCHITECTURE

The WuRx system proposed here use of an unconventional architecture, illustrated in Fig. 1, which is based on DT signal processing. External events are detected in this proposal through a DT mixer (energy detection) and filtering. This strategy guarantees strong attenuation of specific frequencies and is notably useful to reduce the effect of the harmonic folding in the frequency mixing process [6]. The DT-WuRx circuit described in this section uses a current sampling and a passive charge-sharing filter stages. The system architecture is detailed in the following subsections.

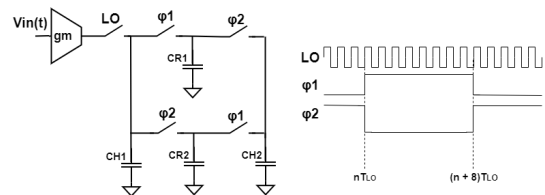


Fig. 1. Discrete-time passive mixer and filters.

A. Windowed Integrated Sampler

While the voltage sampler requires external protection from aliasing issues, the current sampler presents an intrinsic alias attenuation sinc transfer function [6]. The charge $q_{in}[n]$ accumulated over the capacitor C_{H1} (charge packet) corresponds to the integration of the transconductor output current over

the sampling period $T_s (= T_{LO}/2)$. This arrangement, named Windowed Integrated Sampler (WIS), is defined as

$$q_{in}[n] = \int_0^{T_s} g_m \cdot V_{in}(t) dt. \quad (1)$$

Evaluating the voltage integrated over C_{H1} in Fig.1 as $V_c = \frac{q_{in}[n]}{C_{H1} + C_R}$ with respect to the input voltage, the frequency response of the WIS operation can be derived as

$$H_{WIS}(f) = \frac{g_m \cdot T_s}{C_R + C_H} \cdot \frac{\sin(\pi \cdot f \cdot T_s)}{\pi \cdot f \cdot T_s}, \quad (2)$$

which corresponds to a sinc function with notch attenuation at the even harmonics of the LO frequency, which is typical of a 50% duty-cycle mixer. Figure 2 illustrates the notch attenuation behavior of this sinc filter in dash-dotted red line. In addition to the continuous-time sinc function, the circuit illustrated in Fig. 1 also implements a Finite Impulse Response (FIR) and an Infinite Impulse Response (IIR) filter, described in the following subsections.

B. FIR Filter

The FIR filter is implemented by the accumulation of N charge packets over C_{H1} . This effect is defined by the clock decimation between the sampling frequency $f_s = 2 \times LO$ and the filter clock frequency ϕ_1 , as shown in Fig. 1.

The FIR transfer function depends only on the sum of input voltage samples highlighted in the z-domain, as

$$\frac{V_{out}}{V_{in}} = N \cdot \left(\frac{1 - z^{-N}}{1 - z^{-1}} \right). \quad (3)$$

For simplicity, the circuit analysis only considers the top branch of the circuit in Fig. 1; complete analysis is obtained using circuit symmetry. The charge packets are assumed to be shared evenly by the capacitors [4]. The frequency response of the FIR filter is illustrated by the dotted blue line in Fig. 2.

C. IIR Filter

In Fig. 1, the signal ϕ_2 controls the discharge of the rotating capacitor C_{R1} into the second history capacitor C_{H2} . This operation transfers the charges throughout the circuit inducing feedback. The charge sharing is stored at a previous sample in C_{R1} with a current sampled from C_{H1} . This event can be expressed as a sum of charge packets over time as

$$\begin{cases} V_{out}[n] = (1 - \alpha_1) \cdot V_1[n - 1] \\ V_1[n] = \alpha_1 \cdot V_1[n - 1] + V_{in}[n] \end{cases}, \quad (4)$$

where $\alpha_1 = C_{H1}/(C_{H1} + C_R)$; V_{in} is the voltage accumulated on the capacitor C_{H1} ; V_1 is the voltage at C_R ; V_{out} is the voltage on the capacitor C_{H2} (see Fig. 1 for details). The union of the branches will present a $\alpha_2 \cdot (1 + z^{-1})$ feature to V_{out} , where $\alpha_2 = C_{H2}/(C_{H2} + C_R)$. Similarly to the FIR filter, this time-domain expression can be rearranged into z-domain as

$$\frac{V_{out}}{V_{in}} = \alpha_2 \cdot \left(\frac{(1 - \alpha_1) \cdot z^{-1}}{1 - \alpha_1 \cdot z^{-1}} \cdot (1 + z^{-1}) \right). \quad (5)$$

The transfer function of the IIR filter is illustrated by the dashed green line in Fig. 2 as the DT filter. As a discrete-time filter, the filter shape repeats itself on f_s/N multiple frequencies.

D. DT-WuRx Architecture

Figure 2 illustrates the frequency response for the DT-WuRx considering an LO in 900 MHz ($f_s = 1.8$ GHz) and $N = 8$ in continuous black line. One may observe that the IIR peaks (in dashed green line) at f_s/N multiples are mitigated by the notches in the FIR response. The same occurs with the FIR peaks (in dotted blue line) at f_s multiples and the notches from WIS filter (in dotted-dash red line). As all the filter contributions are constructive at zero frequency. Thus, the combined response represents a low-pass filter with higher selectivity than separated filters.

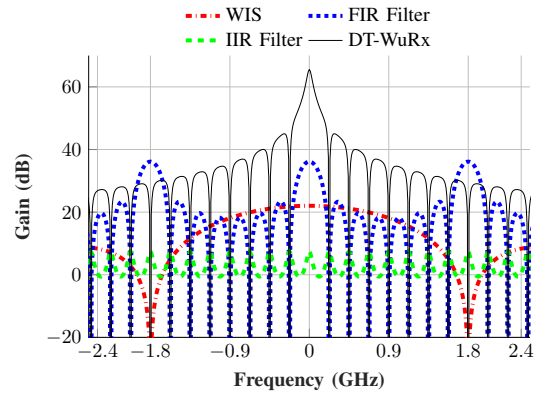


Fig. 2. Frequency response of DT-WuRx filtering scheme.

III. DT-WURX CIRCUIT DESIGN

The proposed DT-WuRx focus on 900 MHz, low power, for 100 kHz bandwidth LoRaWAN applications. The design presented in Fig. 3 relies on the use of digital blocks in the aligner and frequency divider to reduce the static power. This transconductor targets a -70 dBm sensitivity followed by a DT mixer filtering. An integrated impedance matching network and a base-band amplifier completes the DT-WuRx implementation aiming a power consumption below $40 \mu W$.

The DT-WuRx has a trade-off between power consumption and input signal sensitivity. The minimum detectable signal, also referred as the receptor sensitivity is defined by

$$MDS = KTB + NF + SNR_{min}, \quad (6)$$

where NF is the noise figure of the circuit in dB; KTB is the total thermal noise power over the bandwidth; SNR_{min} is the minimum signal-to-noise ratio required by the OOK modulation. For LoRaWAN applications, the OOK modulation with $SNR_{min} = -12$ dB, and the ambient noise at room temperature equal to -174 dBm/Hz are considered [7]. Thus, the sensitivity is defined mainly by the noise figure, which must be better than 50 dB.

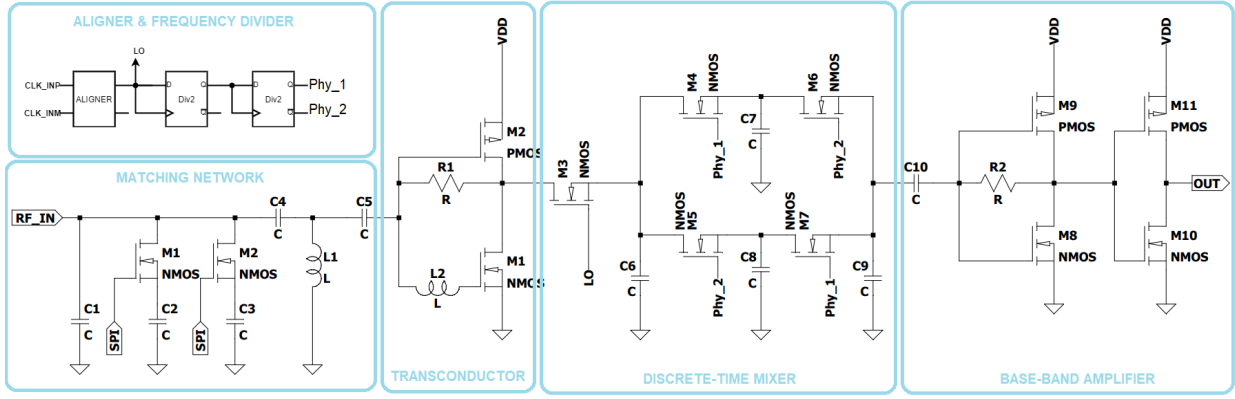


Fig. 3. DT-WuRx transistor-level and block diagram.

As demonstrated by [7], the noise factor for a DT circuit is dominated by the noise density which the mixer inserts in the signal, the total thermal noise $V_{N,in}^2$, and the DT-WuRx gain A_v , as

$$N = \frac{1}{A_v^2} \cdot \frac{V_{N,in}^2}{4kTR_s}. \quad (7)$$

The total thermal noise

$$\overline{V_{N,in}^2} = 2m kT R_{ON} + \frac{(1-m)^2 kT}{f_s C_R} \quad (8)$$

is composed by the noise through the switch during the ON phase and the noise stored in the capacitor during the OFF phase [5].

In (8), the A_v is indeed the combination of voltage gain and filtering illustrated by the continuous black line in Fig. 2. The m is the duty cycle. The $4KT$ is the thermal coefficient. The equivalent resistance, R_s for a similar sampling circuit is presented in [6] as $R_s = 1/(f_{s2} C_{H2})$. Similarly, the work [5] expresses the switch resistance as $R_{ON} = 1/(f_{s2} C_R)$.

The decimation frequency f_{s2} is defined as $f_s/8$ aiming power reduction. The capacitors were designed as $C_{H1} = 800$ fF, $C_R = 100$ fF and $C_{H2} = 100$ fF with the objective of better combine the current sampler, FIR and IIR filter responses. The capacitors were selected based on the reduction of harmonics in a PXF simulation on Virtuoso Spectre Simulator. All the transistors in the circuit were designed with reduced size, $W/L = 1 \mu\text{m}/180$ nm to reduce power consumption and charge-injection phenomenon, since the transistors size impacts directly on the power consumption of the clock generation block [5].

The system is completed, as shown in Fig. 3, by (a) a base-band amplifier, (b) a clock generation (frequency dividers) and (c) a on-chip matching network with configurable capacitor bank. The clock aligner circuitry included in (b) is based on the architecture proposed in [5], while [8] presents the basic structure of the designed divider by 2.

The circuit is implemented in TSMC 180 nm and its extracted layout having an area of $468.92 \times 306.2 \mu\text{m}^2$ is illustrated in Fig. 4 post-layout simulated (PLS) in Virtuoso Spectre. The transient simulation with a 900 MHz input sine

wave, modulated by 100 kHz OOK signal and -70 dBm of input power is presented in Fig. 5.

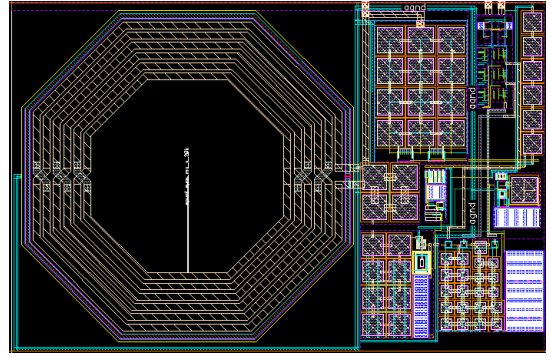


Fig. 4. DT-WuRx layout illustration, with an area of $468.92 \times 306.2 \mu\text{m}^2$.

The power consumption is evaluated for PLS DT-WuRx as $33.33 \mu\text{W}$. The passive mixer circuit itself has a zero power consumption since this block does not have DC supply. The power consumed by the switches in the mixer is accounted for in other blocks, namely the frequency divider and the clock buffer being 56.28% and 23.76% of the total consumption, respectively. The receiver amplification has a cost of 20% of the total consumption, being the transconductor at 4% and the Base-band amplifier at 16%.

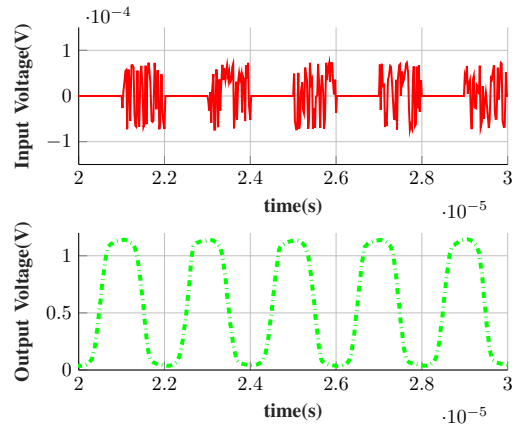


Fig. 5. OOK modulation and circuit response.

The DT-WuRx sensitivity is evaluated from the receiver noise figure. The noise analysis is obtained through a PNOISE simulation for an input-power sweep PSS in Virtuoso Spectre. Figure 6(a) compares the input signal power minus the SNR_{min} , in continuous red line, with the total noise $KTB+NF$, in dash-dotted blue line, present at the input port. The sensitivity of -70 dBm is estimated at the intersection of both lines. The DT-WuRx small-signal gain is obtained through a PAC for a fixed -20 dBm input-power PSS in Virtuoso Spectre. Thus, the signals that are downconverted to 100 kHz which is the message information in base band. The test setup is configured to have a LO signal at 900 MHz. The resulting spectrum in Fig. 6(b) shows the filtering properties of the circuit. The in-band gain is 70 dB. The harmonics suffer a very aggressive attenuation at the notch frequencies which will be folded to the base band during the mixing and DT signal processing. A minimum of 140 dB rejection is obtained.

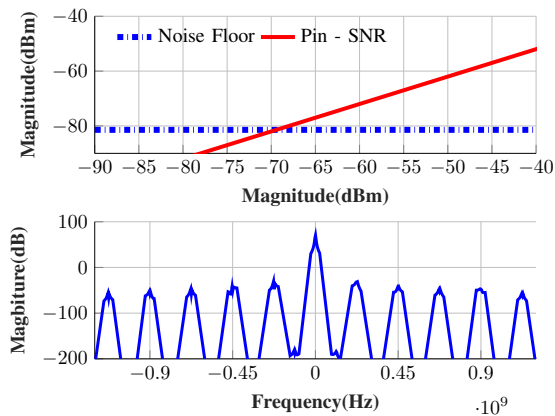


Fig. 6. DT-WuRx (a) Sensitivity and (b) small-signal gain.

To guarantee the DT-WuRx yield against process variability, the gain and the NF are assessed to process variations of 3σ . A Monte Carlo simulation was performed for 200 samples, and it is illustrated in Fig. 7. One may observe that the mode of both characteristics are consistent with typical analysis besides process variation.

Table I compares the performance of the proposal with state-of-the-art of WuRx. It should be noted that some of the works presented in the table adopt input MEMS filter (subscript \diamond in Tab. I), while the others use envelope detection (subscript \dagger in Tab. I).

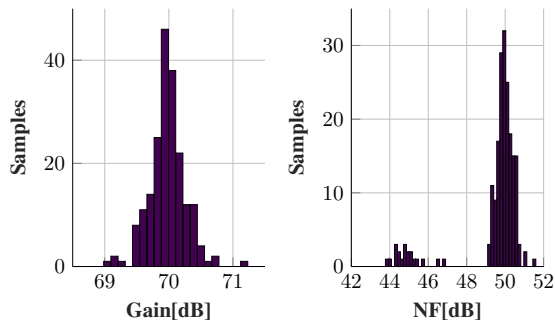


Fig. 7. PLS Monte Carlo analysis for the gain and the NF .

TABLE I
WAKE-UP RECEIVER PERFORMANCE COMPARISON.

	Tech [nm]	Voltage [V]	Freq. [MHz]	Data Rate [Kbps]	Sens. [dBm]	Power [μ W]
This Work	180	1.2	900	100	-70	33.3
[7] [†]	130	1.2	915	200	-60	2.4
[9] [†]	180	0.45	402	50	-55	129
[10]	130	1.2	902	200	-75	22.9
[11] [†]	90	2	2400	1000	-58	164
[12] [◊]	65	1	400	100	-47	0.018

[†] Envelop Detector; [◊] MEMS filter

IV. CONCLUSION

In this work, a novel wake-up receiver based on discrete-time filters is proposed. The circuit implementation for a 180nm CMOS process was described in a system-level approach. The results show that the DT signal processing significantly reduces the requirements for external band-pass filter. The proposed circuit presents a flexible architecture for a low-cost CMOS technology node that achieves a sensitivity of -70 dBm with 33.3μ W of power consumption. Obtained performance is comparable to recent designs in the literature.

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