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mm-Wave Through-Load Element for on-wafer Measurement Applications

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Abstract—This paper presents an innovative Through-Load element aimed at characterization applications at mm-wave frequencies. The proposed structure can behave as a Through connection or as a 50-Ω load depending on a DC control voltage. Among other potential applications, this system can be used to implement a transfer switch or an attenuator. A demonstrator was fabricated and measured in the STM 55-nm BiCMOS technology. Over a wide bandwidth, from 55 GHz up to 170 GHz, experimental measurements demonstrate a maximum 1.6-dB of insertion loss when behaving as a Through connection and a minimum 14-dB of insertion loss when behaving as a 50-Ω load. In both cases, the return loss is better than 10 dB. The insertion loss at 90 GHz is 0.6 dB for the Through connection and 20 dB for the 50-Ω load connection.

Index Terms—Through-Load, on-wafer, 3-dB Coupler, Slow-wave, BiCMOS, attenuator, transfer-switch millimeter-wave.

I. INTRODUCTION

MODERN BiCMOS technologies enable the integration of high-performance circuits and systems operating at millimeter-wave (mm-wave) frequencies (that is, in the range 30-300 GHz) at a moderate-to-low cost. Indeed, modern SiGe BiCMOS technologies feature transistors whose f_T or f_{MAX} is beyond the mm-Wave band [1]. In this scenario, these technologies appear as a suitable candidate for high-volume production of transceivers operating in this frequency band. As a matter of fact, in the last few years, pushing circuit operation to mm-wave frequencies has been the object of an ever-increasing interest from the academic and industrial communities. Among other application scenarios, the higher frequencies available in the mm-wave band allow to obtain faster data-rates and higher bandwidth in communication applications or higher spatial resolution in radar applications.

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The faster data rate is a key parameter for enabling current and future communication standards, while radar resolution has become a key issue in the context of autonomous vehicles and advanced imaging applications.

However, pushing operation to such a high frequency range makes the characterization and test of these devices and systems a challenging task that may compromise their development. In general, a mm-wave device, as any other RF device, is characterized in terms of a number of functional performance parameters that are measured at the operation frequency (or frequency range) using dedicated high-frequency test equipment. Test setups may vary depending on the particular device under test and performance figures to extract, but they are typically based on the use of high-frequency Vector Network Analyzers (VNA). A VNA is a versatile test instrument that measures the input/output power ratios on a given Device Under Test (DUT) for determining the scattering parameters (S-Parameters) of the DUT.

However, as frequency increases, the impact of parasitics in the measurement setups may complicate significantly these characterization measurements. Thus, the effect of parasitics in calibration standards, traditionally used for VNA calibration, may lead to significantly greater measurement uncertainties [2]. Moreover, some measurements may turn impossible to perform as the losses between the measurement system and the on-wafer pads may significantly reduce the measurable range of the test instruments. For instance, load-pull measurements, devised to assess the optimum output impedance of a transistor for maximum power output [3], may require to present reflection coefficients at the output of the transistor with magnitudes close to unity. Hence, the losses in the interconnections between the external load-pull setup and the actual on-wafer DUT greatly reduce the range of impedances that are synthesized at the input of the DUT. A similar logic can be applied to power measurements, for whom the losses between the DUT and the

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detection system may place the output power level below the detectable threshold of the power detector.

In this context, moving the measurement system on chip may overcome some of the current limitations of mm-wave measurements. In this line, several works have reported on-wafer (on-silicon) solutions for different measurement systems [4]–[6], such as power detection, load-pulling schemes or even S-Parameters measurement. Nevertheless, the proposed on-wafer instruments, although being the subject of major research efforts nowadays, are far from achieving the wideband versatility and precision of external measurement instruments. For this purpose, wideband high-performance on-wafer building blocks have to be devised.

In this work, we propose an innovative element that may simplify the implementation of on-chip characterization and test instrumentation at mm-wave frequencies. The proposed element is a two-port device that can act as: (i) a Through connection, or, (ii) a 50- Ω load connected to each port, as a function of a DC control signal. As it will be presented later in this paper, this device might open the door to a full range of applications. Indeed, such a system may be very useful in the design of transfer switches or even attenuators, as discussed at the end of this paper. Hence, the aim of this work is not only to propose a Through-Load system, but also to present a wideband system performing this function. The proposed through-load element was first presented by the authors in [7] and validated using electromagnetic and transistor-level simulations. The present work presents an in-depth analysis of the principles of operation of the proposed element, details the design of a proof-of-concept prototype with a central frequency of 120 GHz and demonstrates the feasibility and performance of the Through-Load element with measurements results on a fabricated prototype.

The results reported hereby open the door to enhance the measurement capabilities of on-wafer instruments (for instance for the implementation of a Through-Load element in an integrated VNA), although the proposed architecture could be also used in external instruments without loss of generality. In this paper we focus our analysis on two main target applications: (i) the implementation of a transfer switch, and (ii) the implementation of an attenuator. Nevertheless, the proposed element may be useful in a wide variety of applications, especially in the fields of precise high-frequency instrumentation and Built-In Self-Test (BIST).

The rest of this paper is organized as follows: section II presents the proposed architecture and describes its working principle through a detailed analytical study. Next, section III describes the design procedure and measurement results of a demonstrator in the STM 55-nm BiCMOS technology. Section IV discusses the main applications of the proposed architecture. Finally, section V summarizes the main conclusions of this work.

II. PROPOSED THROUGH-LOAD ELEMENT

The functionality of the proposed Through-Load Element is based on the combination of two main devices: (i) a 3-dB coupler, and (ii) two n-type Metal-Oxide-Semiconductor

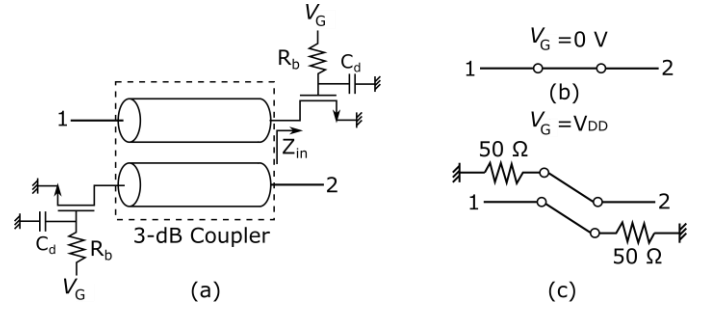


Fig. 1. (a) Schematic view of the Through-Load element. The nMOS transistors are connected to the coupled ports of the 3-dB coupler. (b) Function of the proposed device when $V_G = 0$ V. (c) Function of the proposed device when $V_G = V_{DD}$.

(nMOS) transistors in a common-source configuration, as shown in Fig. 1(a). A biasing control voltage V_G applied to the gate of the transistors allows changing the states of the Through-Load element. The system is devised in such a way that when V_G is equal to 0 V, the transistors are in the cutoff state and the system behaves as a through connection, as depicted in Fig. 1(b). Conversely, when the transistors are biased at $V_G = V_{DD}$, i.e., in their conductance region, the system behaves as a single-ended 50- Ω resistance connected to ports 1 and 2, as shown in Fig. 1(c).

In the following subsections we detail how this behavior can be achieved using traditional n-type MOS Field-Effect Transistors (MOSFET) and 3-dB couplers. Moreover, we develop analytical design guidelines that take into account the effect of the coupler and transistors main non-idealities on the performance of the Through-Load element.

A. Through-Load Element operation principle

In this section the working principle of the proposed architecture is described. As introduced previously, the aim is to propose a wideband system. Hence, a frequency-dependent analysis must be carried out.

Let us consider an ideal 3-dB coupler integrated using the coupled-line architecture and loaded at its coupled outputs (i.e., ports II and III) by an impedance Z_{load} , as shown in Fig. 2. The choice of this architecture will be subsequently justified later in this section. Let us begin by considering the S-Parameter matrix of the coupler. When matched at the reference impedance, Z_0 , we can write,

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} 0 & S_{II,I} & S_{III,I} & 0 \\ S_{II,I} & 0 & 0 & S_{III,I} \\ S_{III,I} & 0 & 0 & S_{II,I} \\ 0 & S_{III,I} & S_{II,I} & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}. \quad (1)$$

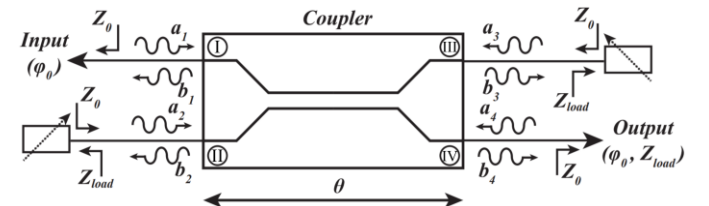


Fig. 2. Ideal 3-dB coupler loaded by Z_{load} impedances.

Where a_i and b_i represent the incident and reflected power waves at the coupler ports, as represented in Fig. 2, and S_{ij} represent the S-Parameters of the coupler. In the case of a perfectly matched coupler, a_4 presents a null value. Hence,

$$\begin{cases} b_1 = S_{II,I} \cdot a_2 + S_{III,I} \cdot a_3 \\ b_2 = S_{II,I} \cdot a_1 \\ b_3 = S_{III,I} \cdot a_1 \\ b_4 = S_{III,I} \cdot a_2 + S_{II,I} \cdot a_3 \end{cases} \quad (2)$$

Now, let us consider the reflection coefficient at the interface between the loads and the coupler (i.e., ports II and III). This reflection coefficient Γ_L can be written as,

$$\Gamma_L = \frac{Z_{load} - Z_0}{Z_{load} + Z_0} \quad (3)$$

Hence,

$$a_2 = \Gamma_L \cdot b_2, \quad (4)$$

and,

$$a_3 = \Gamma_L \cdot b_3. \quad (5)$$

Then, a_2 and a_3 in (2) can be substituted by (4) and (5), leading to:

$$\begin{cases} b_1 = S_{II,I} \cdot \Gamma_L \cdot b_2 + S_{III,I} \cdot \Gamma_L \cdot b_3 \\ b_2 = S_{II,I} \cdot a_1 \\ b_3 = S_{III,I} \cdot a_1 \\ b_4 = S_{III,I} \cdot \Gamma_L \cdot b_2 + S_{II,I} \cdot \Gamma_L \cdot b_3 \end{cases} \quad (6)$$

Substituting the expressions of b_2 and b_3 in (6) into the expressions of b_1 and b_4 in (6) yields,

$$b_1 = \Gamma_L (S_{II,I}^2 + S_{III,I}^2) a_1, \quad (7)$$

and

$$b_4 = 2\Gamma_L \cdot S_{II,I} \cdot S_{III,I} \cdot a_1, \quad (8)$$

Hence, S_{11} , which represents the $S_{I,I}$ of a coupler loaded by Z_{load} , can be expressed as,

$$S_{11} = \frac{b_1}{a_1} = \Gamma_L (S_{II,I}^2 + S_{III,I}^2), \quad (9)$$

and S_{21} , which represents the $S_{IV,I}$ of a coupler loaded by Z_{load} , as,

$$S_{21} = \frac{b_4}{a_1} = 2\Gamma_L \cdot S_{II,I} \cdot S_{III,I}. \quad (10)$$

It can be demonstrated [8] that $S_{II,I}$ in a lossless, perfectly-matched coupler can be expressed as,

$$S_{II,I} = \frac{jk \sin \theta}{\sqrt{1 - k^2} \cos \theta + j \sin \theta} \quad (11)$$

where θ represents the electrical length of the coupler and k the coupling coefficient. On the other hand, the expression of $S_{III,I}$, in a coupler under these considerations, can be demonstrated to be:

$$S_{III,I} = \frac{\sqrt{1 - k^2}}{\sqrt{1 - k^2} \cos \theta + j \sin \theta} \quad (12)$$

As the coupler is considered to present a 3-dB coupling, then $k = 1/\sqrt{2}$.

Under these considerations, at the frequency for which the coupler presents $\theta = \pi/2$ radians (i.e., the central frequency of the coupler) S_{11} is null and $S_{21} = -j \cdot \Gamma_L$. Note that this behavior, when $\theta = \pi/2$, would also hold for a branchline coupler.

Next, let us analyze the expressions in (9) and (10), as a function of θ and $|\Gamma_L|$. Note that the analysis over different values of θ is equivalent to a frequency analysis. Thus, Fig. 3 shows the S_{11} magnitude for different coupler electrical lengths (X-axis) and different load reflection coefficients (Y-axis). It can be observed that such a structure is matched to Z_0 over a wide range of frequencies for any value of Γ_L . In addition, an ideal 3-dB coupler under this configuration would be matched to Z_0 when $\Gamma_L = 0$ (i.e., $Z_{load} = Z_0$) at any frequency, which is obviously an expected result.

On the other hand, Fig. 4 displays the magnitude of S_{21} as a function of coupler electrical lengths (X-axis) and different load reflection coefficients (Y-axis). Similar conclusions can be derived. Firstly, the proposed system shows similar performance over a wide band. In addition, when $|\Gamma_L| = 0$, the system shows an infinite insertion loss (i.e., $|S_{21}| = 0$), which is also an expected result since the coupled-line coupler type is backward.

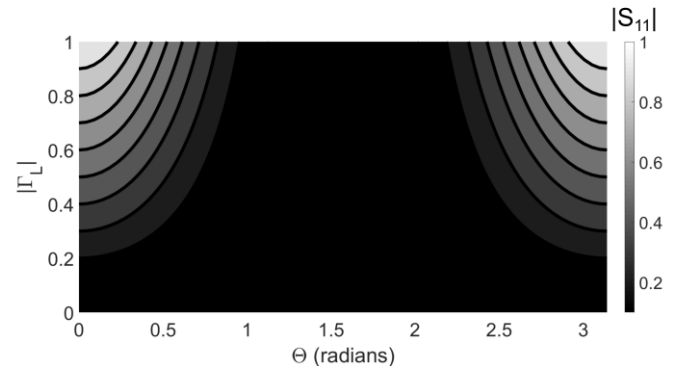


Fig. 3. $|S_{11}|$ of an ideal 3-dB coupler loaded by Z_{load} impedances as a function of θ and $|\Gamma_L|$.

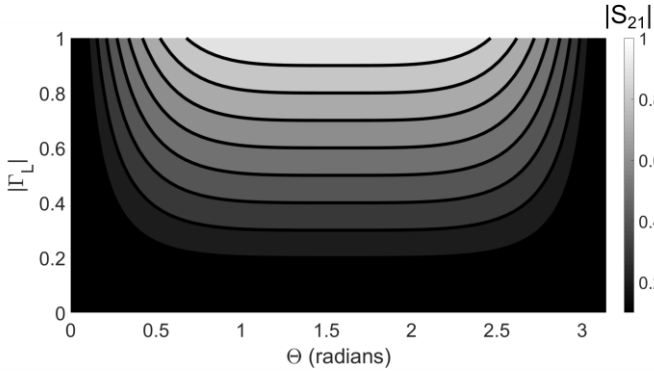


Fig. 4. $|S_{21}|$ of an ideal 3-dB coupler loaded by Z_{load} impedances as a function of θ and $|\Gamma_L|$.

Using these results, it can be concluded that if we consider a load presenting two programmable states with a unitary and a null reflection coefficient $|\Gamma_L|$, the system behaves as a Through connection over a wide band of frequencies when $|\Gamma_L| = 1$ and as a Z_0 load, at both ports of the system, when $|\Gamma_L| = 0$ for any frequency.

If Z_0 is considered to be purely real, $|\Gamma_L|$ presents a null magnitude for $Z_L = Z_0$. On the other hand $|\Gamma_L| = 1$ when

$$\begin{cases} \Re(Z_{load}) = 0 \\ \Re(Z_{load}) = \infty \end{cases} \quad \forall \Im(Z_{load}) \quad (13)$$

Summarizing, the dual behavior of the system (i.e., Through and Load) can be achieved with a load presenting either a real part of its impedance equal to zero or to infinity for obtaining the Through state and a $Z_L = Z_0$ for the Load state.

For the sake of simplicity, Z_0 is considered to be 50Ω for the rest of this paper, as it is the reference impedance in most systems.

B. 3-dB Coupler

Generally speaking, there are two widely employed design styles for the implementation of mm-Wave integrated 3-dB couplers: (i) the branchline coupler [9], and (ii) the coupled-line coupler [8], shown in Fig. 5(a) and Fig. 5(b), respectively.

The branchline couplers can be integrated in a conventional integrated technology with relative ease. However, they show reduced bandwidth performance, as compared to their coupled-lines counterparts. To illustrate this issue, let us consider two ideal $50\text{-}\Omega$ 3-dB couplers, with central frequencies of 100 GHz, one designed using a branchline coupler architecture and

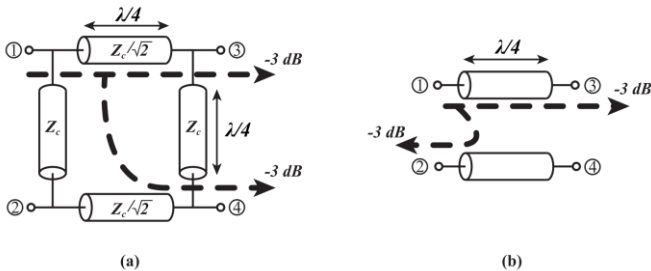


Fig. 5. Schematic view of (a) a branchline coupler and, (b) a coupled-line coupler.

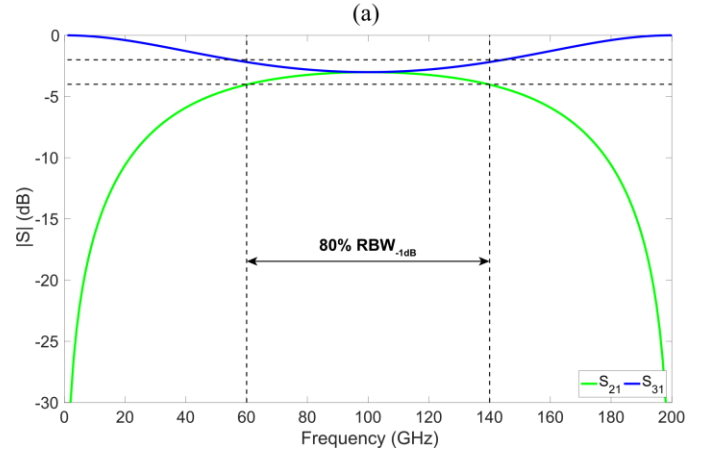
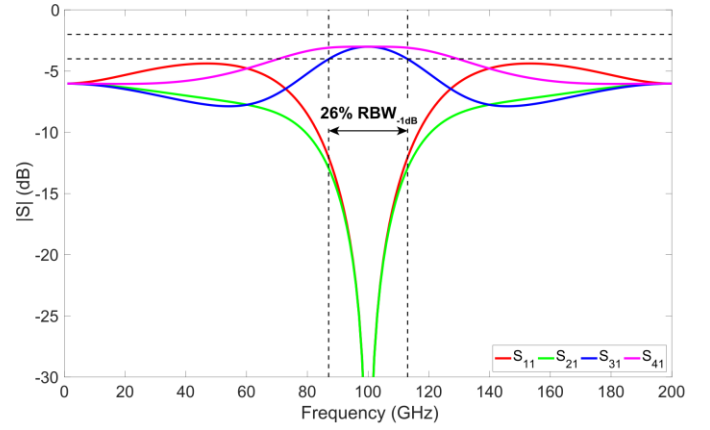


Fig. 6. S-Parameter magnitude of an ideal 3-dB (a) branchline coupler, and (b) coupled-line coupler.

another designed using coupled lines. Under these considerations, and using a classical architecture, the branchline coupler is composed of four quarter-wavelength transmission lines. If a $50\text{-}\Omega$ 3-dB coupler is considered, two of these transmission lines present a characteristic impedance of 50Ω while the other pair present a characteristic impedance of $50/\sqrt{2} \Omega$. On the other hand, the coupled-line coupler is composed of two quarter-wavelength coupled transmission lines whose even- and odd-mode impedances can be derived from

$$\begin{cases} Z_{C,e} = Z_C \cdot \sqrt{\frac{1+k}{1-k}} \\ Z_{C,o} = Z_C \cdot \sqrt{\frac{1-k}{1+k}} \end{cases} \quad (14)$$

as a function of the coupling coefficient, k (i.e., $1/\sqrt{2}$ in the case of a 3-dB coupling). Hence, a $50\text{-}\Omega$ 3-dB coupler requires a $Z_{C,e}$ and $Z_{C,o}$ of approximately 120 and 20Ω , respectively.

Fig. 6(a) and Fig. 6(b) display the S-Parameters magnitude of the ideal 3-dB couplers designed with branchline or coupled-line architectures, respectively. Note that if a ± 1 dB bandwidth (BW) is defined in the transmission S-parameters, that is S_{31}

and S_{41} for the branchline coupler, and S_{31} and S_{21} for the coupled-line coupler, respectively, the branchline coupler presents a 26% of Relative BW (RBW), while the coupled-line coupler shows a RBW of 80%. In addition, the branchline coupler presents high isolation and return loss only for a narrow band of frequencies. On the other hand, an ideal coupled-line coupler shows infinite isolation and matching at any frequency (i.e., infinite BW), and hence not shown in Fig. 6(b). The superiority of the coupled-line coupler can also be observed in terms of its phase shift. If a $\pm 5^\circ$ BW is defined on the phase difference between the coupled and through ports of the coupler, expected to be 90° , (i.e., $\angle S_{31} - \angle S_{41}$ for the branchline coupler, and $\angle S_{31} - \angle S_{21}$, for the coupled-lines coupler), the branchline coupler presents a 34% RBW, while the coupled-lines coupler presents an infinite BW.

Despite the superior performance of a coupled-line coupler over a branchline coupler, especially when aiming at large bandwidths, their integration in modern silicon technologies remains an issue when using classical transmission line architectures (that is microstrip lines or CoPlanar Waveguides, CPW). The main reasons for this difficulty lay on the stringent design rules of advanced integrated technologies (that usually prohibit approaching metals below a certain threshold) and the inhomogeneity of the medium where the electromagnetic (EM) wave propagates. These issues result in different odd- and even-mode phase velocities, and hence in a degraded performance of the designed 3-dB couplers, especially in terms of isolation and bandwidth [9].

Several techniques and architectures of coupled-line couplers using microstrip technology have been reported on the literature [10]–[13]. However, many of these techniques [10], [11], [13] rely on the use of the so-called coupled microstrip lines in a broadside configuration to achieve the necessary coupling.

This architecture, asymmetrical by nature, together with the inhomogeneity of the BEOL (i.e., different $\epsilon_{r,eff}$ for different BEOL layers) leads to poor directivity and narrow bandwidths. In this scenario, compensation in order to equalize the phase velocity of the even- and odd-modes is necessary to improve the performance of the coupler. For example, authors in [11] propose a lumped LC circuit to improve the behavior of the proposed coupler. With this approach, they are able to achieve isolation levels beyond 20 dB.

To overcome these challenges, the Coupled Slow-wave CPW (CS-CPW) architecture was proposed in [14]. In this article, authors presented the CS-CPW topology and gave broad design

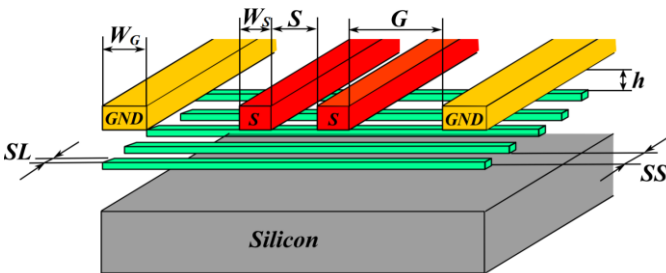


Fig. 7. Representation of the CS-CPW architecture and its geometrical magnitudes.

rules. Subsequently, an analytical parametric model was given in [15] together with the design and experimental validation of state-of-the-art mm-wave 3-dB couplers. Indeed, couplers presented in [15] reported the greatest RBW in terms of insertion loss and phase difference as well as a great isolation.

These couplers are composed of a classical coupled CPW structure where electrically floating metallic fingers (or ribbons) have been added transversally to the propagation direction below the signal and ground strips. These ribbons, in the design step, allow tuning the electrical coupling between the strips independently from the magnetic coupling coefficient. A representation of this architecture and the geometric magnitudes that define it is shown in Fig. 7. In addition, cuts can be performed at the center or sides of these ribbons, to tune the electrical coupling coefficient, adding several degrees of freedom for the designer.

Moreover, the addition of the fingers leads to a slow-wave effect (i.e., an artificial increase of the effective dielectric constant $\epsilon_{r,eff}$). The increase of $\epsilon_{r,eff}$ reduces the propagation velocity and reduces the necessary physical length to implement a given electrical length, thus leading to more compact structures [16], [17].

The design flexibility and demonstrated performance of the CS-CPW architecture make it very suitable for the proposed Through-Load element implementation.

C. Loading MOSFET design

As introduced above, to obtain the desired performance, the load has to present two particular impedances as the response to a control signal. Hence, the nMOS transistor in Fig. 1(a) has to be carefully designed to present these two differentiated states.

In fact, if we consider that the control voltage is a binary digital control that switches the transistor state between the cutoff and the linear regions, two possible scenarios would be possible: (i) a transistor presenting a $50\text{-}\Omega$ resistance in its cutoff state and a null resistance when biased into its linear region or, (ii) a transistor presenting an infinite resistance in its cutoff state and a $50\text{-}\Omega$ resistance in the linear region. Even though these two options are theoretically possible, the second one is favored hereby as it leads to lower parasitic effects.

To illustrate this choice, let us qualitatively describe the requirements for an nMOS in the common-source configuration shown in Fig. 1. For the sake of simplicity, the gate length is considered as a constant parameter. In this scenario, to satisfy the first combination (i.e., $Z_{load,cut-off} = 50\ \Omega$ and $Z_{load,linear} = 0\ \Omega$) the transistor should be integrated using a very large gate, leading to high capacitive parasitics. Note that these parasitics would only affect the Load state as the Through state would only suffer from a greater phase shift due to these effects. On the other hand, if the second combination is chosen (i.e., $Z_{load,cut-off} = \infty\ \Omega$ and $Z_{load,linear} = 50\ \Omega$) the gate of the transistor can be implemented with a rather narrow width in most of the modern nanometric nodes. This approach leads to reduced parasitic and better performance of the circuit in the Load state.

The reader may note that $Z_{load} = 0\ \Omega$ and $Z_{load} = \infty\ \Omega$ were stated as possible values for the conductance and cutoff states

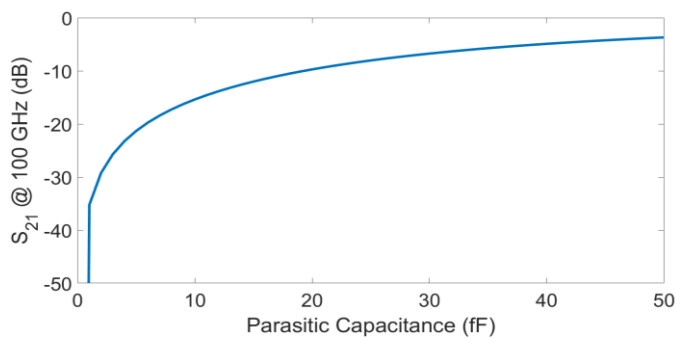


Fig. 8. Magnitude of S_{21} of the Through-Load element at 100 GHz constituted by an ideal 100-GHz 50- Ω 3-dB coupler and a MOSFET modelled by an RC network where $R = 50 \Omega$ and C is a variable.

of a transistor. Obviously, these are approximations for the ideal desired behavior of the transistor. In a practical device, neither of them represent a realistic scenario. However, these guidelines may be used by the designer in order to determine the best transistor geometry to achieve a given design goal.

On the other hand, as introduced before, it cannot be considered that a MOSFET presents a purely real impedance at its drain level. To illustrate in a simple manner the effect of the MOSFET non-idealities, specially the effect of its parasitic capacitances, let us approximate the behavior of the MOSFET in our proposed application as an equivalent parallel RC network. At the central frequency and considering the results displayed in Fig. 4, the greatest impact of the parasitic capacitance is observed for an input impedance of the loading transistor close to 50 Ω (i.e., Load state), as this capacitance increases the magnitude of Γ_L , which is meant to present a null value in this state.

Fig. 8 represents the $|S_{21}|$ of the Through-Load element in the Load state as a function of the capacitance of an RC representation of the MOSFET. The figure was obtained using an ideal 50- Ω 3-dB coupler with a central frequency of 100 GHz together with the RC representation of the MOSFET (with a resistor R of 50 Ω and a capacitance ranging from 0 to 50 fF).

Note that the isolation of the Through-Load element is strongly related to the equivalent parasitic capacitance of the MOSFET as seen between the drain and source terminals. In order to minimize this effect, the sizing of the transistor should favor smaller geometries.

III. PROOF-OF-CONCEPT PROTOTYPE DESIGN

In order to demonstrate the feasibility and the on-silicon performance of this architecture a prototype demonstrator was designed and characterized in the laboratory. The prototype was designed in the STM 55-nm BiCMOS. This technology features a Back-End-of-Line (BEOL), schematically shown in Fig. 9, very suitable for the design of high Quality-factor (Q -factor) passive devices.

The prototype was designed for wideband operation around a central frequency of 120 GHz. This frequency is placed roughly at the middle of the mm-wave band. Hence, a wideband system with this central frequency will be suitable for applications in most of the frequency band of interest.

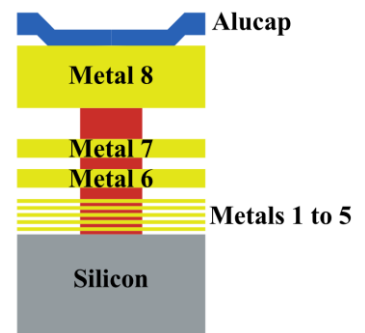


Fig. 9. Representation of the STM 55-nm BEOL.

A. 3-dB Coupler Design and Measurement Results

As introduced above, the coupler was designed using the CS-CPW architecture. For increased electrical coupling, needed to get the 3-dB coupling, cuts were performed on the sides of the floating ribbons. Firstly, this coupler was fabricated as a standalone device, to separately account for its performance in the proposed system. The fabricated coupler was designed using metals 7 and 8 for the signal and ground strips and metal 5 for the floating ribbons. The lateral dimensions were integrated using $W_S = 2 \mu\text{m}$, $S = 1.8 \mu\text{m}$, $G = 20 \mu\text{m}$, $W_G = 15 \mu\text{m}$, $SS = SL = 0.5 \mu\text{m}$, a cut on the ribbon side, CS , of 2 μm and a length of 255 μm . A microphotograph of the fabricated coupler is shown in Fig. 10.

The coupler was measured using a 4-port Anritsu VectorStar MT7838A4 VNA from 1 to 145 GHz. A first-tier line-reflect-reflect-match (LRRM) [18] was performed on an impedance standard substrate (ISS) calibrating the system up to the probe tips. Subsequently, a second-tier on-wafer multimode thru-reflect-line (TRL) calibration [19] was performed, setting the reference planes at the input of the DUT, as shown in Fig. 10.

The measurement results are shown in Fig. 11 together with 3D EM simulations up to 240 GHz obtained using the commercial software ANSYS HFSS. Measurement and simulation results show very good agreement, even though some discontinuities are observed at around 120 GHz for S_{11} and S_{41} , which appeared during the second-tier calibration. At 120 GHz, the system shows -3.7 dB at the through port (i.e.,

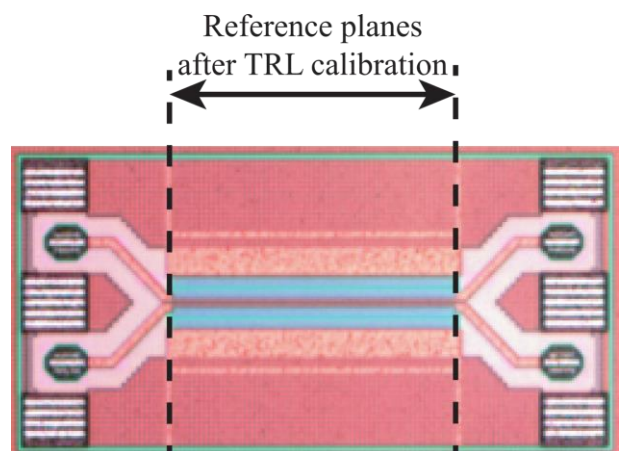


Fig. 10. Microphotograph of the fabricated 3-dB coupler and reference planes after the multimode TRL calibration.

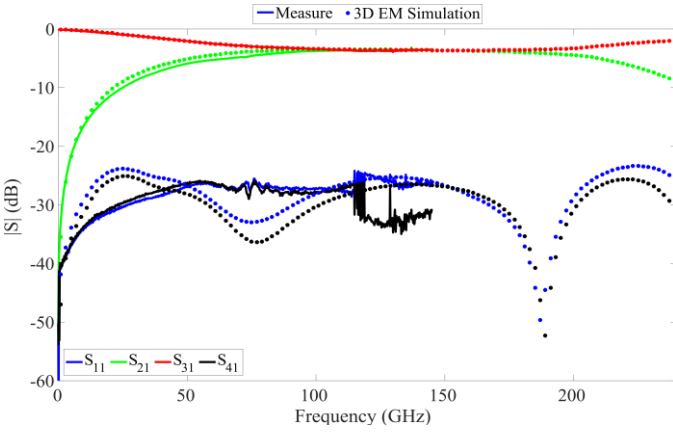


Fig. 11. Measured (solid line) and simulated (dots) S-Parameter magnitude of the 3-dB coupler.

port 3), -3.6 dB at the coupled port (i.e., port 2), and an isolation and return loss greater than 25 dB.

The other important parameter in the design of a 3-dB coupler is the phase difference between its through and coupled ports. The result of this measurement is shown in Fig. 12 for the measured and simulated data sets. Again, very good agreement is observed between simulation and measurement results. At 120 GHz, the measured coupler shows a phase difference of 94° .

Finally, thanks to the slow-wave effect, an effective permittivity $\epsilon_{r,eff}$ of 5 is achieved, leading to a 30% increase as compared to microstrip structures in the same technology, and a subsequent miniaturization effect.

These results show that the CS-CPW architecture is very suitable for the design of high-performance 3-dB couplers on integrated technologies, necessary for the proposed application. As compared to the behavior of an ideal coupler, described in section II, the measured coupler shows a similar behavior with wideband high isolation, return loss and a relatively flat phase shift between its through and coupled outputs.

B. MOSFET Design and Measurement Results

The switching element was integrated using an nMOS transistor with a width of $7.38 \mu\text{m}$, divided in three fingers, and a length of 55 nm. The transistor was sized in order to achieve a minimum $\Im(Z_{load})$ and a maximum $\Re(Z_{load})$ in the OFF-state (i.e., $V_G = 0 \text{ V}$) while achieving an $\Re(Z_{load}) \approx 50 \Omega$ and

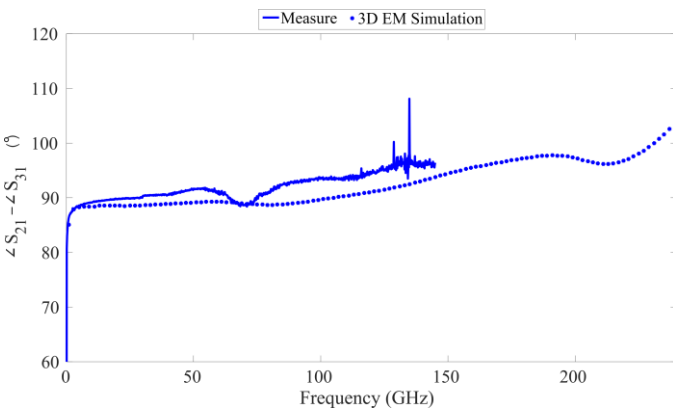


Fig. 12. Measured (solid line) and simulated (dots) phase difference between the through and coupled ports, as seen from the input for the designed 3-dB coupler.

maintaining a minimum $\Im(Z_{load})$ in the ON-state (i.e., $V_G = V_{DD}$, or 1.2 V in this technology). In addition, a high-value resistance, R_b , and a decoupling capacitance, C_d , were placed at the gate of the transistor, as shown in Fig. 1. The role of the resistance, which was integrated using a high-resistivity resistor presenting $60 \text{ k}\Omega$ of resistance, is to isolate the biasing circuitry from the RF signal. On the other hand, the capacitor was integrated using a Metal-Oxide-Metal (MOM) capacitor presenting a capacitance of 300 fF.

The proposed switching element was integrated as a standalone device for characterization purposes and measured using two different VNAs, a R&S ZVA67 with ZVA-Z110E extenders from 250 MHz to 110 GHz and a R&S ZVA27 with ZC220 extenders from 140 to 220 GHz. An on-wafer TRL calibration [20] was performed in both measurement setups, setting the reference planes at the input of the DUT. The Line standard for the lower band presented a $315 \mu\text{m}$ additional length, as compared to the Through standard (i.e., 90 degrees of electrical length at around 110 GHz). Hence, if we consider the calibration to be valid for those frequencies where the additional length of the Line is between 10 and 170 degrees, the performed calibration can be considered to be valid between around 10 and 110 GHz –and beyond, even if not used. On the other hand, the upper band was calibrated using a Line standard presenting an additional length of $150 \mu\text{m}$ (i.e., 90 degrees of electrical length at around 220 GHz), which led to an accurate calibration throughout the whole G-band (i.e., 140-220 GHz).

Fig. 13 presents the post-layout and measurement results of the $|S_{11}|$ at the input of the switching element, in the 250 MHz to 220 GHz band. Both, post-layout simulation and measurement show relatively good agreement. Some disagreement is observed in the lower part of the considered band for the ON-state, where the electrical length of the Line standard becomes increasingly small and sensitivity is lost.

Within the considered band (i.e., 10-220 GHz), measurements and post-layout simulation report an $|S_{11}|$ ranging from -50 mdB to -1.1 dB (disregarding the unphysical behavior of S_{11} occurring between 80 and 110 GHz, caused by the uncertainty of the VNA performing this measurement) for the OFF-state of the switching element. On the other hand, in this frequency range and for the ON-state, simulation reported an $|S_{11}|$ ranging from -22 to -12 dB while measurement reports -35 to -8 dB of $|S_{11}|$. Note that some disagreement is seen

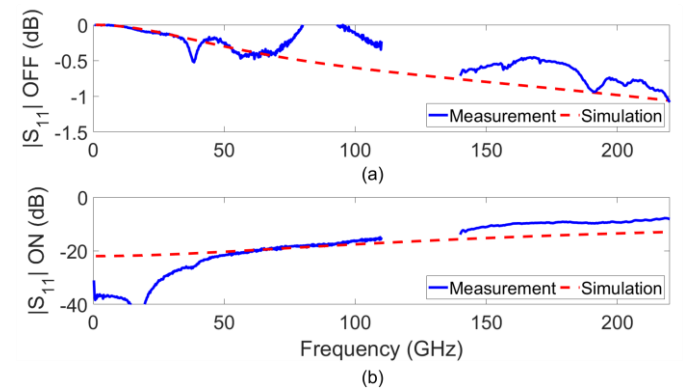


Fig. 13. Measured (solid line) and post-layout simulation (dashes) of the: (a) $|S_{11}|$ of the switching element in its OFF-state (i.e., $V_G = 0 \text{ V}$) and (b) ON-state (i.e., $V_G = 1.2 \text{ V}$).

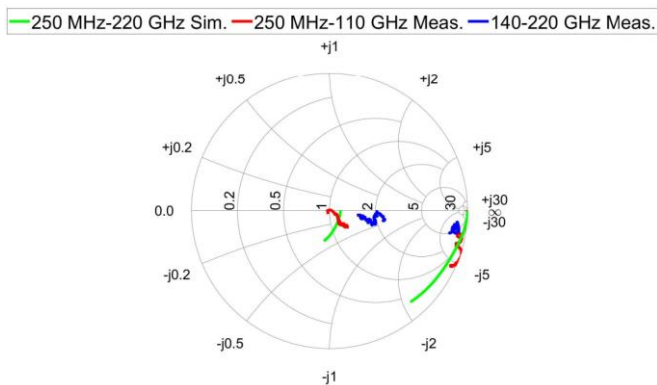


Fig. 14. Smith chart representation of the Load standard for its OFF (edge of the chart) and ON-states (center of the chart). The red lines present the 250 MHz-110 GHz measured frequency band, blue lines the 140-220 GHz measured frequency band and the green lines represent the [post-layout simulation-based results](#) in the 250MHz-220 GHz band.

between measurement and simulation in the upper part of the considered band. It is worth saying that the models in the Process Design Kit (PDK) have not been validated at these high frequencies and hence, some disagreement might be expected. In any case, the observed differences remain relatively contained.

Finally, Fig. 14 presents the Smith Chart representation of the measured S_{11} at the input of the MOSFET after de-embedding. Note that again, as frequency increases, divergence is observed. The simulation and 250 MHz – 110 GHz datasets show good agreement, while in the 140-220 GHz frequency band, simulation is less close to the measurement due to the limited accuracy of the PDK models.

C. Through-Load Measurement Results

Fig. 15 shows a microphotograph of the complete Through-Load system. The complete system, without access lines, RF and DC pads, has a footprint of 0.02 mm². The Through-Load element was measured using the same setup and measurement conditions employed for the MOSFET and presented above. In addition, the linearity was studied with input powers in the -20 to 3 dBm range, as limited by our test equipment. Within this range, the device showed a linear behavior. On the other hand, simulations show no significant compression with input powers up to 20 dBm.

Fig. 16 presents the measured (solid line) and post-layout simulation (dashed line) of the reflection coefficient

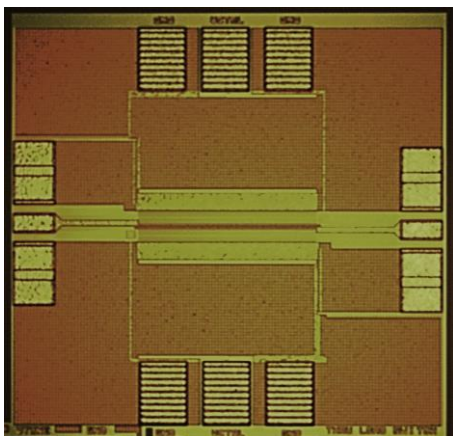


Fig. 15. Microphotograph of the Through-Load element.

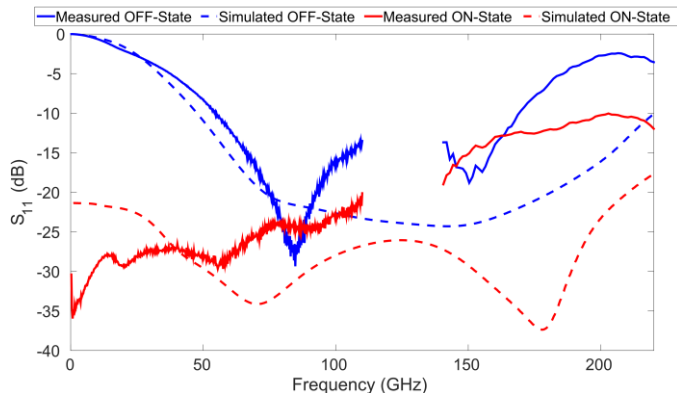


Fig. 16. Measured (solid line) and post-layout simulation (dashes) of S_{11} of the Through-Load system in its ON-state (i.e., $V_G = 1.2$ V) and OFF-state (i.e., $V_G = 0$ V)

magnitude of the Through-Load system in the 250 MHz to 220 GHz frequency band for both, ON- and OFF-states. Both measured datasets present relatively good agreement with their simulated counterparts. Again, some disagreement can be observed in the upper band due to the operation limits of the employed MOSFET models.

The proposed system shows a bandwidth of 115 GHz, from 55 to 170 GHz, if a return loss greater than 10 dB is considered. If the central frequency is considered to be the median between those values (i.e., approximately 112 GHz), the proposed system shows a Relative Bandwidth (RBW) of around 100% and hence presents a wideband solution, as intended.

Finally, Fig. 17 presents the post-layout simulation (dashed line) and measured (solid line) insertion loss of the Through-Load system in both, the ON- and OFF-states. Within the 55-170 GHz band, the measured and simulated insertion loss range between 0.6 and 1.6 dB in its OFF-state (i.e., behaving as a Through connection). On the other hand, the measured ON-state (i.e., behaving as a 50- Ω load) insertion loss ranges between 24 and 14 dB, similarly to the simulated dataset.

The device was integrated in a prototype run and hence we have very low number of samples from the same area of a single wafer. Process variations in our fabricated samples are negligible and do not lead to significant performance variations from one fabricated device to another. However, to get some insight into the effect of process variations, we performed a Monte Carlo (MC) analysis using the process variation and

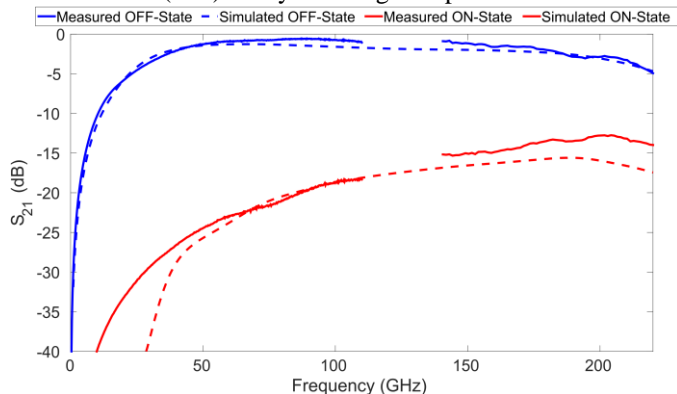


Fig. 17. Measured (solid line) and post-layout simulation (dashes) of S_{21} of the Through-Load system in its ON-state (i.e., $V_G = 1.2$ V) and OFF-state (i.e., $V_G = 0$ V).

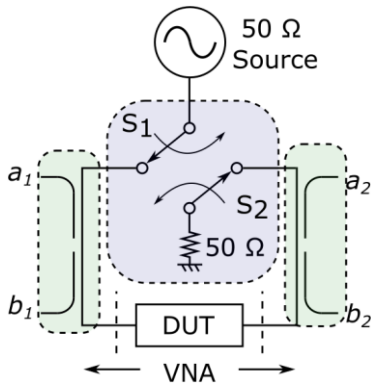


Fig. 18. Schematic representation of a VNA. The transfer-switch is in blue and the directional couplers are in green.

mismatch models provided in the Process Design Kit of the selected 55nm BiCMOS technology. This way, we generated 1000 instances of the Through-Load element. This analysis showed that, in the OFF-state (ON-state), the standard deviation of the Return Loss is around 0.4 dB (0.03 dB) while the standard deviation of the Insertion Loss is around 0.01 dB (1.6 dB). In addition, similar performance variations were observed for the simulated 0-100 °C temperature range. Hence, this architecture, integrated in the 55-nm BiCMOS technology, is robust against process and temperature variations.

IV. APPLICATIONS

Due to the large bandwidth, insertion loss difference between ON- and OFF-states together with the reduced losses in the OFF-state, multiple applications can take advantage of the proposed system. In particular, this paper will discuss two potential applications: (i) a Transfer-Switch, and (ii) an integrated attenuator.

A. Transfer Switch

A transfer switch is a device integrated within a multi-port VNA that is in charge of switching the port to whom the input wave is applied and the one acting as a 50-Ω load. A schematic representation of such device, together with the couplers of a 2-port VNA is shown in Fig. 18.

The operation of the transfer switch in an architecture like the one shown in Fig. 18 allows the measurement of the 4 scattering parameters describing the behavior of a 2-port system. First, the transfer switch is in the position shown in this figure, and thus injecting the signal of the 50-Ω source on the left port of the DUT and loading its right port to 50 Ω, allowing the measurement of S_{11} (i.e., b_1/a_1) and S_{21} (i.e., b_2/a_1). Then, the position of the switches in the transfer switch are inverted, injecting the signal on the right port of the DUT and loading its left port to 50 Ω, permitting the measurement of S_{12} (i.e., b_1/a_2) and S_{22} (i.e., b_2/a_2).

Note that this is a key element in a multi-port VNA. Hence, enabling the integration of multi-port VNA for on-wafer characterization and BIST applications demands the design of transfer switches. The design of mm-Wave transfer switches is still a major bottleneck for the integration of multi-port VNA solutions, as no on-silicon transfer switch, to the best of the authors' knowledge, has been reported in the literature up to this date.

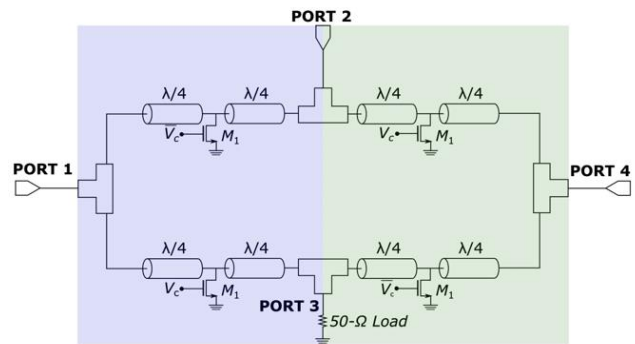


Fig. 19. Possible implementation of a transfer switch in the mm-Wave frequency band.

In the mm-Wave domain, a practical integrated transfer switch could be implemented as shown in Fig. 19 (i.e., using two Single-Pole Double-Throw, SPDT, switches highlighted in blue and green, and a 50-Ω load). However this architecture has several disadvantages. First, it is a relatively narrow-band solution as its bandwidth is limited by the $\lambda/4$ transmission lines. In addition, it presents a relatively large insertion loss. To illustrate this issue, current state-of-the-art MOS-based SPDT switches present around 3-4 dB of insertion loss [21]–[25]. In addition, if high-performance is targeted, a co-design of the transfer switches and the 50-Ω load has to be envisioned. Otherwise, the parasitics introduced may lead to a malfunction of the system.

In this context, the Through-Load system represents an attractive alternative for the implementation of this function as the co-design between coupler and 50-Ω load is inherently considered. For its implementation in a complete 2-port VNA architecture, the scheme shown in Fig. 20 can be proposed. Note that two Through-Load elements are required for this implementation and an additional power divider is required. An ideal power divider delivers half of the input power to each of its outputs (i.e., -3 dB of the input power to each Through-Load element). To maintain the bandwidth of the system, the coupled-line 3-dB coupler used for the implementation of the Through-Load element can be reused to implement the power divider function, eliminating the need for additional design steps.

It is important to note that a fraction of the power would be lost in the Through-Load system that is in its ON-state (i.e., ideally, 3-dB). However, this loss together with the losses of the Through-Load element – around 0.6-1.6 dB, in this design –

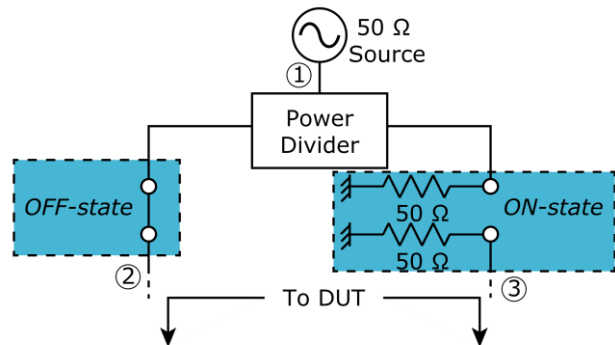


Fig. 20. Possible implementation of a transfer switch using the proposed Through-Load architecture.

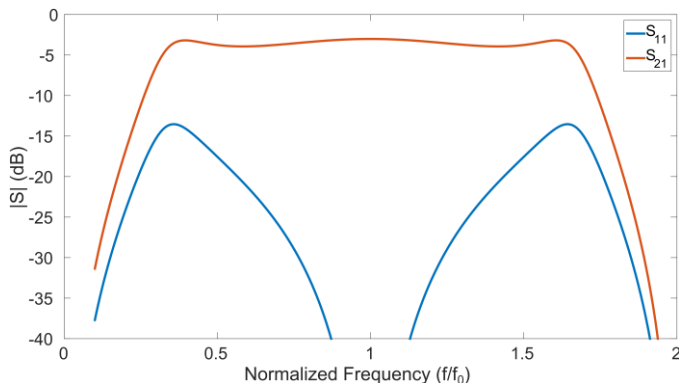


Fig. 21. S-Parameters of the proposed transfer switch architecture using ideal elements and a 3-dB coupled-line coupler to implement the power divider.

represents the same loss that the current SPDT solutions present [21]–[25], while improving their bandwidth and avoiding the additional step of accurate 50- Ω load design that they would require.

For instance, if ideal elements are considered and a 3-dB coupled lines coupler is used for the implementation of the power divider, the S-Parameter magnitude of the proposed solution can be traced versus the normalized frequency where f_0 is the central frequency of the coupler, as shown in Fig. 21. Note that port 1 corresponds to the output of the 50- Ω source in Fig. 20 and port 2 is connected to the output of the Through-Load element in the OFF-state (i.e., left port of the DUT in Fig. 20).

As seen in Fig. 21, such a solution would present a return loss greater than 13 dB for any frequency and an insertion loss lower than 5 dB from normalized frequencies ranging between 0.3 and 1.7. Isolation between the two ports of the DUT (i.e., ports 2 and 3 in Fig. 20) is not seen in Fig. 21 as its magnitude using ideal elements is null at any frequency. A similar behavior would be observed for the return loss seen at the output of the DUT meant to be loaded by 50 Ω (i.e., $|S_{33}| = 0$).

To put this idea into perspective using real devices, let us use the measurements to implement the circuit in Fig. 20. For this purpose, the power divider is integrated using the 3-dB coupler presented in section III.A. and the Through-Load elements presented in section III.C. Note that only 1-145 GHz measurements could be carried out for the 3-dB coupler. Hence, the results beyond 140 GHz reported hereby are carried out

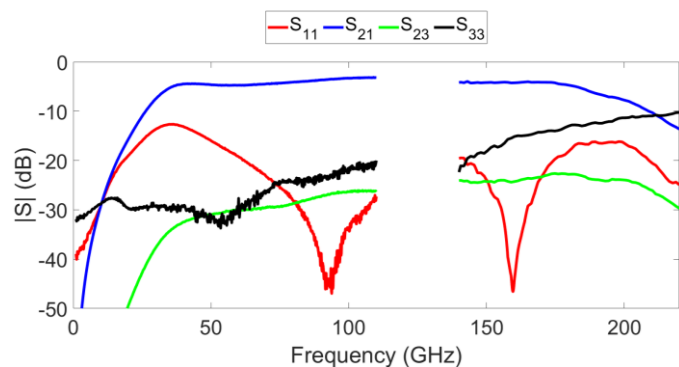


Fig. 22. S-Parameters of the proposed transfer switch architecture using measured data. Results beyond 110 GHz were obtained by using the simulations of the 3-dB coupler with the measurement of the Through-Load element.

TABLE I
STATE-OF-THE-ART TRANSFER SWITCHES

Ref	[26]	[26]	This work
Freq. (GHz)	140-220	140-195	35-180
$ S_{11} $ (dB)	>10	>10	>13
$ S_{21} $ (dB)	4.5-5.9	5.7-7	3.2-5
$ S_{23} $ (dB)	20-33	27-44	24-33
$ S_{33} $ (dB)	10-32	13-18	13-32
# of DC voltages	2	2	1
Area (mm ²)	0.58	0.69	$\approx 0.06^1$

¹Estimated

using the simulation-based results for the coupler. As this device was not fabricated, the interconnections are considered to be ideal. However, the geometry of the building blocks allows to directly connect them with practically zero-length interconnections.

These results are shown in Fig. 22, which displays the magnitude of the most relevant S-Parameters for this application across the 1-220 GHz frequency range. In this configuration, at a 110 GHz, the proposed system presents an insertion loss of 3.2 dB, really close to its ideal 3 dB of losses shown in Fig. 21. At this frequency, the isolation (i.e., $|S_{23}|$) is of 24 dB, its return loss of 27 dB at the RF source level (i.e., S_{11}). Finally, the port of the DUT that is meant to be loaded by 50 Ω , would effectively see a load close to this value, as the return loss at this port, S_{33} , is of 20 dB, at 110 GHz.

In addition to the high performance observed at 110 GHz, another great advantage of this architecture for the implementation of transfer switches is its large bandwidth. Indeed, the insertion loss is lower than 5 dB in the 35-180 GHz frequency band. Moreover, the isolation is below 24 dB for any frequency in the considered band. Throughout the whole considered band, the return loss at source level and the loaded side of the DUT is greater than 13 and 10 dB, respectively.

To the best of authors' knowledge, currently, only one mm-wave transfer switch has been reported in the literature in a silicon-based technology [26]. This work reports two implementations of transfer switches using different architectures but mainly based on the schematic view shown in Fig. 19.

A comparison between the results reported in [26] and the results obtained in this paper is shown in Table I. The proposed architecture is superior in most of the analyzed metrics, it shows a much greater bandwidth, reduced losses, better 50- Ω matching, increased control simplicity and a much reduced footprint. In terms of isolation and return loss both

TABLE II
STATE-OF-THE-ART ATTENUATORS

Ref	Tech.	Freq. (GHz)	Att. Range (dB)	RL (dB)	1-dB CP (dBm)	Power (mW)	# of DC voltages	Area (mm ²)
[27]	0.13- μ m CMOS	DC-2.5	1.5-42	> 8.2	2.5	1.9	5	N/A
[28]	0.18- μ m BiCMOS	10-67	13-53	>8.4	0	0	5	0.76
[29]	0.8- μ m CMOS	DC-0.9	3-31	>9	5	12	N/A	1.57
[30]	0.18- μ m CMOS	DC-14	10-40	>10	15	0	8	0.5
[30]	0.18- μ m CMOS	8-12	10-40	>10	13	0	8	0.34
[31]	GaAs	0.045-50	3-70	>10	N/A	0	14	5.8
[32]	0.12- μ m BiCMOS	10-50	2-13	>9	4	0	12	0.15
[33]	65-nm CMOS	10-50	5-18	>8.7	15	0	12	0.19
[33]	65-nm CMOS	15-43	4-17	>8.8	14	0	12	0.29
This work	55-nm BiCMOS	55-170	0.6-20	>10	>3	0	1	0.02

architectures present similar performance. Hence, the proposed architecture presented hereby appears as a major solution for the implementation of mm-wave transfer switches in integrated technologies, which could lead to new characterization paradigms.

B. Attenuator

Attenuators are a ubiquitous element in measurement setups, as measurement systems often need to operate in relatively low-power conditions. Hence, for DUTs whose output/input power is high, an attenuation scheme is required to protect the measurement systems.

Integrated attenuators [27]–[32] have been widely studied in the past years. However, very few demonstrators in the mm-Wave band have been reported using silicon-based technologies [28], [32]. Most of the reported designs [28]–[33], require multiple control voltages as different stages aiming at different attenuation levels are designed in a discrete-control perspective. In addition, some of these works [27], [29] use amplification schemes to counteract the large losses of the proposed attenuator in its minimum attenuation state.

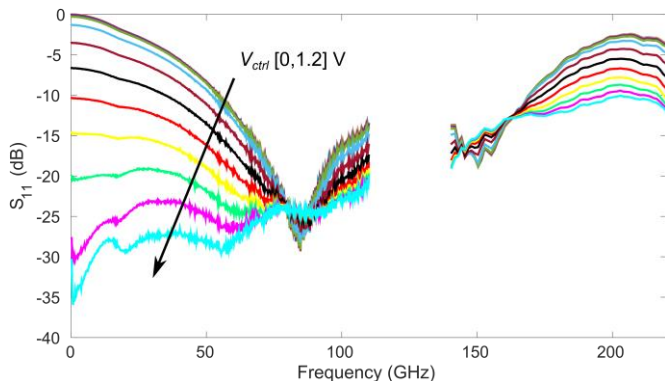


Fig. 23. Measured return loss magnitude of the through-load element with $V_G = [0 - 1.2]$ V in the 250 MHz – 220 GHz band.

In the previous sections of this document, only the so-called ON- and OFF-states (i.e., V_G equals to V_{DD} and 0 V, respectively) were explored. However, a new functionality appears when the voltages ranging between these two states are considered.

In this line, we consider the setup presented in section III and sweep V_G from 0 to 1.2 V with a 100 mV step. Fig. 23 presents the $|S_{11}|$ measurement in the 250 MHz to 220 GHz band. In the previously considered bandwidth of the Through-Load switch element (i.e., 55-170 GHz), the system respects the 10 dB return loss condition imposed for the bandwidth consideration for any V_G state.

Fig. 24 shows the obtained results for the $|S_{21}|$, obtained under the same conditions as the previously presented results. It can be noted that an attenuator-like behavior is observed. This behavior is observed over a large bandwidth and can be continuously tuned using the control voltage V_G . In the considered bandwidth of the Trough-Load element, the system provides a tunable attenuation between 1.6 and 14 dB in its

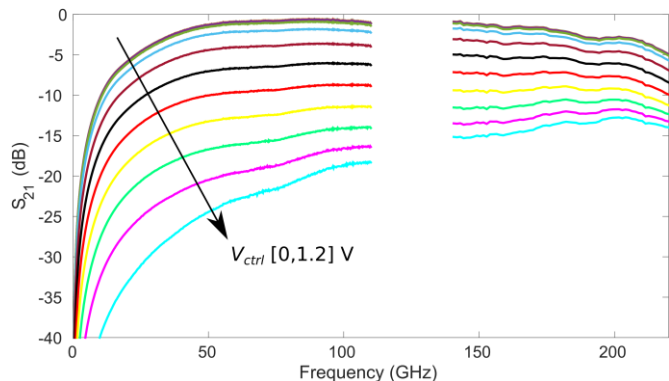


Fig. 24. Measured insertion loss magnitude of the through-load element with $V_G = [0 - 1.2]$ V in the 250 MHz – 220 GHz band.

narrower point (i.e., 170 GHz). However, at around 90 GHz, the attenuation can range between 0.6 and more than 20 dB.

The proposed Through-Load is a passive system that has the advantage of requiring solely one control voltage that can, in addition, be tuned in a continuous manner to, in its turn, vary the attenuation level as a continuous function of V_G . In addition, if greater levels of attenuation are required, multiple instances of the proposed element can be easily cascaded, which would in turn be controlled by the same V_G control voltage. If this strategy is adopted, disregarding the interconnection parasitics, the insertion loss for each state of the through-load system would be a linear (in dB) function of the number of cascaded Through-Load systems.

For instance, if the measured Through-Load system is considered and the interconnection parasitics are disregarded, when cascading three Through-Load systems an attenuation range between 1.8 dB and 60 dB could be achieved, at 90 GHz. This considered structure would only require a single control voltage and would only represent a compact footprint of 0.06 mm².

To put the obtained results into perspective, Table II presents the results of the proposed attenuator together with the current state-of-the-art proposals for the implementation of this circuit. First, note that the proposed system presents the highest operating frequency and an ultra-wideband coverage. In addition, it presents the most reduced losses in its low-attenuation state. Even though it presents a moderate attenuation in its maximum attenuation state, its reduced footprint (i.e., around a 90% reduction to the smallest implementation in the considered state-of-the-art) together with its reduced losses makes it an excellent candidate for being cascaded with several instances of the same element, as introduced before. Moreover, its biasing simplicity, power handling capabilities and passive configuration makes it an optimal candidate for the implementation of mm-Wave and sub-THz attenuators.

V. CONCLUSIONS

This paper proposes a novel on-chip Through-Load element for integrated mm-wave applications. The proposed element offers a programmable behavior that can be switched from a 50 Ω load to a Through connection using a single DC control voltage. The functionality of the proposed element is analytically studied and detailed guidelines are provided for its design in advance nanometric integrated technologies.

A prototype demonstrator in STMicroelectronics 55-nm BiCMOS technology has been fabricated and characterized in the laboratory to show the feasibility and performance of the proposed Through-Load element. On-silicon results at 90 GHz demonstrate an insertion loss ranging from 0.6 dB to 20 dB as a function of V_G , and a return loss of around 25 dB. In addition, the proposed system shows an ultra-wide bandwidth of 115 GHz, considering a return loss greater than 10 dB, which represents a relative bandwidth of around 100%.

Finally two possible applications of the proposed Through-Load element are outlined: (i) a building block for a transfer-switch function, (ii) an attenuator. Comparisons are carried out with the current state-of-the-art implementations of these circuits, showing the potential of the proposed architecture.

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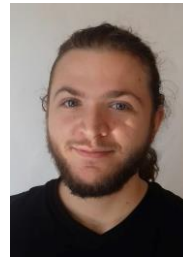
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