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# A self-powered integrated solution for frequency tuning of piezoelectric energy harvesters

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**Abstract**—This paper presents the integrated design of a tunable interface for wideband energy harvesting, the Short-Circuit Synchronous Electric Charges Extraction (SC-SECE). By tuning both the phase of the energy harvesting event,  $\phi_S$ , and the angular duration of the short-circuit phase,  $\Delta\phi$ , this interface maximizes both the harvested energy while tuning the dynamics of the energy harvester. The proposed ASIC is self-powered, includes a cold start, and only consumes less than  $1\mu W$ , which is a very small percentage of the harvested energy. It includes as well a low-power ( $24nW$ ) gradient algorithm which controls the value of  $(\phi_S, \Delta\phi)$  and tries to maximize the harvested power for any vibration's frequency and amplitude.

## I. INTRODUCTION

Wireless sensor nodes designed to ensure risk prevention and monitoring are more and more present in our day-to-day life. Most of these sensors only require a small amount of energy to sense, process and send data. This makes energy scavenging a good alternative to batteries, as it may lead to systems combining long lifetime, robustness, and compactness. In closed and confined environments, where the thermal gradients and solar radiations are weak, the major energy source can be found under the form of mechanical vibrations.

Among electromechanical transducers, piezoelectric materials are of interest because of their good trade-off between power density and technological maturity. In order to amplify the mechanical strain applied on such materials, they are usually deposited on a linear mechanical oscillator having high quality factor. The main drawback of such structure is the drastic decrease of power when there is a slight mismatch between the vibration frequency and the harvester resonant frequency. Mismatches may be caused by several reasons such as inaccuracy in the harvester fabrication leading to a shift of the resonant frequencies, aging of the mechanical oscillator, change in the ambient vibration spectrum, among others. In order to face this challenge, some electrical strategies have been proposed in order to electrically tune the dynamics of a highly coupled energy harvester [1-2]. Among them, it has been shown that the Short-Circuit Synchronous Electrical Charge Extraction (SC-SECE) interface allows to drastically enlarge the energy bandwidth while maximizing the harvested power [2]. However, a self-powered implementation of the SC-SECE has yet to be designed.

In this paper, we propose an integrated ASIC implementing the SC-SECE in  $0.6\mu m$  XFAB. The proposed

design is self-powered, includes a cold-start system, and is able to tune the harvester dynamics in order to work at resonance on a relatively large frequency band.

## II. PROPOSED INTEGRATED SYSTEM

The proposed integrated circuit implements the SC-SECE strategy, a non-linear extraction technique that alternates energy harvesting times and short-circuits times. Two tunable parameters are used:  $\phi_S \in [0, \pi]$  and  $\Delta\phi \in [0, \pi]$ . As depicted in Figure 1,  $\phi_S$  represents the angle between the mechanical displacement extremum and the energy harvesting event, and  $\Delta\phi$  represents the angular duration of the short-circuit. These two parameters allow to electrically tune the resonant frequency of the harvester as well as its damping [2]. The system power path is shown in Figure 2, and the MOS are controlled in order to obtain the SC-SECE waveforms shown in Fig.1. A detailed sequencing of the proposed interface is given in [3], in the standard SECE case ( $\phi_S = \pi$  and  $\Delta\phi = 0$ ).

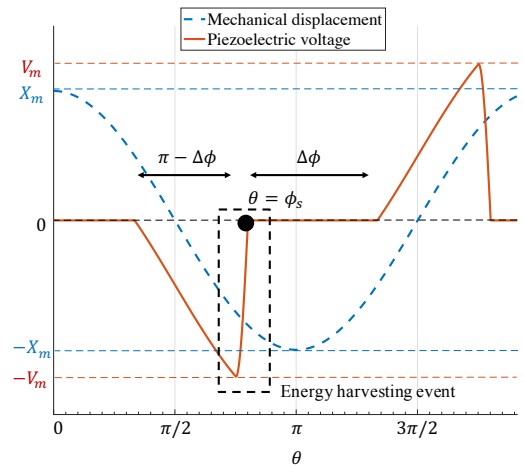


FIGURE 1. MECHANICAL DISPLACEMENT AND PIEZOELECTRIC VOLTAGE WAVEFORMS OF THE SC-SECE [3]

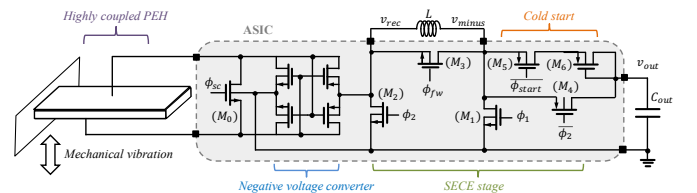


FIGURE 2. POWER PATH OF THE PROPOSED SC-SECE INTERFACE

## III. IMPLEMENTATION AND INTEGRATION CHALLENGES

## A. Consumption of the self-powered interface

In order to control the various power MOS shown in Fig. 2, many analog senses and a low-power MPPT algorithm have been designed. The main constraint we had, while designing these circuits, was their energy consumption which should not be greater than a small percent of the harvested energy. Figure 3 shows the main analog and digital functions of the control interface, as well as their respective energy consumptions. The total power consumption of the senses does not exceed  $1\mu W$ , which is much smaller than the harvested energy in most case ( $100\mu W - 1mW$ ).

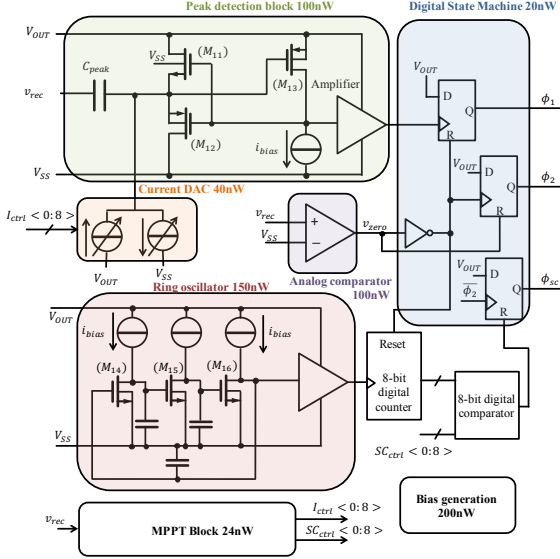


FIGURE 3. SIMPLIFIED VIEW OF VARIOUS ANALOG SENSES

The MPPT algorithm itself does not consume much power ( $24nW$ ), and proves that designing a self-powered algorithm is feasible and not a major constrain.

## B. Losses in the harvesting interface

The other losses in the interface are not linked with the senses shown in Figure 3, but with the power path itself (Figure 2). The total losses in the harvesting interface can be expressed as the sum of switching losses  $P_{sw}$ , conduction losses  $P_{cond}$ , and transfer losses  $P_{trans}$ :

$$P_{loss} = P_{sw} + P_{cond} + P_{trans} \quad (1)$$

$$P_{loss} = f_{vib} V_{out}^2 \sum \lambda_{C_{in_i}} W_i + \frac{1}{2} I_0^2 \sum \frac{R_S L_i}{W_i} + I_0^2 R_L \quad (2)$$

Where  $(W_i, L_i)$  are the width and length of each transistor in the power path,  $f_{vib}$  the vibration frequency,  $\lambda_{C_{in}}$  the gate capacitance per transistor unit length,  $R_S$  the sheet resistance of the MOS channel,  $I_0$  the RMS current in the inductance, and  $R_L$  the inductance parasitic resistance. Since  $f_{vib}$  is usually relatively low  $\approx 20 - 1000H_z$ , the switching losses are usually much lower than the conduction and transfer losses. For a particular technology, there are three possibilities to reduce those losses:

- Decreasing  $I_0$ . This can be done thanks to circuit techniques, such as the Multi Shot-SECE [4], or by making faster harvesting events with a harvester/inductance of smaller size.
- Increasing  $W_i$ . However, this increases the surface of silicon used for the interface. In our case, to obtain an efficiency of 90% we had to use a silicon surface of  $5mm^2$ .
- Decreasing  $R_L$ . However, this usually lead to an increase of the inductance size.

## C. Power limits of the interface

One major limit of any SECE-based interface relies in both the interface breakdown voltage and saturation current of the inductance. Indeed, the maximum extracted power from the harvester is given by:

$$P_{max} = \min(f_{vib} V_{lim}^2 C_p, f_{vib} I_{sat}^2 L) \quad (3)$$

With  $C_p$  the capacitance of the piezoelectric material,  $V_{lim}$  the limit voltage that may be supported by the electrical interface, and  $I_{sat}$  the saturation current of the inductance  $L$ . If we want to increase  $P_{max}$ , there are two possibilities:

- Increasing  $C_p$  by an appropriate harvester design. However, since  $C_p$  is proportional to the surface of the piezoelectric material, this often leads to an increase of the harvester size.
- Increasing  $V_{lim}$  thanks to the choice of high voltage transistors/technology. In our case, we chose to use high voltage transistors from XFAB whose maximum  $V_{DS}$  and  $V_{GS}$  are 20V. However, the higher the voltage limit of a transistor, the greater its  $L_i$ . Therefore, choosing high voltage transistors will both increase their size and their conduction losses.
- Increasing  $L$ . This choice should be made carefully since there is a direct relation between the saturation current value of an inductance and its size. Finally, all these tradeoffs have been summarized in Table 1.

TABLE 1. TRADEOFFS FACED DURING THE INTERFACE INTEGRATION

	System size	Switching losses	Conduction losses	Transfer losses	Maximum power
Increasing the transistors sizes	⊗	⊗	⊕⊕	=	=
Increasing the harvester size	⊗	=	⊗	⊗	⊕
Increasing the inductance size	⊗	=	=	=	⊕⊕
Choosing higher voltage transistors	⊗	⊗	⊗⊗	=	⊕⊕
Adopting multishot techniques	=	⊗	⊕	⊕	⊕⊕

## IV. CONCLUSION

In this paper, we present the design of an ASIC implementing the SC-SECE strategy, whose power consumption is lower than  $1\mu W$  in typical conditions. Challenges arise when we want to increase the harvested power while keeping the size of the system as low as possible. Transient waveforms, details of the operation modes, and final results of this circuit will be presented during the conference.

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