Study of mobile ionic charges by thermally stimulated currents in 4H-SiC MOS capacitors with thick SiO2 layers

Christophe Raynaud, Marie-Laure Locatelli, J.F. Mogniotte, R. Arvinte, G. Grosset

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C. Raynaud[a], M.-L. Locatelli[b], J.-F. Mogniotte[c], R. Arvinte[b], G. Grosset[d]

[a] Univ Lyon, INSA Lyon, CNRS, Ampère, F-69621, France

[b] LAPLACE ; Université de Toulouse, CNRS, UPS, INPT; France

[c] HYBRIA Institute of Business & Technologies, Univ Lyon, INSA Lyon, Ampère UMR 5005, F-69621, France

[d] Ion Beam Service, ZI Peynier Rousset, rue Gaston Imbert, F-13790, France

Abstract

Thick oxides deposited on 4H-SiC epilayers to form Metal-Oxide-Semiconductor capacitors have been studied by Capacitance-Voltage (CV) and Thermally Stimulated Ionic Current (TSIC) measurements. The very negative flatband voltage V_{FB} in regards to the theoretical value indicates the presence in the oxide of a large number of positive charges. Positive mobile charges are responsible for a large part of this unusually V_{FB}, as shown by the hysteresis cycle on CV characteristics. Four traps have been detected at the gate/oxide interface and three at the oxide/SiC interface. One of them is similar to a trap already detected in MOS 3C-SiC and 6H-SiC structures. The others seem rather different. Dependences of the detrapping energy of mobile ions in these traps have been determined. Secondary Ion Mass Spectroscopy analyses have shown the presence of K^+ and Na^+ ions in the oxide in concentrations that agree well with the values obtained by TSIC measurements.

Keyword : silicon carbide; thick oxide; oxide traps; mobile ions

1. Introduction

Silicon Carbide as a wide band gap semiconductor has been extensively studied in the past 25 years. Thus a large number of discrete devices have been demonstrated. The technology is now mature enough to provide commercial devices in the area of high voltage electronics. 600V, 1200 V and even 3300 V Schottky diodes are commercially available with different nominal current ranges, up to 50A for 1200 V diodes. Best laboratory results achieved breakdown voltage of 10.8 kV in 2003 [1]. Development of SiC MOS devices have been more complicated. Indeed, since the revival of SiC in 90's (with the development of the sublimation method for crystal growth, and the first commercialized 1" wafer), studies on the thermally grown oxide to form SiO_2/SiC interface, the main useful one for MOS devices, have always shown a higher defects density than on silicon devices [2], especially on p-type layers. However some progress have been made, especially with the nitridation process and the interface state density and the oxide traps density have been noticeably reduced [see for example 1c and reference therein]. It is important to note that deposited oxides are generally of poorer quality than thermally grown layers, in terms of interface states and bulk impurities (fixed and mobile charges) [2, 3]. Recently deposited oxides on 4H-SiC show a low interface state density in the range 9×10^{11} $cm^{-2}eV^{-1}$ [3] and low densities of fixed and mobile charges, but these oxides are thin (< 50nm). Research progress finally have resulted in the commercialization of power MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) that are available up to 1700 V. However, some problems remain to be solved. For instance, power MOSFETs are currently studied because they suffer from reliability issues such as a shift of the threshold voltage during their functioning [4], or premature breakdown of the devices due to short-circuit [5]. Some of these problems which are crucial to develop reliable power devices for industrial applications are suspected to be correlated to the presence of defects in the gate oxide. For other power devices e.g. JBS (Junction Barrier Schottky) or bipolar diodes, able to sustain voltages as high as possible in regards to their theoretical capabilities, periphery of the component has to be carefully designed. By periphery, we mean the termination of junction, e.g. JTE (Junction Termination Extension), or guard rings, but also the passivation layer above the semiconductor surface. This passivation layer is generally formed by a primary layer

directly deposited or grown on SiC epilayer, i.e. SiO_2 (before the metallization process). A secondary layer encapsulates the first one. This secondary coating may be a polymer. Concerning the primary passivation layer, a large thickness can be needed and the quality of this oxide (i.e. the density of the charge therein) is crucial, because it directly influences the efficiency of the periphery protection [6]. We have performed TSIC (Thermally Stimulated Ionic Current) measurements and SIMS (Secondary Ion Mass Spectroscopy) analyses on MOS capacitors, having an oxide layer equivalent to the one required for passivation layer, i.e. in the order of 1 μm. It is far thicker for standard MOSFET transistor structures. SIMS allows to identify the chemical species present in the oxide, and their densities, but with some uncertainties in their distribution. TSIC analyses can give information on their densities and also on their trapping-detrapping properties at the interfaces (Metal/SiO_2 and SiO_2/SiC interfaces). Thus these two techniques are rather complementary. TSIC technique is not commonly used and no literature is available concerning TSIC on 4H-SiC. All available data concern silicon devices ; only one study obtained on 6H and 3C-SiC polytypes has been published [7] to our knowledge.

2. Experimental details

2.1. Description of the samples

In order to fabricate high voltage devices with periphery protections including a thick silica passivation layer, we have realized MOS capacitors as test structures, on the same wafer, and using the same fabrication process characteristics. A N-type epilayer (of 35 μm thickness, and $8.5x10^{14}$ cm^{-3} doping level) grown on a 4H-SiC N^+-type substrate, purchased from Showa-Denko, has been used. The oxide layer was obtained initially by wet oxidation of the 4H-SiC epilayer surface in order to grow a thin SiO_2 film of ~30 nm in thickness. Further, a thick SiO_2 layer of ~1.5 μm was deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) process using TEOS (tetraethoxysilane). An ohmic contact at the substrate back side was obtained by metal deposition and an annealing was performed in order to realize the bottom electrode of the MOS structures. The front side electrode

(gate) consists in an Ag/Ni/Ti stack with a total thickness of around 2 μm, deposited by successive sputtering steps. Circular front side electrodes of 1.5 mm in diameter were shaped by photolithography. Then, after a secondary passivation layer spin-coating and photolithography, a final annealing (polymerization cure) was applied to the wafer.

2.2. Description of the test bench

C-V (Capacitance-voltage) measurements have been made using a Keysight impedance analyzer E4990A, or a power device analyser B1505 when voltages higher than 40 V were required. As the MOS capacitors are on wafer chips, a probe station has been used to contact the gate and the substrate (back side). TSIC measurements have been performed using a Keithley SourceMeter K2636,and a cryostat in which the DUT (device under test) was glued with silver lacquer, to ensure a good thermal contact. The temperature range available is ~80 K up to ~600K. A vacuum of ~ 10^{-6} mbar is obtained after a first heating to 600 K. The applied voltage is limited to 200 V by the apparatus.

3. Results and discussion

3.1. Preliminary measurements: CV at room temperature and at high temperature.

C-V measurements have been realized at room temperature at a frequency of 100 kHz (the highest frequency leading to still negligible series resistance effects), on a device with a diameter of 1.5 mm (Figure 1), in the two scan directions. From the maximum capacitance C_{ox} in accumulation regime (V >0), the deduced oxide thickness is e_{ox} = 1.57 μm. As expected in 4H-SiC, no inversion layer is observed due to the very weak minority carrier generation rate. So the depletion regime is used to determine the doping level and the flatband voltage V_{FB} by plotting $(C_{ox}/C)^2$-1 vs. V_G (inset of Figure 1). From the slope, the doping level is estimated to be 8.0×10^{14} cm^{-3}, which is in agreement with the epilayer data sheet.

No difference is observed between C(V) curves in the two scan directions when the gate voltage V_G is limited to -100 V (arbitrary chosen for first precautious measurements). When biasing down to -200 V in depletion mode, a little shift of ~2 V is observed on V_{FB} between the curves obtained in the two scan directions at 300K. V_{FB} = -59,4 V using the sweep from accumulation to depletion mode, and -V_{FB} = -61.6 V using the sweep from depletion to accumulation mode. The difference of ~2V in V_{FB} values may be due to the presence of deep states (interface states which have a longer response time and that can discharge during the bias sweep, either because they are deeper in the bandgap, either because they are a little deeper in SiO_2 than interface states) which need a longer time to discharge, so that a scan from -100 V to positive bias is not long enough to allow deep traps to emit their electron. On the contrary, scan from -200 V to positive bias is longer and emission of electrons from deep traps is more probable and V_{FB} is a little reduced. Of course, such high values of V_{FB} are no more observed in thermally grown oxide, usual values are in the [-5V, 5V] range [8]. However,

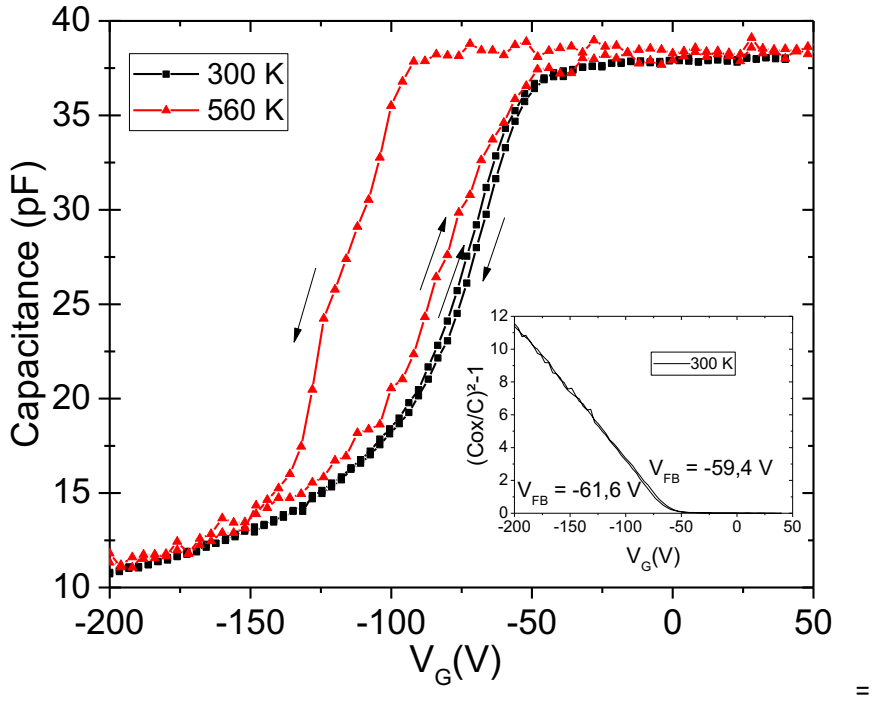

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Figure 1 : C-V characteristics measured at 100 kHz on the 1.5 mm Ø capacitors at 300 K and 560 K. The inset shows the linear plot of $(C_{Ox}/C)^2$ -1 vs V_G.

these large negative values of V_{FB} indicate the presence of a large amount of positive charges in the oxide Q_{ox}. If these charges are fixed charge at the SiO_2/SiC interface their density should be at least of 8×10^{11} cm^{-2} to result in V_{FB} ~ -59 V. But it is more probable that they are also mobile charges or charges trapped in the oxide bulk.

Similar C-V measurements have been performed at 560 K. A clear difference is observed between the two sweep directions, resulting in a higher V_{FB} shift (~37 V, resulting in V_{FB} ~-100 V when sweeping from +200V to -200 V). Note that the hysteresis loop between the two C-V curves shows a clockwise rotation at 300 K but a anti-clockwise rotation at 560 K. The anti-clockwise rotation should be relevant of the presence of mobile charge in the oxide. Indeed, if positive mobile charges are present in the oxide, when V_G >0, they are at the SiO_2/SiC interface and so they induced a negative flatband shift. When they are at the gate/SiO_2 interface, they do not induce any flatband shift, and the C-V from depletion to accumulation is shifted toward the right. It results in an anticlockwise rotation! A shift of ~37 V should be relevant to a mobile charge density of $\sim5\times10^{11}$ cm^{-2}. To compare, mobile charges in SiO_2 grown on silicon are inexistent, or so low that undetectable and without consequence. Two of the most recent publications about alkali ions in SiO_2 grown on Si date from 1984 [9] and 1988 [10], and in these studies, alkali ions have been intentionally introduced in the oxide. This is the reason why there is a lack of knowledge about ions mobility in SiO_2.

Previous to TSIC measurements, isothermal I-V measurements have been performed at 300 K between -200 V and 200 V and no significant current (> 1 pA) have been measured. It is consistent with the high thickness of the oxide layer (e.g. no Fowler-Nordheim mechanism is possible with such a thickness).

3.2. TSIC measurements

In order to understand the origin of this large negative flatband voltage shift, TSIC measurements have been performed. This technique has been developed by Hickmott [11] to study the effect of sodium ions in SiO_2 grown on silicon, and also by Choquet et al. [10] to study Na and K ion in SiO_2.

This technique consists in measuring with a picoammeter the current I flowing across the oxide, i.e. between the gate and the substrate of a MOS structures as a function of temperature T.

The structure is preliminary heated at high temperature (in our case at 600 K for the worst tests) under a constant gate bias (the trapping voltage) V_G, so that the mobile ion, if there is, are driven by the electric field in the oxide towards the interface. If the mobile ions are positive, which is generally assumed for alkali ions such as Na^+ or K^+, they are driven and trapped at the SiO_2/SiC (ox/SiC) interface when V_G >0, and at the metal/SiO_2 (G/ox) interface when V_G <0. After that the structure is cooled down to 100 K. Then, the gate bias is changed to $-V_G$ (the detrapping voltage) and the temperature is increased with a fixed rate α. In our case, α has been fixed to either 0.1 or 0.2 Ks^{-1} so that the heating sweep does not exceed ~90 min. When the mobile ions are detrapped from the interface, the picoammeter measures a current peak at a temperature named T_{max}. Knowing the heating rate, the area A under the I-T curve is related to the density of the detrapped mobile charges by the relation $A = q\alpha N_m$. Details of the technique are described in Ref. [10]. T_{max} is related to the energy E of the detrapping by

$$\frac{\sqrt{E}}{kT_{max}^2} = \frac{\upsilon}{\alpha}\exp\left(-\frac{E}{kT_{max}}\right) \quad \text{(Eq. 1)}$$

where ν is a factor ranging from 10^{10} to 10^{13} s^{-1} $eV^{-1/2}$ and k the Boltzmann constant. Solving (Eq.1) using a mean value of $\nu = 5\times10^{11}$ s^{-1} $eV^{-1/2}$ allows to calculate E for each value of T_{max}. The oxide electric field ξ_{ox} is calculated by

$$\xi_{ox} = \frac{V_G - V_{FB}}{e_{ox}} \quad \text{(Eq.2)}$$

So for each value of V_G, T_{max} can be related to the corresponding ξ_{ox}. The plot of E vs. $\xi_{ox}^{1/2}$ and its slope χ is useful to compare our results to other published results. Since V_{FB} varies drastically with voltage at high temperature, a variation of the electric field during the heating sweep should be considered.

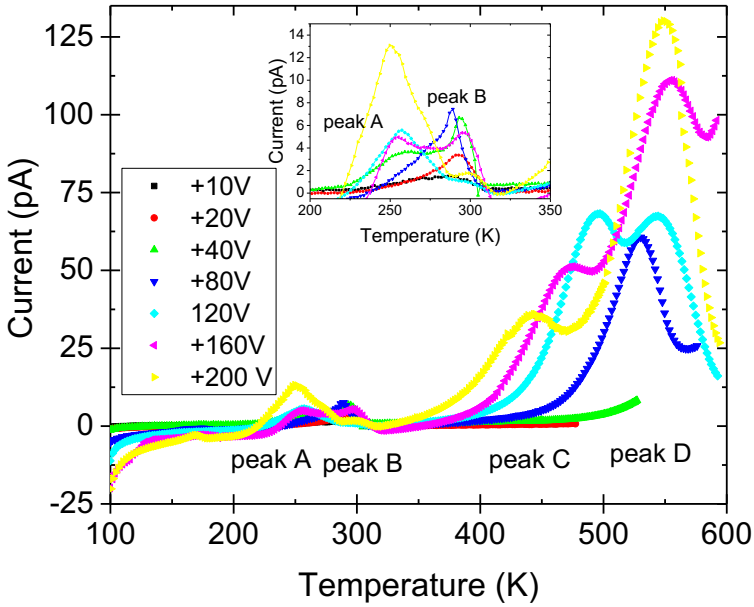

Figure 2 : TSIC spectra recorded under several positive detrapping gate bias $-V_G$ varying from +10 V to +200 V, after a trapping at high temperature under negative V_G. The observed peaks are due to detrapping at the gate/SiO_2 interface. The inset is a zoom on the current between 200 and 350 K.

Figure 2 shows different TSIC spectra as a function of a positive detrapping voltage (positive $-V_G$ applied during heating). The inset is a zoom on the current between 200 and 350 K. Mainly 4 peaks are observed during the sweeping from low to high temperature. The maxima of these 4 peaks seem to be dependent on the applied voltage. Two of them appear at ~250 K (peak A) and ~300 K (peak B) and are of relatively small magnitude (i.e. 1-10 pA). The two others appear at higher temperatures (between 450K and 530 K for peak C, and at 550 K for peak D) and are of larger amplitude. These peaks are relevant for detrapping at the G/ox interface.

To be accurate, the current must be recorded also during temperature scan without reversing the voltage supply at low temperature. The current so measured is called the baseline. It should consist in leakage current which should occur without the contribution of the mobile charges. Since each

scan is time consuming, the baselines have been measured for trapping voltages of 120 V, 200 V and -120 V (Fig. 3). Therefore the real TSIC measurement is obtained by subtracting the baseline from the scan obtained at the same trapping voltage value. A surprising feature of these baselines is the presence of a peak at ~540 K. We believe that it is due to an incomplete trapping at high temperature before cooling down . Two reasons can be considered : i) maybe the time of trapping is not long enough; ii) maybe the temperature of 600 K is not high enough. The inset in Figure 3 shows a small peak that appears on the baseline for positive V_G. We have no explanation for this peak, unless it is due to the ionization of carriers in the N-type epilayer, which could lead to the formation of an inversion layer and modify the electric field in the oxide. However, the magnitudes of these baselines are very low and therefore they do not modify the analyses of the TSIC spectra.

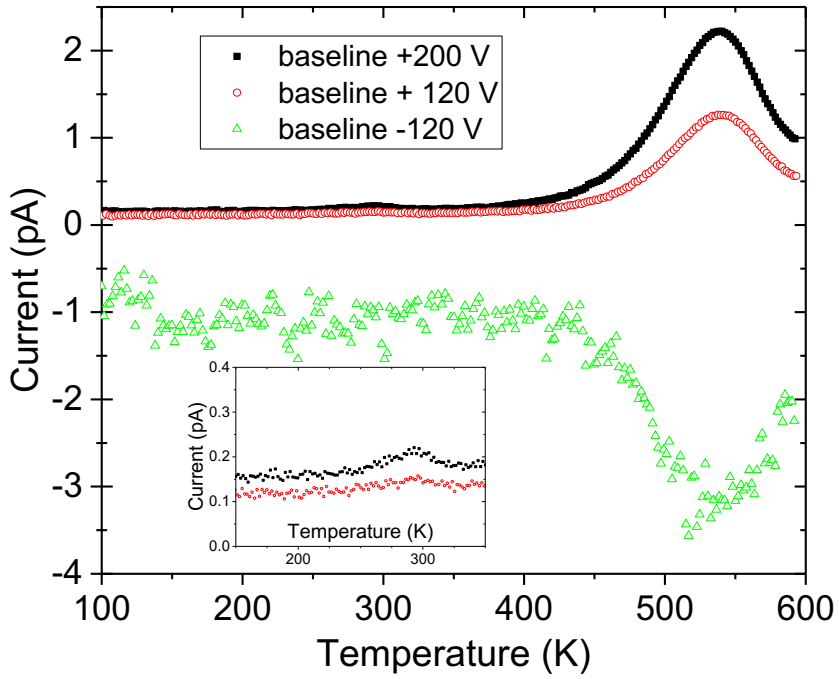

Figure 3 : TSIC baseline recorded under several gate bias V_G (-120V, +120 V and 200 V) after a trapping at high temperature under the same V_G. The inset is a zoom between 200 and 300 K.

Extracted parameters from these spectra are summarized in Table 1. Peak A gives an energy E ~ 0.67 eV and peak B an energy E ~0.78 eV. For $-V_G$ = 20 V, peak A does not appear, instead at 200 V peak A is higher than peak B. Up to ~100 V, the density of the charges which correspond with peak A and B is ~4×10^{11} cm^{-2}. This density increases upto 8×10^{11} cm^{-2} for $-V_G$ = 200 V. It is possible that for lower V_G value, the mobile ions have not been all trapped during the time the structure is heated at high temperature.

Table 1 : Parameters of observed TSIC peaks obtained during heating sweep with a rate = 0.2 Ks^{-1}. Positive (resp. negative) detrapping voltage ($-V_G$) corresponds to detrapping from G/ox (resp. ox/SiC) interface.

$-V_G$ (V)	80	120	200	-120
Peak A	T_{max} = 257 K $N_m = 3\times10^{11}$ cm^{-2}	T_{max} = 257 K $N_m = 2\times10^{11}$ cm^{-2}	T_{max} = 251 K $N_m = 8\times10^{11}$ cm^{-2}	
Peak B	T_{max} = 296 K $N_m = 5\times10^{10}$ cm^{-2}	T_{max} = 296 K $N_m = 2\times10^{11}$ cm^{-2}	T_{max} = 300 K $N_m = 6\times10^{10}$ cm^{-2}	T_{max} = 268 K $N_m=2.8\times10^{11}$ cm^{-2}
Peak C	T_{max} = 530 K $N_m = 4\times10^{12}$ cm^{-2}	T_{max} = 495 K $N_m = 9.5\times10^{12}$ cm^{-2}	T_{max} = 452 K $N_m = 6.7\times10^{12}$ cm^{-2}	T_{max} = 484 K $N_m=9.7\times10^{12}$ cm^{-2}
Peak D		T_{max} = 554 K $N_m = 5\times10^{12}$ cm^{-2}	T_{max} = 546 K $N_m = 7\times10^{12}$ cm^{-2}	T_{max} = 550 K $N_m = 8.8\times10^{12}$ cm^{-2}

Peak C and D show higher current, and they do not appear at low V_G value due to the temperature limitation of the cryostat. Peak C begins to appear at $-V_G$ = 80 V. Charge densities corresponding to peak C and D are found in the range 10^{12}-10^{13} cm^{-2}, as reported in Table 1.

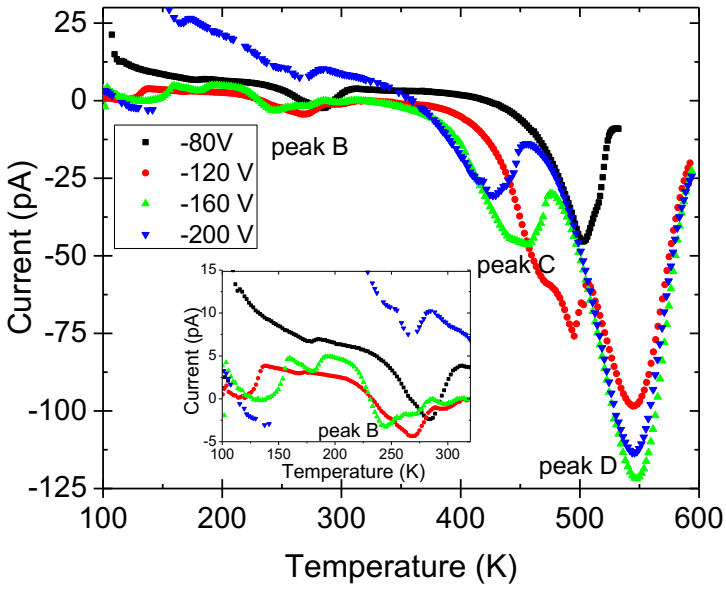

Figure 4 : TSIC spectra recorded under several detrapping gate bias $-V_G$ varying from -80 V to -200 V, after a trapping at high temperature under positive V_G. The observed peaks are due to detrapping at the ox/SiC interface. The inset is a zoom on the current between 200 and 350 K.

Figure 4 shows the spectra of the negative detrapping gate bias after trapping at high temperature. The detrapping curves shown in Figure 4 are similar with the trapping ones presented in Figure 2 for voltages below - 80V and above. The densities of mobile charges have been calculated for $-V_G$ =-120 V and are in the same range as the positive detrapping voltages.

For comparing our results with the published ones [10 and references therein], it is convenient to calculate the detrapping energy of mobile charges vs. the oxide electric field, and, if possible, its variation with ξ_{ox}. Detrapping energies have been calculated as detailed previously by solving (Eq.1) for each peak at every detrapping voltage. ξ_{ox} have been calculated using (Eq.2) with V_{FB} = -59 V, which is a reasonable assumption considering Fig.1 for measurements subsequent to a positive trapping voltage. After positive trapping voltage, ξ_{ox} have been calculated using V_{FB} = -100 V. For these high values, the main mobile charges have been indeed drifted to the ox/SiC interface and we can assume that the flatband voltage is at its minimum. The spectrum obtained with V_G = -80 V has not been used to determine the activation energy because it is not possible to evaluate correctly the electric field in the oxide, which probably is very low.

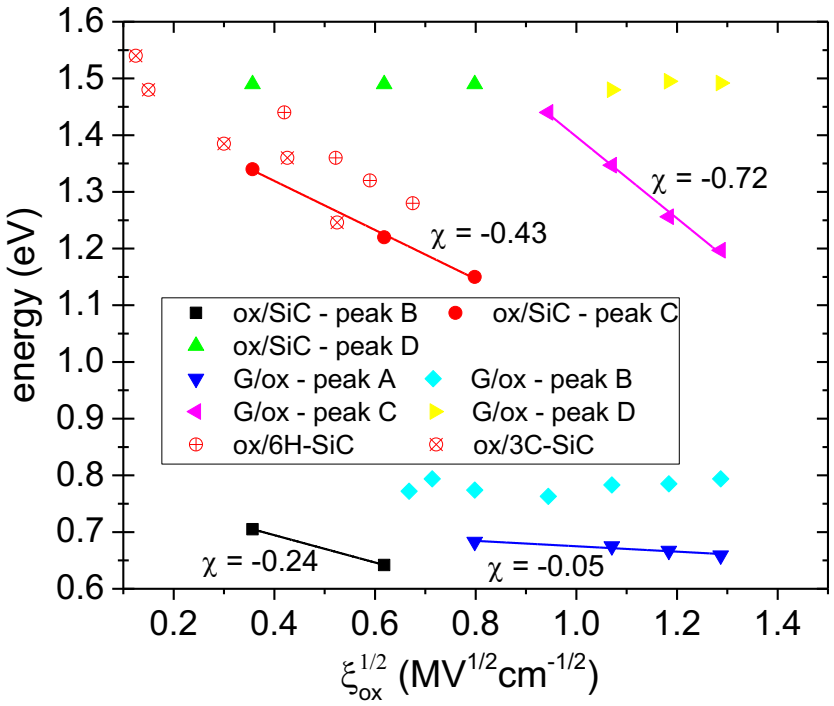

Figure 5 : Synthesis of the activation energies extracted from TSIC spectra for detrapping voltage – V_G > 0 (G/ox interface) and for –V_G < 0 (ox/SiC interface). Results from Ref. [10] for other ox/SiC interfaces (6H and 3C polytypes) are also shown for comparison.

For peak D, the activation energy is about 1.5 eV (for V_G = ±120, ±160 and ±200V) which is not dependent on gate voltage, i.e. on the electric field. It means that the traps that capture mobile charges are similar at the two interfaces (gate/oxide and oxide/semiconductor). For peak C, the detrapping energy is lower, i.e. in the range ~1.2eV and varies with the applied voltage, therefore with ξ_{ox}. Figure 5 shows the detrapping energies for the different observed peaks. The χ value obtained for peak C is -0.43 eV $MV^{-1/2}cm^{1/2}$ at the ox/SiC interface and -0.72 eV $MV^{-1/2}cm^{1/2}$ at the G/ox interface.

Peak B corresponds to a trap with an energy in the range 0.76 - 0.8 eV at the G/ox interface and 0.64-0.71 eV at the ox/SiC interface. The variation at the G/ox interface is not clear. Although, at the ox/SiC interface it seems to decrease with χ = -0.24 eV $MV^{-1/2}cm^{1/2}$.

Peak A is observed only at the G/ox interface with an energy similar to that of peak B at ox/SiC interface.

Previous studies [10] on thermal oxide grown on 6H- and 3C-SiC have shown that traps for mobile charges are similar in 6H-SiC, 3C-SiC and Si structures, therefore these interfacial traps are not fundamentally dependent on the interface. One of these trap energies was in the range 1.3-1.5 eV with χ ~-0.6 eV $MV^{-1/2}cm^{1/2}$, which is similar to the peak C at ox/SiC interface

The other peaks present no similar characteristics with the traps in 3C or 6H-SiC structures [10]. The difference may be due to the different nature of the oxide : i.e. thermally grown in Ref.[10] vs. deposited in our study. However, the presence of a thin interfacial thermally grown oxide can explain some of the similarities between trap C (ox/SiC face) and the one observed in [10].

Yet, the detrapping energy value depends on the traps nature, and it is probable that the value of χ depends also on the nature of trapped mobile charges. Therefore, it is worth to identify the physical

nature of the mobile charges that are presumably positive alkali ions. With this aim, SIMS measurements have been performed.

3.3. SIMS analyses

The presence of Na and K alkali ions was investigated by SIMS measurements, performed by EAG Laboratories, with a Physical Electronics Model 6600 equipment, using oxygen bombardment with positive-ion detection. The concentration detection limits are 10^{13} and 2×10^{13} atoms/cm^3 for K and Na species respectively. The SIMS depth concentration profiles of both Na and K within the SiO_2 passivation layer under study are shown in Figure 6. These profiles indicate clearly the presence of both species at the surface of the oxide layer, with concentrations above 10^{17} atoms/cm^3 close to the surface.

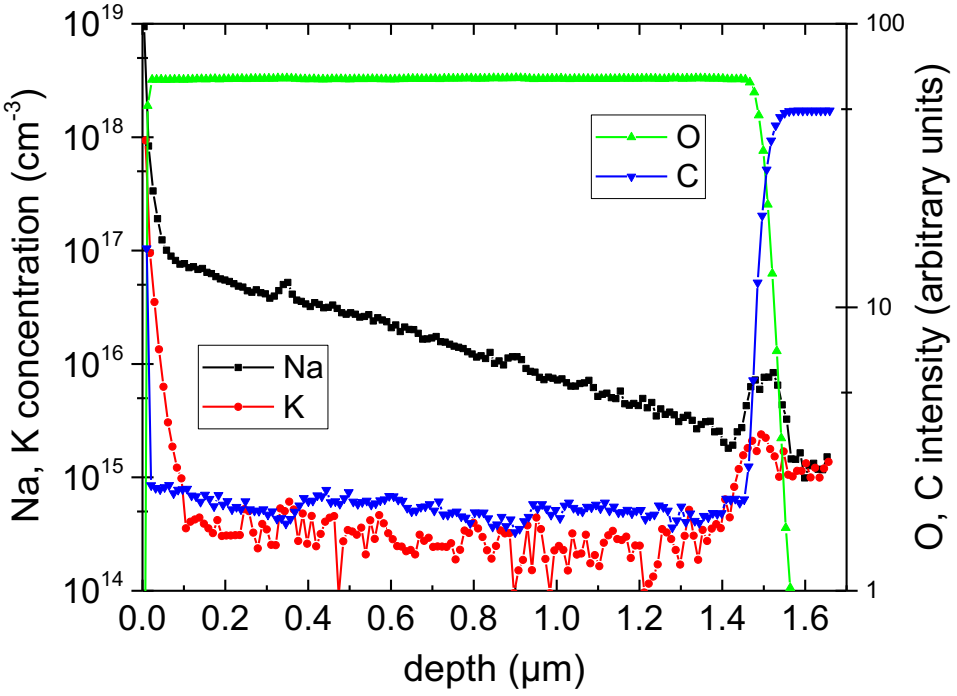

Figure 6 : SIMS depth concentration profiles of Na and K within the SiO_2 passivation layer. O and C intensities were monitored as marker species, and were not quantified as shown on right hand side y-axis.

A tailing of the Na profile through the silica layer, and a peak at the ox/SiC interface (~10^{16} atoms/cm^3) can be observed. However, the peak at the ox/SiC interface may be considered as an artifact of the SIMS measurement. Although, during the analysis an optimization was performed in order to minimize the Na migration impact. Compared to Na, a lower K concentration was observed into the depth of the oxide layer. The K concentration seems almost stable at ~3×10^{14} atoms/cm^3 up to the ox/SiC interface whereas a peak of ~2×10^{15} atoms/cm^3 can be seen. The K species are not as mobile as Na species during the measurement, which can reflect a more reliable concentration profile. In this case, an evaluation of the K ion dose present in the whole oxide layer was determined. Thus, a dose of 5.26×10^{12}atoms/cm^2 was derived from the SIMS profile (principally related to the surface region contribution). This dose value is similar with the charge densities values obtained for peaks C and D, as described above. As a result, the surface contamination by Na and K ions as determined by SIMS analysis seems to be the source of positive mobile ions involved in the results obtained by C-V and TSIC measurements.

4. Conclusion

Thermally stimulated ionic current measurements have been performed up to 200 V and 600 K in order to study the oxide interfaces traps in MOS structures fabricated with a thick oxide deposited by PECVD on n-type 4H-SiC epilayers. These thick oxides are not intended to realize gate oxide but to make passivation layers. SIMS measurements show the presence of K^+ and Na^+ species in a large concentration. TSIC spectra shows a detrapping of mobile ions in at least four kinds of traps, with energies at ~1.5 eV, 1.2-1.4 eV, and others between 0.6 and 0.8 eV. Note that one of these peak seems to be only present at the oxide/gate interface. These traps are different (energy values and their dependences with the electric field) from traps detected in thermally grown oxide on 3C and 6H-SiC epilayers, except for a trap observed at the ox/SiC interface (i.e. trap C). This difference can be due to the different oxide natures (deposited vs. thermally grown). On the other hand, the similarity at the ox/SiC interface can be due to the presence of a thin intermediate wet oxide.

5. Acknowledgment

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6. Data availability

The raw/processed data required to reproduce these findings cannot be shared at this time due to technical or time limitations.

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