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In-depth analysis of Electrical Characteristics for Polycrystalline Silicon Vertical Thin Film Transistors

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Abstract

A polycrystalline silicon vertical thin film transistor (VTFT) is fabricated, and the electrical parameters are extracted and compared with the typical lateral thin film transistor (LTFT). The similar subthreshold slope and the distinct field effect mobility is verified by the DOS calculation in the deep and shallow trap regions, respectively, and in this article, it is used to compare with the grain boundary trap density at a lower

$V_{ds}=10$ mV that eliminates the velocity saturation effect. The accurate threshold voltage is also calculated by a systematic model including the grain boundary barrier modulation effect. A pseudo-subthreshold region is demonstrated, and the threshold voltage exactly corresponds to the $3kT$ point of the grain boundary barrier. The low field effect mobility of VTFT is mainly due to the small grain size and also slightly affected by the parasitic resistance, which can be improved by optimizing the processing conditions, especially by improving the sidewalls smoothness and the active layer quality.

Key words: polycrystalline silicon, vertical thin film transistor, pseudo-subthreshold region, grain boundary barrier, density of states

I. INTRODUCTION

Recently, with the rapid development of all kinds of electronic devices, such as in flat panel display technologies [1] (especially in active matrix LCD [2], active matrix OLED [3] et. al.), in RFID tags [4], in random access memories [5], and in low-cost logic circuits [6], high-quality polycrystalline silicon thin film transistors have been put forward and adopted. For these applications, one research focused on the drive current optimization. In addition to the approach of increasing the field effect mobility by various processing methods such as laser crystallization [7], or metal-induced crystallization [8], another method is adopting short-

channel transistors. In order to seek this aim, thin film transistors with vertical configuration were adopted, where source and drain layers lie on top and at bottom of the stacked layers, and channel length is defined by the barrier layer thickness between source and drain, being independent of the photolithographic designing rule [9, 10]. This vertical configuration not only potentially enables a large drive current, but also potentially enables to increase the operating frequency by an inverse square relationship with the channel length [11].

In our optimized device configuration, the channel layer of the polycrystalline silicon vertical thin film transistor (VTFT) is deposited on top of the sidewalls formed by a plasma etching process [10]. Therefore, the dry-etched morphology of the sidewalls greatly affects the nucleation and growth of the active layer. In addition, the growth kinetics for the vertically deposited channel layer is unclear, which may be different from the growth kinetics of a lateral thin film transistor (LTFT). Usually, the electrical parameters are efficient quality factors of the VTFT electrical performance, such as the field effect mobility, threshold voltage, subthreshold slope. However, these parameters are prone to be affected by the grain boundary trap density [12] and the external parasitic resistance [13], which require more precise definitions. In this article, the research focuses on the effect of the grain boundary on the threshold voltage and the parasitic resistance extraction. Furthermore, in order to provide in-

depth analysis of the electrical performance, the effects of the grain boundary trap density and the total density of states (DOS) are shown, where the DOS of a VTFT is compared with the one of a LTFT in order to show the relevance between the electrical parameters and the DOS. Note that, in our previous publication [14], the DOS of VTFT and LTFT have been compared and analyzed, which studies the VTFT at a comparatively higher $V_{ds}=100$ mV, and the device with Si_3N_4 barrier layer is superior to the VTFT with SiO_2 barrier layer. In order to further avoid the short-channel effects and eliminate the velocity saturation effect and thus simplify the following analysis, the characterization based on lower $V_{ds}=10$ mV is adopted for the optimized VTFT with Si_3N_4 barrier layer, and the corresponding DOS of the VTFT is also shown and compared with a typical LTFT.

II. EXPERIMENT

The VTFT devices fabrication requires a five-mask process. Initially, the wafer substrates were cleaned by standard RCA cleaning steps. Then a thick SiO_2 buffer layer is formed by atmospheric pressure chemical vapor deposition (APCVD). Thereafter, the layers stacking incorporating source layer, 200 nm Si_3N_4 barrier layer, 1 μm undoped polycrystalline silicon layer, and drain layer are sequentially deposited by low pressure chemical vapor deposition (LPCVD) method. Afterwards, the stacked layers were firstly plasma-etched to form the sidewalls, and thereafter, another partial

dry etching is carried out to etch until reaching the bottom N-type heavily-doped layer to discriminate source and drain layers. Afterwards, a 300 nm undoped polycrystalline silicon layer is deposited on top by LPCVD and then it is patterned by a third mask. Prior to the gate oxide deposition, another RCA cleaning is carried out. And thereafter, a nominal 70 nm gate oxide layer is deposited by APCVD technique, which is then densified. After that, the gate oxide is etched by the fourth mask to show the source and drain contact holes. Finally, the source, drain and gate contact pads are formed by vacuum-depositing a thick aluminum layer and then patterned by a fifth mask and etched in etchant solution. More details on the VTFT fabrication process can be obtained in a previous published paper [10].

For the LTFT fabrication, a four-mask process is carried out. The substrates were cleaned, then a 300 nm thick polycrystalline silicon layer was deposited, with the bottom 150 nm thick undoped layer being the active layer, and the top 150 nm thick N-type heavily-doped layer being the source and drain layer. Firstly, the first partial etching was carried out to reach the bottom 150 nm undoped layer to define the channel, source and drain, then another dry etching was carried out to isolate TFTs. Then the gate oxide is deposited by APCVD, where the third mask is adopted and a wet-etching step is carried out to define the contact holes. Finally, a thick aluminum layer is deposited and patterned to define source, drain and gate contact pads. The detailed processing procedure of a LTFT can be

shown in Reference [15].

The electrical characterization of the fabricated devices is performed using an Agilent 1500A semiconductor parameter analyzer in ambient atmosphere.

Figure 1(a) shows the structure configuration of a four-channel VTFT, which consists of four sidewalls. It is shown that the source and drain are discriminated by a partial etching reaching the bottom heavily-doped source layer, and the channels are formed at the sidewalls. Figure 1(b) shows the plan view of the etched sidewalls. The sidewalls are quasi-vertical, and there are recesses at the Si_3N_4 layer. From the top view of figure 1(c), certain roughness is obtained after the plasma etching, which may greatly affect the nucleation and growth morphology of the active layer.

III. RESULTS AND DISCUSSION

The typical transfer characteristics of a two-channel VTFT are shown in figure 2(a), in order to evaluate the electrical performance quality of the VTFT, the typical transfer characteristics of a LTFT are also demonstrated. For the VTFT, the channel width/length ratio is approximately $40 \mu\text{m} / 1.2 \mu\text{m}$, and the drain-source voltage is fixed at a low value of 10 mV, in order to suppress short-channel effects. In contrast, for the LTFT, the channel width/length ratio is approximately $30 \mu\text{m} / 10 \mu\text{m}$, and the lateral electric

field is below the critical field. Note that, even 10 mV drain-source voltage and 1V drain-source voltage are adopted for VTFT and LTFT, respectively, the nearly same lateral electric field are obtained that enables the comparison. The inset of figure 2(a) shows the transfer characteristics in linear coordinates, due to the large difference of transfer curves for VTFT and LTFT, only the transfer characteristics of VTFT was demonstrated. From a typical VTFT measurement, the output characteristics show kink effect, which is due to the impact ionization in the pinch-off regime under high electric field for short-channel device.

From the transfer characteristics of VTFT and LTFT, different electrical parameters deduced from the simplified electrical model of the MOSFET [11] can be deduced and listed in table 1. Note that, the transconductance is related with the geometric parameters, therefore, the comparison is not rational and is not listed in the table. For LTFT, a much higher I_{on}/I_{off} ratio is obtained. The much larger field effect mobility of LTFT is mainly due to the large grain size of the LTFT active layer with smaller amounts of nucleation seeds as well as better growth kinetics. In contrast, the low mobility of VTFT is mainly due to the rough sidewalls that the active layer deposits on them, which provides abundant seeds that enables the nucleation of the grains, while the effect of the parasitic resistance may also contribute to the field effect mobility. In addition, the growth kinetics of the active layer in the vertical direction in VTFT is still

unclear, which may also limit the field effect mobility of VTFT. In the following context, the effect of the access resistance on the field effect mobility will be discussed. The similar threshold voltages and subthreshold slopes of LTFT and VTFT indicates approximately the same trap densities at the gate insulator/active layer interface, which will be elucidated in the DOS calculation for these two types of TFTs. From a gate bias stress test [16] for a reference device, the threshold voltage has been shifted from 3.06 V to 9.22 V at a gate bias stress of $V_{gs}=15$ V for 6 hours. Even though with a threshold voltage shift, the gate bias stress effect has been reduced beyond 5 hours, while the field effect mobility and the subthreshold slope also degraded due to the trapping effects. Nevertheless, the mobility and subthreshold slope vary slightly, which nearly does not affect the initial mobility and subthreshold slope. The threshold voltage of VTFT will also be discussed via a systematic grain boundary model, indicating the grain boundary barrier plays an important role.

For a systematic model considering the grain boundary barrier modulation effect on the effective mobility μ_{eff} , mobility degradation due to large gate electric field, and carrier velocity saturation effect, the drain current can be expressed as [17]:

$$I_{ds} = \frac{W}{L - V_d / E_{sat}} C_{ox} \overline{\mu_{eff}} (V_{gt} - \frac{1}{2} V_d) V_d \quad (1)$$

with

$$\frac{\mu_{eff}}{\mu_0} = \frac{\exp(-q\Phi_B / kT)}{1 + [\beta(V_{gt} - \delta V_d)]^v} = \mu_0 \frac{\exp[-H / (V_{gt} - \delta V_d)]}{1 + [\beta(V_{gt} - \delta V_d)]^v} \quad (2)$$

Where C_{ox} is the gate capacitance per surface unit, Φ_B is the average energy barrier at grain boundaries, the parameter H indicates the grain boundary barrier modulation effect, the parameter E_{sat} is the saturation field, the parameter β indicates the mobility degradation due to large gate electric field, δ is the fitting parameter of the potential correlative to the position, which is related to the location where the local effective mobility equals to the average effective mobility, and the exponent v is an empirical parameter, which is 1.6 for electrons, and 1 for holes. V_{gt} is the difference between the gate bias V_g and V_t , where V_t is the intrinsic threshold voltage deduced from C-V measurement. μ_0 is the intrinsic mobility without considering the surface scattering and the grain boundary modulation effect.

From another aspect, the drain current can also be expressed by [18]:

$$I_{ds} = \frac{W}{L} \mu_{eff} Q_{ch} V_d \quad (3)$$

Where Q_{ch} is the channel sheet charge density, and its relationship with the gate bias can be expressed as:

$$Q_{ch}(V_g) = \frac{1}{WL} \int_{V_{FB}}^{V_g} (C_{gc} - C_{gc,FB}) dV \quad (4)$$

Where C_{gc} is the gate to channel capacitance, and $C_{gc,FB}$ is the gate to channel capacitance at the flat band condition.

Therefore, the channel sheet charge density can be calculated by integrating the C-V curves from flat band voltage. The frequency of the C-V measurement is 100 KHz by default. In fact, the channel sheet charge density can also be expressed by:

$$Q_{ch}(V_g) = C_{ox}(V_g - V_t) \quad (5)$$

Therefore, the intrinsic threshold voltage V_t and the gate capacitance per unit area, C_{ox} , can be deduced from the $Q_{ch}(V_g)-V_g$ curve, as shown in figure 2(b). The deduced intrinsic threshold voltage for VTFT is -1.15V, and the gate areal capacitance is 50.36 nF/cm².

From formula 2, the intrinsic field effect mobility (μ_0) without considering surface scattering and the grain boundary barrier modulation parameter (H), can be deduced from $\ln(\mu_{eff})-1/[-(V_g - V_t)]$ relationship, as shown from figure 2(c). The deduced intrinsic field effect mobility is 7.66 cm²/V•s, and the parameter H equals to 11.47 V. In addition, it is necessary to mention that, with a large gate bias, the field effect mobility do not show deviation from the fitting line, indicating the mobility degradation due to gate bias can be negligible, which will simplify the further calculation.

Developed by the secondary-derivative method to trace the actual threshold voltage, the third-derivative method of I_d is demonstrated [17], i.e.,

$$\frac{d^3 I_d}{dV_{gt}^3} = 0 \quad (6)$$

Which brings about a formula:

$$AV_{gt}^2 - BV_{gt} + C = 0 \quad (7)$$

Where $A=3H+3(1-2\delta)V_d$

$$B = H^2 + 3HV_d + 6(1-2\delta)\delta V_d^2$$

$$C = \frac{1}{2}H^2V_d + 3\delta(1-\delta)HV_d^2 + 3(1-2\delta)\delta^2V_d^3$$

The analytic solution for the actual threshold voltage can be expressed as:

$$V_{th} = V_t + V_{gt} = V_t + \frac{B + \sqrt{B^2 - 4AC}}{2A} \quad (8)$$

V_{gt} is calculated to be 3.83 V, which is equal to the value of $\frac{H}{3} + \frac{V_d}{2}$.

Therefore, the actual threshold voltage is $V_{th}=2.68$ V. In order to validate the actual threshold voltage, a ratio method for threshold voltage extraction [19, 20] is demonstrated, as shown in figure 3(a), which gives a threshold voltage of approximately 5.26 V, and the calculated low-field mobility is approximately 5.51 cm²/V•s. Note that, the deduced threshold voltage of 5.26 V is very close to the value of 5.32 V deduced from the linear fitting method, and the low-field mobility is also close to the nominal value of 5.63 cm²/V•s deduced from the linear fitting method.

The two methods show values with a slightly difference, which may be due to the extraction accuracy of the ratio method is not assured, unlike the second-derivative method, which gives a derivative peak that enables to accurately determine the actual threshold voltage, the linear fitting method often shows deviations for different chosen regions. In addition, the

parasitic resistance may have an adverse effect on the threshold voltage and field effect mobility. In order to prove this, parasitic resistance calculations are carried out.

Initially, the classical extraction of the access resistance can be expressed as:

$$R_{\text{total}} = \frac{V_d}{I_d} = R_{\text{para}} + \frac{1}{\frac{W}{L} C_{\text{ox}} \mu} \cdot \frac{1}{V_g - V_{th}} \quad (9)$$

This method does not consider the spreading resistance that varies with the gate bias, and the chosen V_{th} is 5.32 V, which is deduced from the linear fitting method. From figure 3(b), the deduced parasitic resistance (R_{para}) is 281.9 Ω . In order to further study the effect of the parasitic resistance on the threshold voltage, another systematic model that clearly assigned the grain boundary barrier modulation effect is also shown [22]:

$$R_{\text{total}} = \frac{V_d}{I_d} = R_{\text{para}} + \frac{1}{\frac{W}{L} C_{\text{ox}} \mu} \cdot \frac{\exp(H / (V_g - V_t))}{V_g - V_t} \quad (10)$$

For the extracted intrinsic threshold voltage V_t of -1.15V, the parasitic resistance is deduced to be 508.5 Ω . In order to further clarify the relationship between the threshold voltage and the parasitic resistance, the threshold voltage V_{th} of 5.32 V deduced from the linear fitting method is also adopted, and the obtained parasitic resistance is approximately 2048.8 Ω . In addition, the mobility has been increased by adopting the threshold voltage of 5.32 V. Therefore, both of the threshold voltage and the field effect mobility are influenced by the parasitic resistance. In fact, the

transmission line method to calculate the access resistance is also adopted, which shows a negative series resistance at the cross point of approximately 240 μm channel width, indicating the improper usage of the transmission line method. In addition, the frequency dependent response test had also been carried out [21], with a 3dB cut-off frequency of approximately 4.2 KHz.

From the above analysis, there is a pseudo-subthreshold region between the actual threshold voltage V_{th} and the intrinsic threshold voltage V_t corresponding to the appearance of the electrons in the channel layer, and the region width is approximately $\frac{H}{3} + \frac{V_d}{2}$. In other words, the actual threshold voltage is modulated by a grain boundary barrier, and the subthreshold current is dominated by the thermionic emission between adjacent grains by passing through the grain boundary barrier, as shown in the sketch view of figure 4(a). In fact, from the relationship between the gate bias V_g and grain boundary barrier Φ_B shown as following:

$$I_{\text{ds}} = \frac{W}{L} C_{\text{ox}} \overline{\mu_{\text{eff}}} (V_g - V_t - \frac{1}{2} V_d) V_d \quad (11)$$

$$\overline{\mu_{\text{eff}}} = \mu_0 \exp(-q\Phi_B / kT) \quad (12)$$

the $3kT$ point of the grain boundary barrier exactly corresponds to the actual threshold voltage of 2.68 V (Fig. 4(b)), indicating that the thermionic emission dominates the subthreshold current.

The grain boundary trap density is calculated based on the following

formula [18]:

$$N_t = \sqrt{\frac{8\epsilon_s C_{ox} (V_g - V_t) \Phi_B}{q^2 t}} \quad (13)$$

Where Φ_B is the grain boundary energy barrier, and t is the inversion layer thickness (which is chosen as 10 nm [23]). Figure 4(c) shows the relationship between the grain boundary barrier and the grain boundary areal trap density per unit electron volt, and it is shown that there is a transition at around $3kT$, below which the trap density increases sharply. In addition, with increasing the grain boundary barrier, the trap density also increases.

From another aspect, the density of states (DOS) of both LTFT and VTFT are calculated [24], as shown from figure 4(d). It is shown that, in the deep trap region (especially $E-E_F < 0.15$ eV), VTFT and LTFT show almost the same density, which verifies that the subthreshold slopes of VTFT and LTFT are almost the same. In contrast, in the shallow trap region, VTFT shows much larger DOS than LTFT. On the one hand, for the same $E-E_F=0.39$ eV, the LTFT shows a DOS of approximately 10^{20} eV⁻¹•cm⁻³, while for VTFT, this value is approximately 10^{23} eV⁻¹•cm⁻³, indicating the reduced number of traps for LTFT, which is beneficial for charge transport. On the other hand, for a gate bias of 30 V, the VTFT shows a smaller band bending, the $E-E_F$ reaches approximately 0.39 eV, while the $E-E_F$ is approximately 0.47 eV for LTFT even with a smaller gate bias of 20 V

from the relationship between the gate bias and the $E-E_F$ calculation according to reference [24]. The enlarged $E-E_F$ value for LTFT enables better transport, as the energy states are closer to the mobility edge, which is verified by the enlarged field effect mobility of LTFT. It is also noteworthy to mention that the E_F is not pinned at higher gate bias, indicating that it is possible to further increase the field effect mobility.

In practice, the deep and shallow traps correspond to the dangling bonds and the strained bonds, respectively, and two types of density distributions are shown, i.e., the Gaussian distribution with a maximum near the midgap, and the exponential band tail states near the mobility edge [25]. From the grain boundary trap density, the Gaussian distribution is clearly observed. In contrast, for our DOS calculation, the exponential band tail states can be clearly shown, while the Gaussian distribution with a maximum near the midgap is not shown, which may be due to that DOS calculation method does not discriminate interface states along the channel from defects located at the grain boundaries.

In addition, in order to improve the mobility of the VTFT, one way is to form better sidewalls by optimization the dry etching process and a post-processing, such as a further wet etching process. The other approach is by another crystallization method, such as the metal-induced lateral crystallization (MILC) [26], which has been adopted in lateral thin film transistor and shows large enhancement in field effect mobility.

IV. CONCLUSION

We fabricated polycrystalline silicon VTFT, and the electrical parameters are extracted and compared with LTFT, the similar subthreshold slope indicates similar deep trap density, and the much smaller field effect mobility of VTFT indicates the large DOS in the shallow trap region, which are verified by DOS comparison for the two types of TFTs. Note that, different from our previous work, the optimized VTFT with Si_3N_4 barrier layer is adopted and characterized at a lower drain-source voltage of 10 mV, in order to suppress the short channel effect and simplify the analysis. From C-V measurement, an accurate model that incorporates the grain boundary barrier modulation effect is introduced, which is also very close to the extracted threshold voltage value by ratio method that suppressed the parasitic resistance. The accurate model shows a pseudo-subthreshold region representing the thermionic emission through grain boundary barrier. The DOS and the grain boundary trap density is compared, which shows gaussian distribution for the grain boundary trap density in the deep trap regime and interface states as well.

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Data Availability Statements

The data that supports the findings of this study are available within the article.

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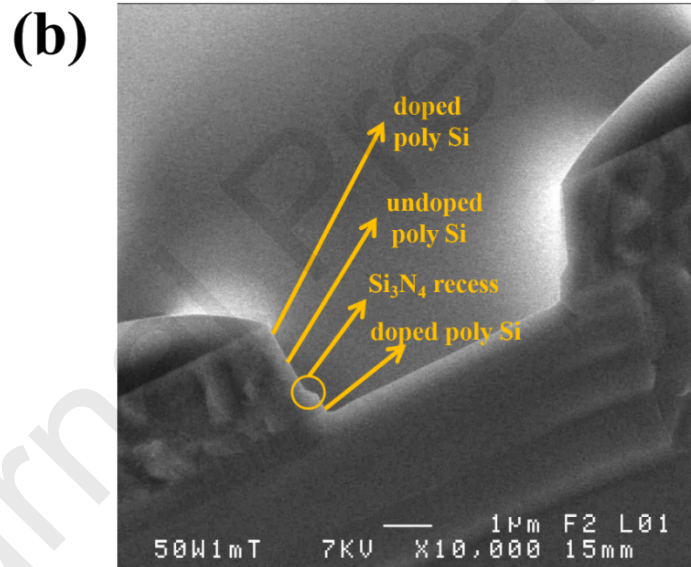
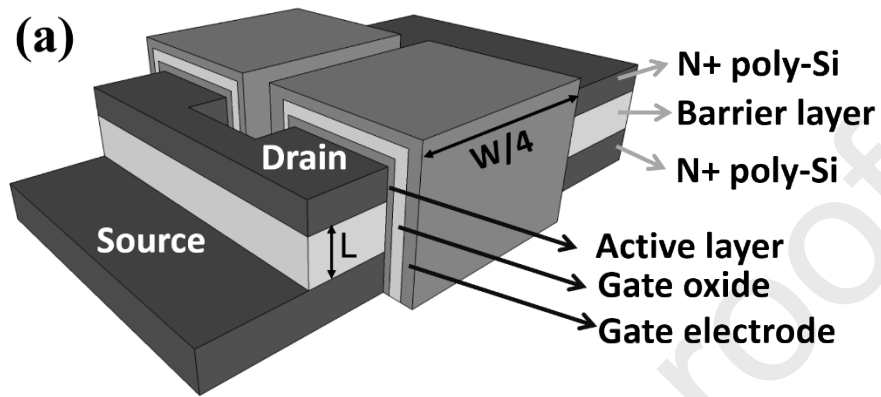
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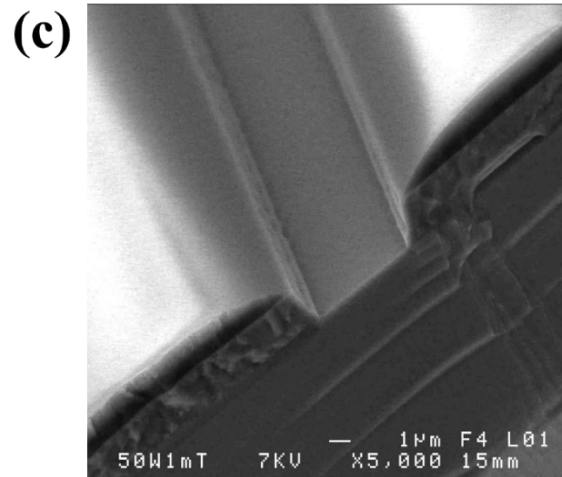
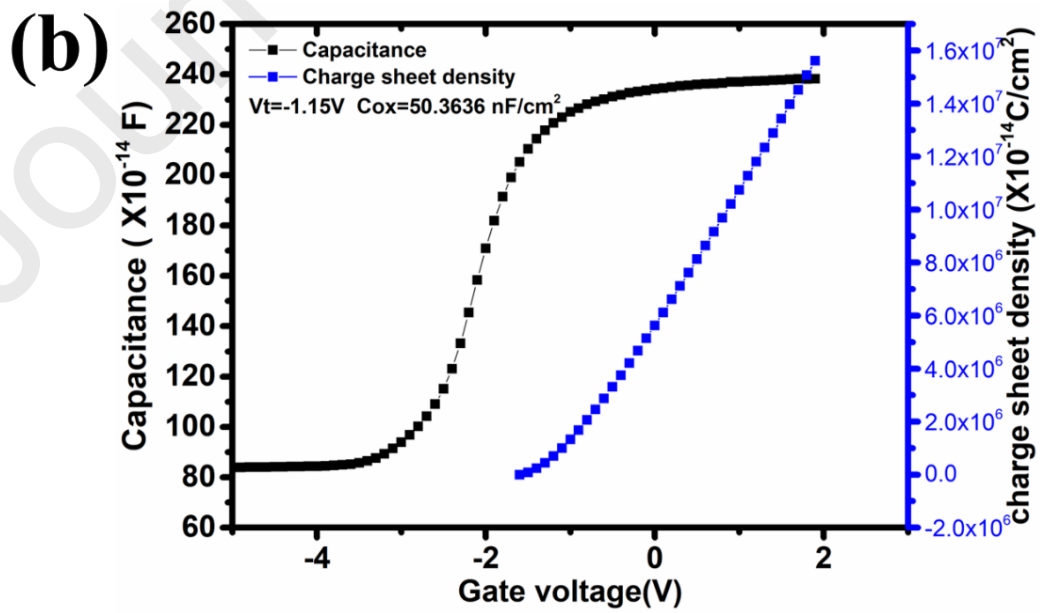
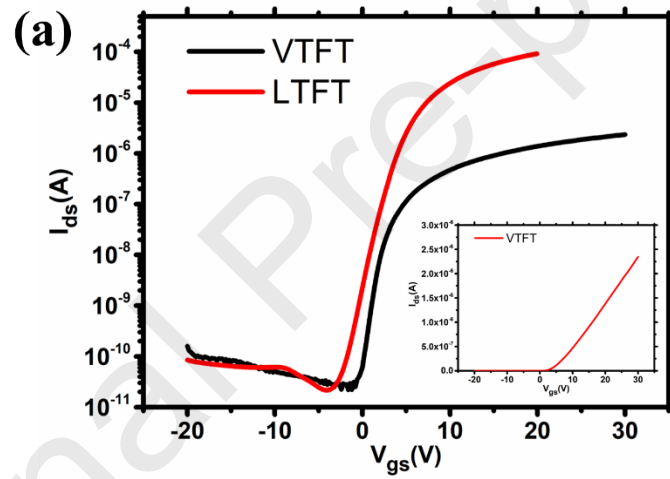


Figure 1: Structures of the fabricated devices, (a) the structure configuration of a two-tooth VTFT, there are four channels at the sidewalls, where L is the channel length, and W is the total width of the channel, (b) plan view of the etched sidewall, a vertical sidewall is formed, however, there are recesses at the Si_3N_4 layer, (c) top view of the etched sidewall, the etched sidewalls show certain roughness.



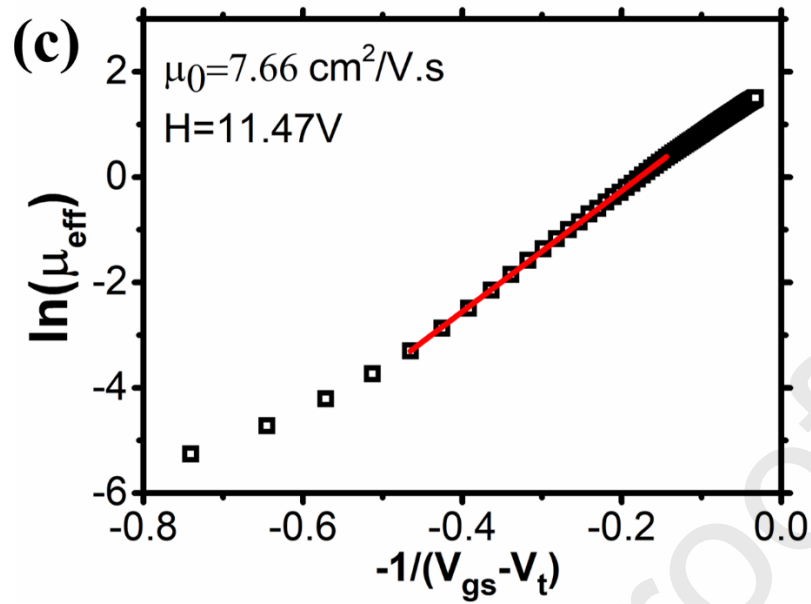
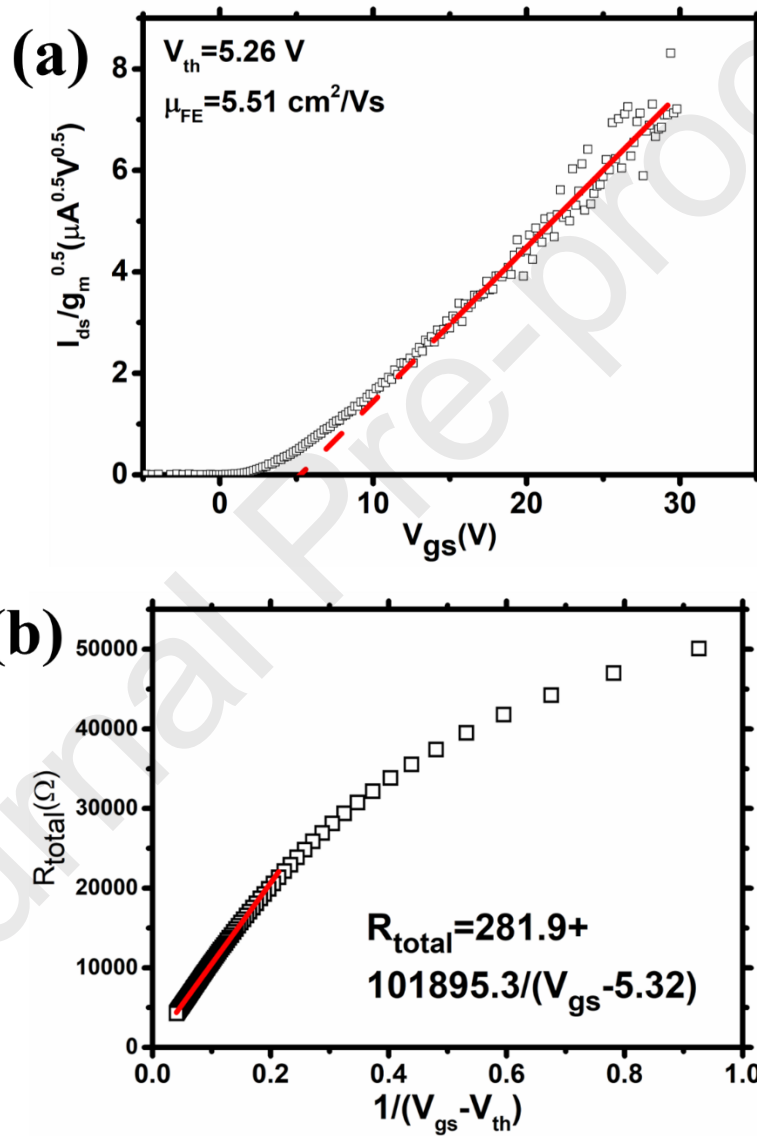


Figure 2: (a) transfer characteristics of the LTFT and VTFT, LTFT shows a much higher $I_{\text{on}}/I_{\text{off}}$ ratio, inset shows the transfer characteristics of VTFT in linear coordinates, (b) gate capacitance and channel charge sheet density for VTFT, the intrinsic threshold voltage and gate capacitance per unit area can be deduced, (c) the relationship between logarithm mobility and the gate bias, no mobility degradation is observed under high gate bias.

Table 1: Electrical parameters for VTFT and LTFT.

Type	V_{ds} (V)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	V_{th} (V)	SS (V/dec)	μ_{FE} ($cm^2/V \cdot s$)
VTFT	0.01	2.345×10^{-6}	2.20×10^{-11}	1.066×10^5	5.32	1.21	5.63
LTFT	1	9.196×10^{-5}	2.15×10^{-11}	4.28×10^6	6.54	1.3	65.9



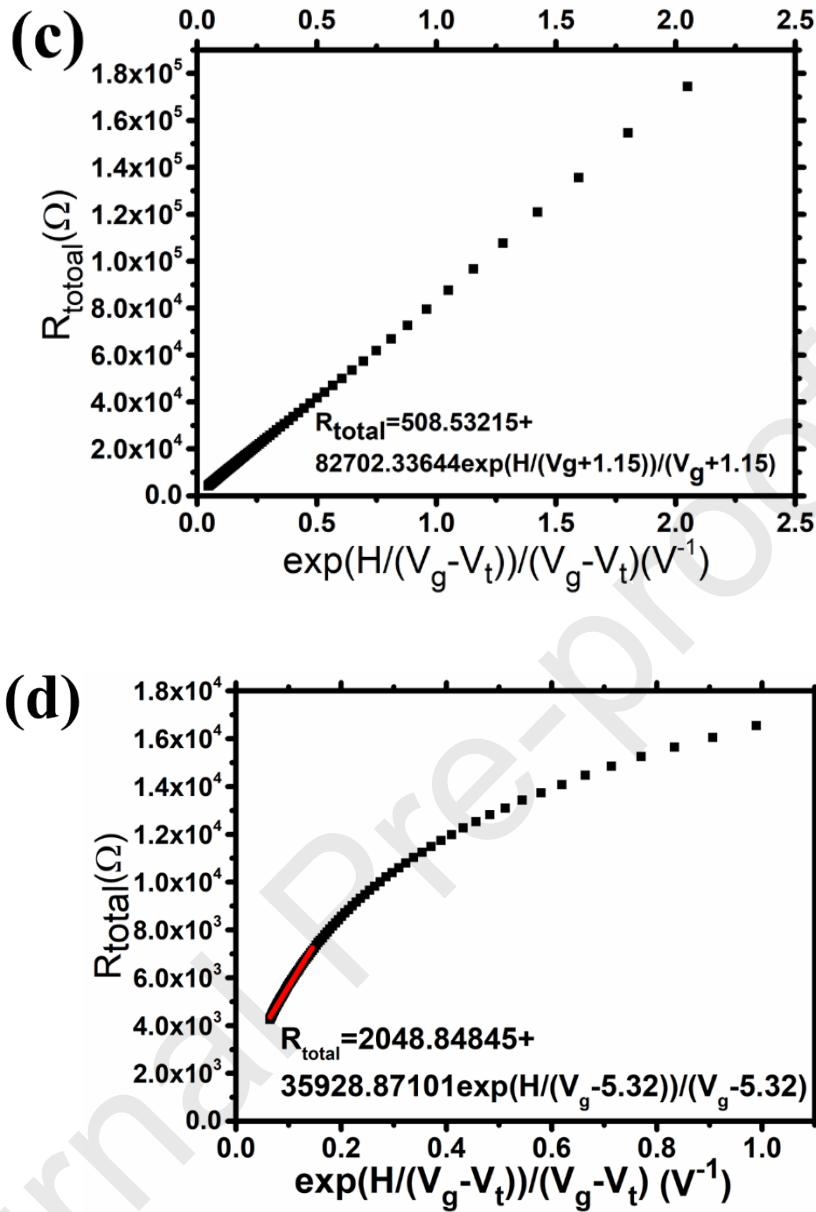
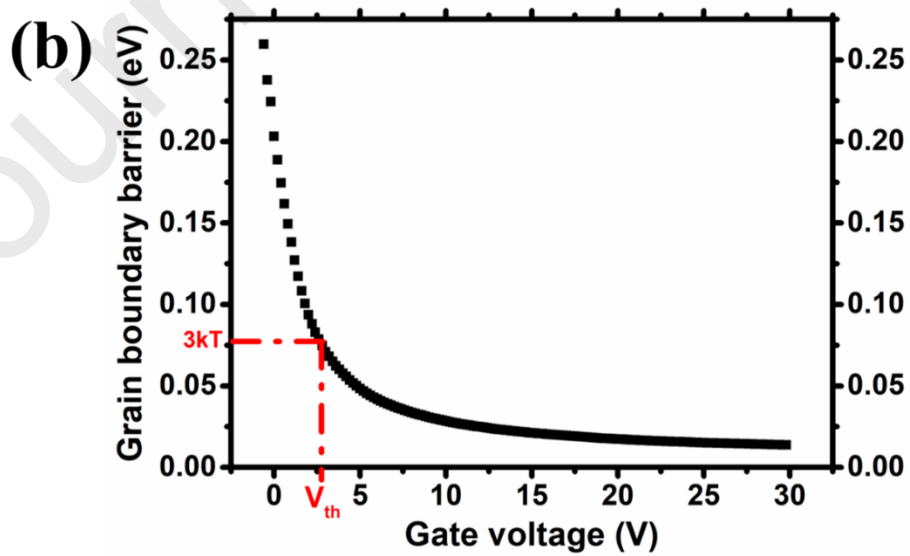
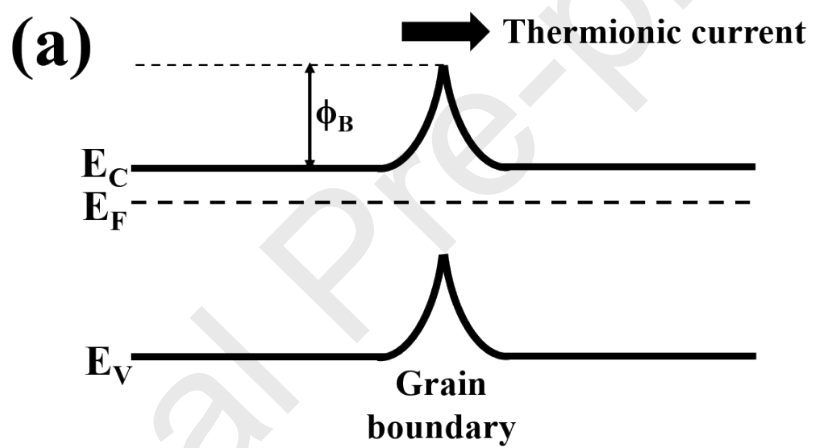


Figure 3: (a) the ratio method to determine the threshold voltage, and the deduced value is 5.26 V, and the low-field mobility is $5.51 \text{ cm}^2/\text{V}\cdot\text{s}$, (b) the parasitic resistance deduced from the classical method, which shows a parasitic resistance of 281.9Ω , (c) the parasitic resistance deduced from the new method, with the threshold voltage of -1.15V , the parasitic resistance is approximately 508.5Ω , (d) the parasitic resistance deduced from the new method for compare, with an increased threshold voltage of

5.32 V, the access resistance increases to 2048.8 Ω .



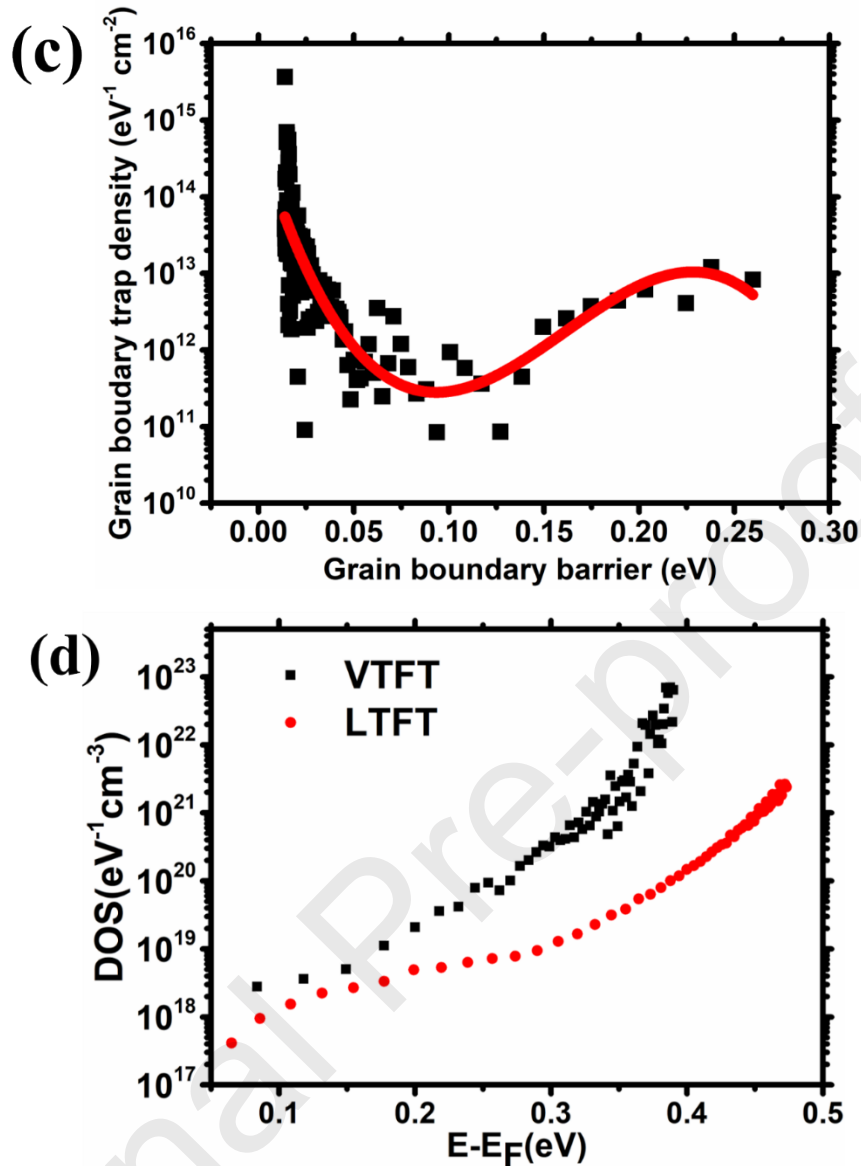


Figure 4: (a) the energy diagram of adjacent grains, the grain boundary barrier is demonstrated, (b) the relationship between gate bias and grain boundary barrier, the $3kT$ barrier corresponds to the threshold voltage calculated from the model, (c) the grain boundary trap density distribution, where there is a transition approximately at the threshold voltage, and (d) the DOS calculation for VTFT and LTFT, which shows similar deep densities and distinct shallow densities.

Declaration of interests

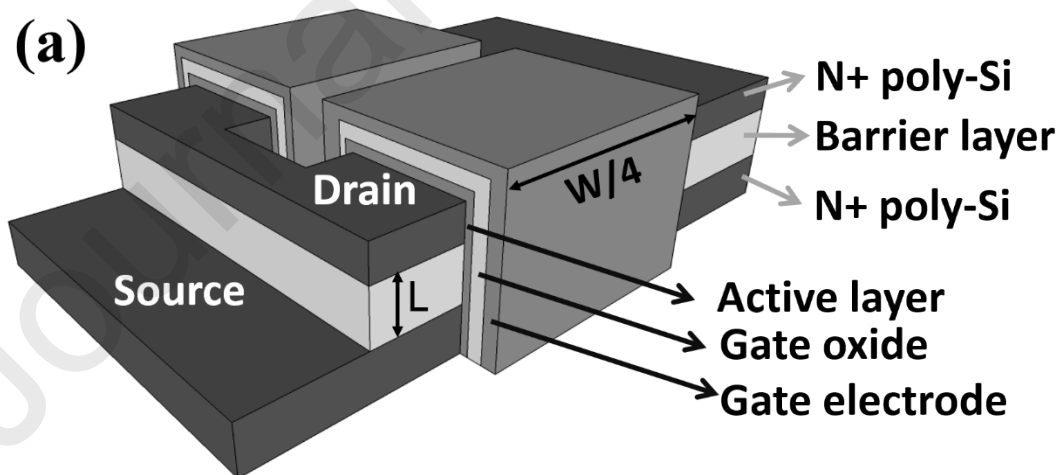
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

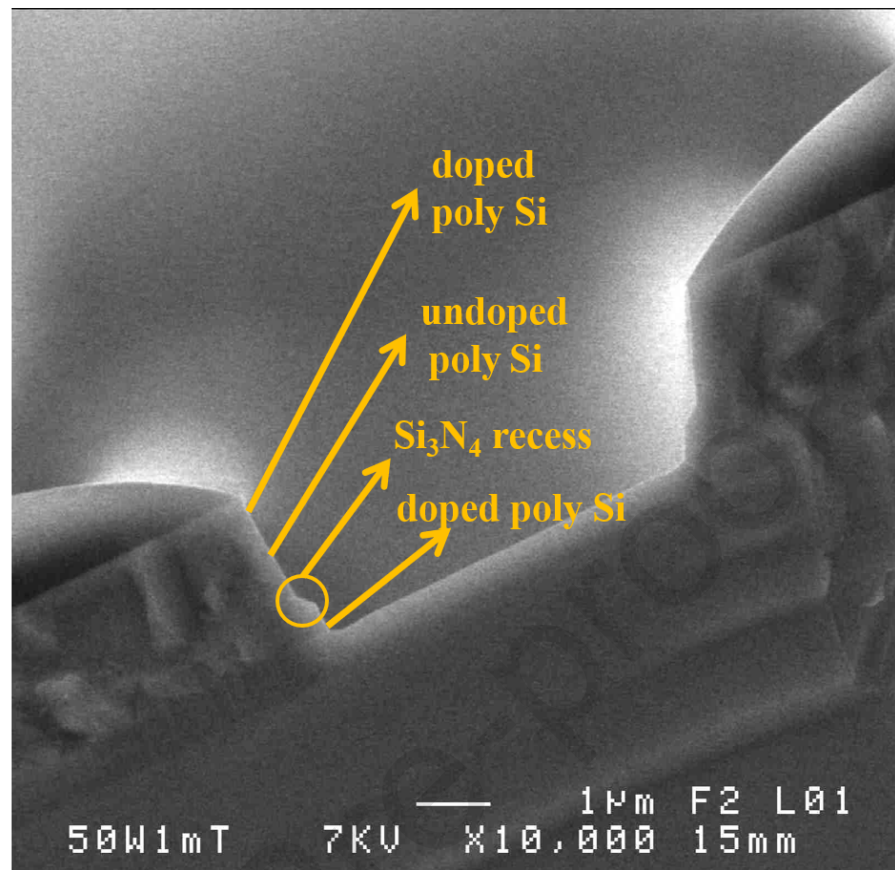
The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

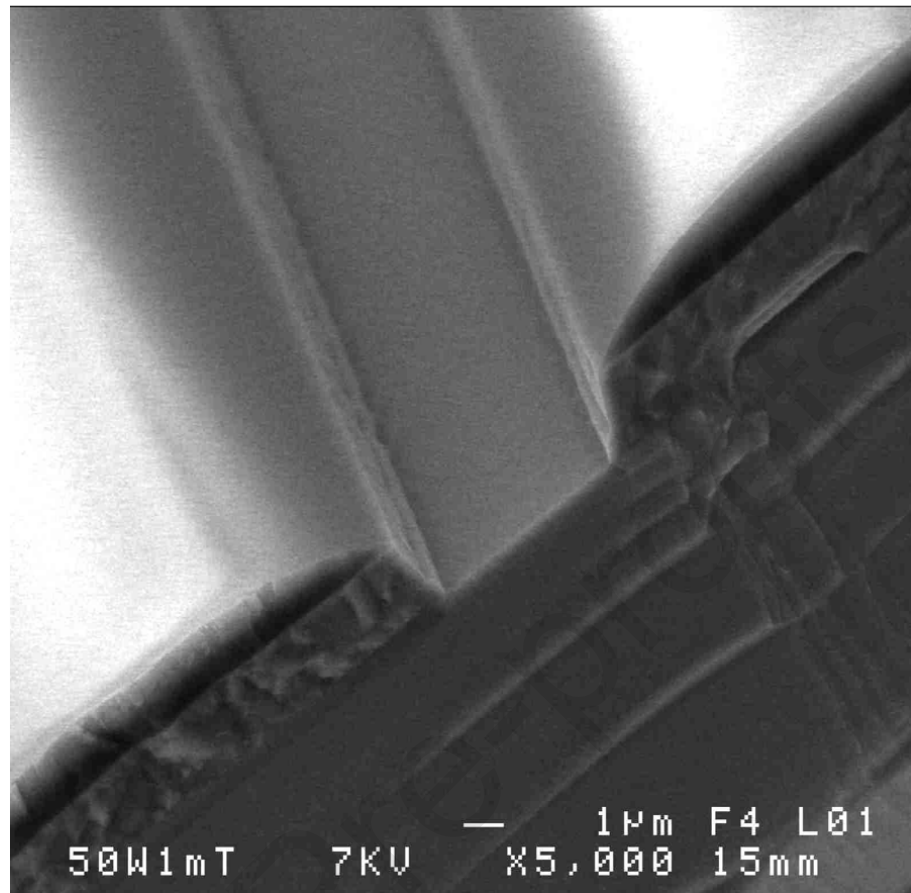
1. The transfer characteristics of VTFT and LTFT are demonstrated and explained via density of states;
2. The systematic model including grain boundary barrier effect is demonstrated and show a pseudo-subthreshold region;
3. Parasitic resistance measurement shows little effect on field effect mobility, and the field effect mobility of VTFT is mainly due to the small grain size.

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(b)

(c)**(a)**