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Keywords

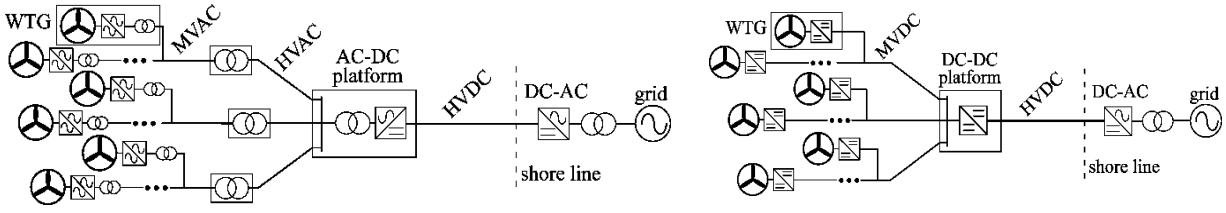
« Real time simulation », « DC collector network », « Renewable energy systems », « Modelling», « Test bench », « Emerging topology », « Hardware (not only Software) », « Converter control».

Abstract

The paper describes the development of a power converter small scale mock-up and a real time model of an off-shore wind farm. A Power Hardware In-the-Loop validation is proposed for a demonstration of grid architecture and control principles. The paper presents the design methodology of the PHIL test bench and underlines the contribution of PHIL in the design flow of power converter development for DC grid application. Experimental results of preliminary PHIL tests are presented.

Introduction

Renewable energy sources have become a key element of the policies to fight climate change worldwide. Wind energy has developed fast over the last decade and for example in Europe it has overtaken coal as the second largest form of installed generation capacity in 2016 [1]. Allowing the use of larger turbine sizes and with stronger and steadier winds, very large wind farms are feasible offshore. The large distances from the shore and the use of submarine cables make HVDC an ideal candidate for their grid integration [2]. With the goal of reducing the cost of the produced energy and lower the risk of commissioning such large projects, alternative ways of implementing the electrical connection of the farms are continuously explored. One such proposal is the offshore DC collector concept, where the standard MVAC grid of the wind farm (Fig. 1 (a)) is replaced by its MVDC counterpart [3]. As a result, two new DC-DC converters are required to step the voltage to MVDC levels at the wind turbine generators (WTG) and to HVDC levels at the offshore platform (Fig. 1 (b)) [4], [5].



a. AC collector b. DC collector

Fig. 1 – Offshore wind farm with AC collector vs DC collector

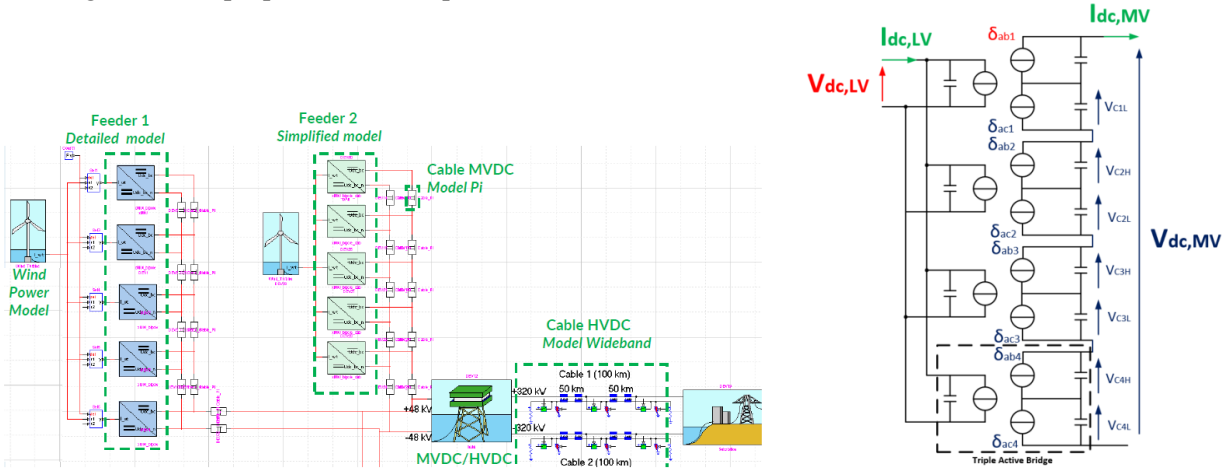
In [6], a new modular DC-DC converter was proposed to step-up the voltage inside the WTG to MVDC levels of ±50 kV to form the offshore DC collection grid. The basic building block of this converter is the Triple Active Bridge (TAB) cell with a voltage conversion ratio of 4 kV to 8 kV and a nominal power of 800 kW. Using the input parallel output series (IPOS) connection of 12 cells results in the required DC-DC converter to step-up the voltage to ±50 kV and a total power rating of 10 MW.

The testing of the full scale prototype of one building block (a cell) reported in [6] is complemented with a small scale mock-up (SSMU) of the DC-DC converter with several cells. This SSMU is connected via power amplifiers to a real time simulator which simulates the behavior of other wind turbines, other converters and cables of the wind farm. In this way a Power Hardware In-the-Loop (PHIL) setup is built. This allows to test the converter operation with the realistic constraints imposed by the wind turbines and HVDC transmission, as it can be done for other applications as railway [7]. For the control, a rapid control prototyping (RCP) approach was used. The model-based design applied to converter development facilitates the step-wise process including: off-line simulations, real time target implementation, automatic code generation and commissioning of small-scale and full-scale prototypes.

Real time model for offshore wind farm

System Modeling

A PHIL validation passes firstly by a real time implementation of the simulated circuit. In this work, the real time target "OP5700" with the software Hypersim are used.
The whole power system with 90 wind turbines, 10MW each, is designed using a technical and economical optimization algorithm [8]. During each simulation fixed time-step, the mathematical functions and equations representing the system are solved successively. Since the chosen time-step needs to be as small as possible for accuracy matters, the system requirements introduce a big modelling challenge. For this purpose, some simplifications are introduced to the simulated circuit.



a. b.

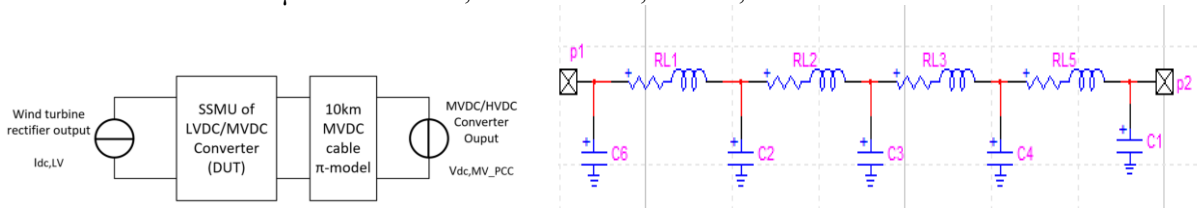
Fig. 2 - Hypersim real time model for offshore wind farm (a) ; reduced order averaged model of the LVDC/MVDC converter with 4 cells (SSMU) (b)

Considering that the offshore generators are controlled in power control mode, they are represented with DC current sources. On the other hand, the onshore converter is represented with a DC voltage source since this converter is controlled in voltage control mode [9]. In addition, the converter MVDC/HVDC has been modeled as an ideal current transformer with a fixed ratio (ratio between input and output DC voltages) with capacitors on both sides. The voltage can be regulated for one side by adapting the current flow. For connection links, PI model has been chosen to model the MVDC cables where the HVDC ones are represented using wideband model.
For the LVDC/MVDC converter, the reduced order averaged model (ROAM) is used. This modeling approach can be applied by neglecting the dynamics of the AC stage where f=20 kHz. Considering only one TAB converter cell, the ROAM is represented with three current sources controlled by the phase shift (see Fig. 2 (b) for 4 TABs).

Simplified model

One step in the PHIL workflow consists of the validation of the device under test (DUT) and of the stability of the PHIL setup using a simplified model.
For the preliminary PHIL tests, the DUT is a small scale mock-up of the LVDC/MVDC converter and the real-time model includes:

- The MVDC/HVDC converter output modelled as a perfect voltage source
- The wind turbine generator and its rectifier modelled as a perfect current source
- The cables between the MVDC/HVDC converter and the LVDC/MVDC converter. They are modelled as PI model cables as shown on Fig. 3 (b) for a distance of 10km with RL1 = RL2 = RL3 = RL5 = 25µH - 50mΩ/km; C1 = C6 = 12,5nF/km; C2 = C3 = C4 = 25nF/km.



a. b.

Fig. 3 – (a) Simplified real time model for PHIL tests ; (b) PI model of the MVDC cable in Hypersim

Small Scale Mock-Up of the LVDC/MVDC power converter for PHIL

A small scale mock-up of the power converter was developed in order to validate the topology and control of the DC-DC converter. Two constraints were taken into account in order to satisfy the dynamic behavior as close as possible between the full scale mock-up (FSMU) and the small scale mock-up (SSMU). First, the control interface was kept identical. Second, the methodology of scaling used for the power circuit was to keep the same electrostatic and magnetic time constants between the SSMU and the FSMU. The electrostatic time constant T_e, is used to size the capacitances and the magnetic time constant T_m, is used to size the leakage inductance of the transformer.

$$\frac{E}{P} = \frac{[\mathrm{J}]}{[\mathrm{J}] \cdot [\mathrm{s}]^{-1}} = [\mathrm{s}] \tag{1}$$

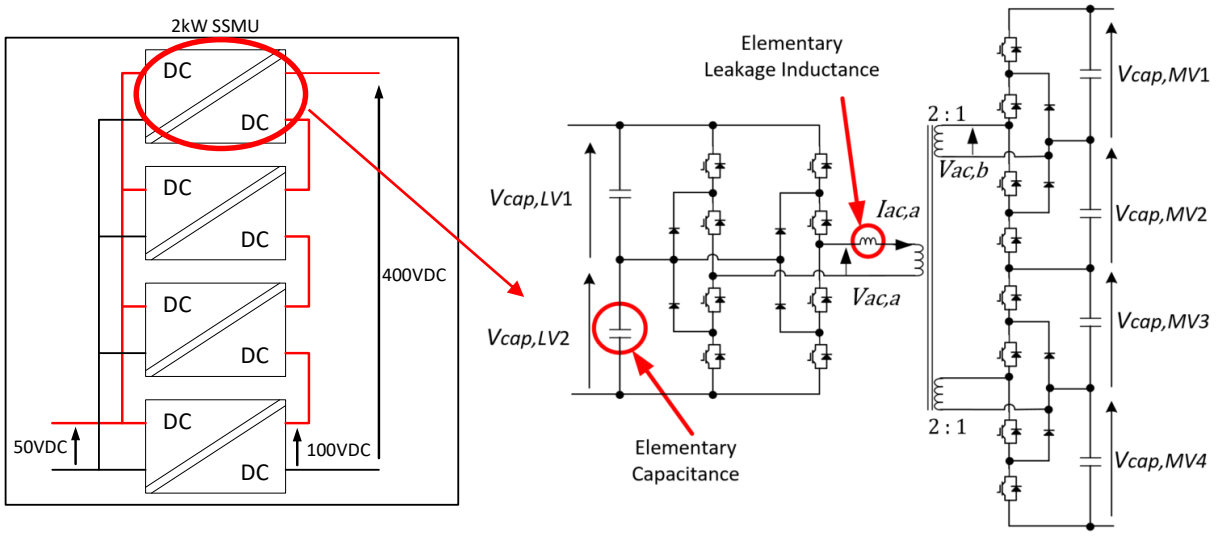
$$T_e = \frac{\frac{1}{2} C_{eq} V^2}{P} \tag{2}$$

$$T_m = \frac{\frac{1}{2} L_{eq} I^2}{P} \tag{3}$$

Therefore, the values of power, voltage and current can be adjusted to be compatible with the external system. Then, the scaled values of capacitance and inductance are calculated by first calculating the time constants T_e and T_m using the FSMU parameters (Power, Voltage, and Current) in the equations (2) and (3) and in a second time using T_e and T_m with the SSMU parameters, by inverting the equations (2) and (3).

For the purpose of integration in the PHIL platform, the ratings of the SSMU are defined as: 2kW, 50VDC input, 400VDC output and 4 cells. Therefore, the values of the elementary DC-link capacitance and of the leakage inductance of the transformer, identified in Fig. 4 (b) are calculated.
The choices and the results are summarized in Table I and illustrated in Fig. 4 (a).

At first, one cell of the converter has been implemented and tested in order to validate the hardware and the control principles. The 20kHz – 820VA medium frequency transformer has been custom-made in order to have the leakage inductance specified by the scaling method presented above. The control has been implemented using Matlab/Simulink automatic code generation and Speedgoat real time target.



a. b.

Fig. 4 - DC-DC converter diagram (a); NPC TAB cell diagram (b)

Table I: Results of the scaling process

Parameter	Value FSMU	Value SSMU	Justification
Output Voltage, converter ($V_{dc,MV}$)	50kV DC	400V DC	Compatibility with PHIL Platform
Output Voltage, cell	8kV DC	100V DC	Consequence of the quantity of cells
Input Voltage ($V_{dc,LV}$)	4kV DC	50V DC	Consequence of the transformation ratio
Power Rating of the converter	5MW	2kW	Compatibility with PHIL platform
Elementary DC-link capacitance	90µF	290µF	Scaling calculations
Transformer leakage inductance	30µH	9,6µH	Scaling calculations

Power Hardware In-the-Loop setup

In this section, the SSMU is tested in PHIL environment. As it was introduced before, this experience consists in combining a virtual environment simulated on a real time target with a real hardware [10], [11], in our case the SSMU of the DC-DC LVDC/MVDC converter. To do so, analog inputs and outputs are used to exchange signals between the real time simulation and the hardware, as illustrated in Fig. 7 [12], [13]. Since the SSMU is a 50VDC-400VDC 2kW device, two amplifiers are required to adapt current and voltage levels.

The interface of the PHIL setup is presented in Fig. 6 and Fig. 7 where Fig. 6 presents the position of the SSMU in the entire wind farm real time model and Fig. 7 presents the signals exchange interface with the simplified real time model. It has been considered that the input current $I_{dc,LV}$ is imposed by the wind turbines and the voltage bus V_{dc,MV_PCC} is controlled at the point of common connection (PCC). However, since the MVDC cable is taken into account, $I_{dc,LV}$ and $V_{dc,MV}$ are the signals sent from the real time system (RTS) to the device under test (DUT) where $V_{dc,MV}$ is the voltage at the MV terminals of the LVDC/MVDC converter (see Fig. 8). At the same time, $V_{dc,LV}$ and $I_{dc,MV}$ are measured at DUT terminals in order to send them back to the real time simulation to "close the loop for PHIL": $I_{dc,MV}$ measurement is injected in the PI-model cable. Therefore, amplifiers must be able to source and sink current and voltage (4Q power amplifiers).

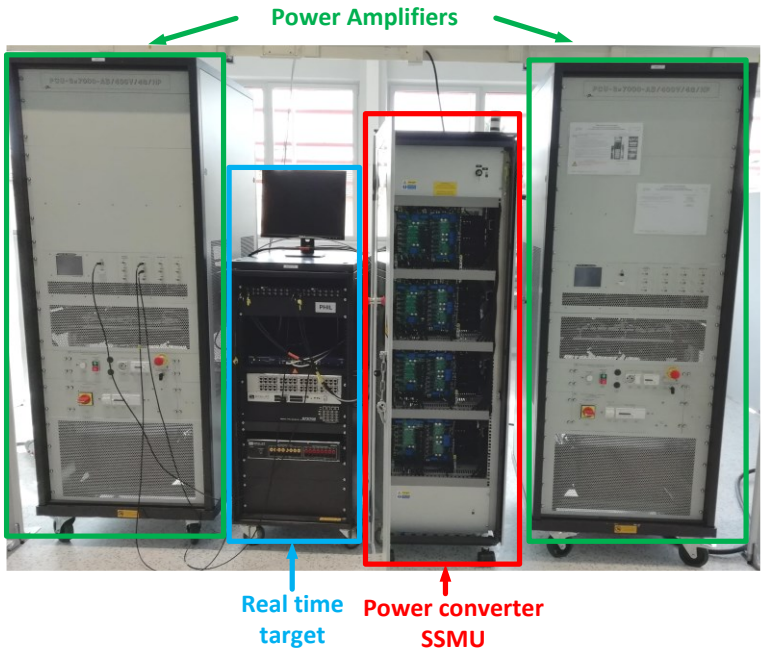


Fig. 5 – PHIL setup implementation

Power, current or voltage control strategy can be applied for the DC-DC. However, in this work, the voltage regulation is selected because of the architecture specification (see Fig. 2 (a)). The fact that the input current $I_{dc,LV}$ is imposed by the wind turbines forces the LVDC/MVDC converter to regulate the input voltage $V_{dc,LV}$. Likewise, the output voltage $V_{dc,MV}$ is imposed by MVDC/HVDC converter, so balancing the output capacitors is required. The time constant of the regulation of $V_{dc,LV}$ has been set to 1ms while the time constant for the regulation of the balancing MV side capacitors has been set to 3ms. The time-step of the real-time simulation has been set to 20µs.

The test scenario is divided in 3:

1. start-up sequence which consists in energizing both sides of the converter
2. power ramp up to the rated power of the converter
3. stop of the wind turbine

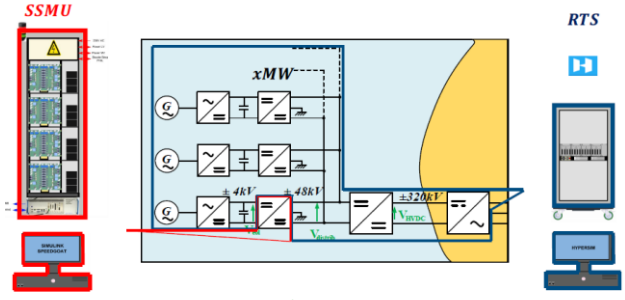


Fig. 6 – Position of the SSMU in the complete wind farm real time model

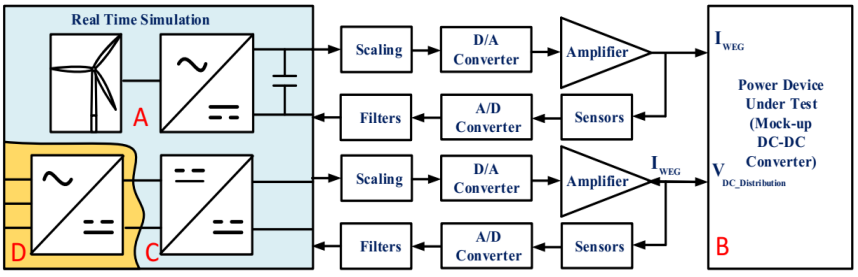


Fig. 7 – Signals exchange interface between the device under test and the real time simulation

Start-up sequence of the converter

It is assumed that the voltage at the PCC is present. The precharge of the MV capacitors is done using the contactor K_{pr1} (Fig. 8), closed at $t = t_0$, which connects the converter to the DC collector via a resistance, R_{pr}. This resistance forms an RC circuit with all the MV capacitors in series in order to increase smoothly the MV voltage of the converter near 400VDC. Then the contactor K_{pr2} is closed at $t = t_1$ in order to by-pass the resistor. These two contactors with the resistor would be a DC breaker with a pre-insertion resistor (PIR) in the final application.

Once the MV capacitors are fully charged, the next step is to charge the low voltage capacitors. The MV bridges are controlled in open loop from $t = t_2$ to $t = t_3$ in order to generate square wave voltages with a duty cycle smoothly increasing from 0 to 0.5 while the LV bridges are acting as diode rectifiers. Once the low voltage capacitors are considered charged - voltage above 95% of the nominal voltage during a certain time - the control of the converter is started at $t = t_3$. The 4 cells of the converter are controlled in order to maintain the LVDC voltage at 50VDC and to equilibrate the MV capacitor voltages. At this point, the converter start-up is over.

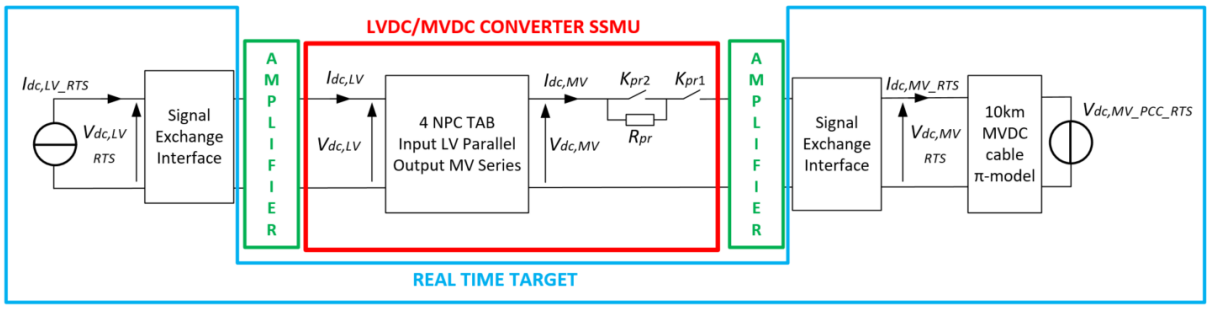


Fig. 8 – Interface between the SSMU converter, the amplifiers and the simplified real time model

Wind turbine power ramp

For the response to a start-up of the wind turbine generation, a power ramp of 40A/s is applied to pass from no power production to maximum power production 2kW in one second.

Wind turbine stop

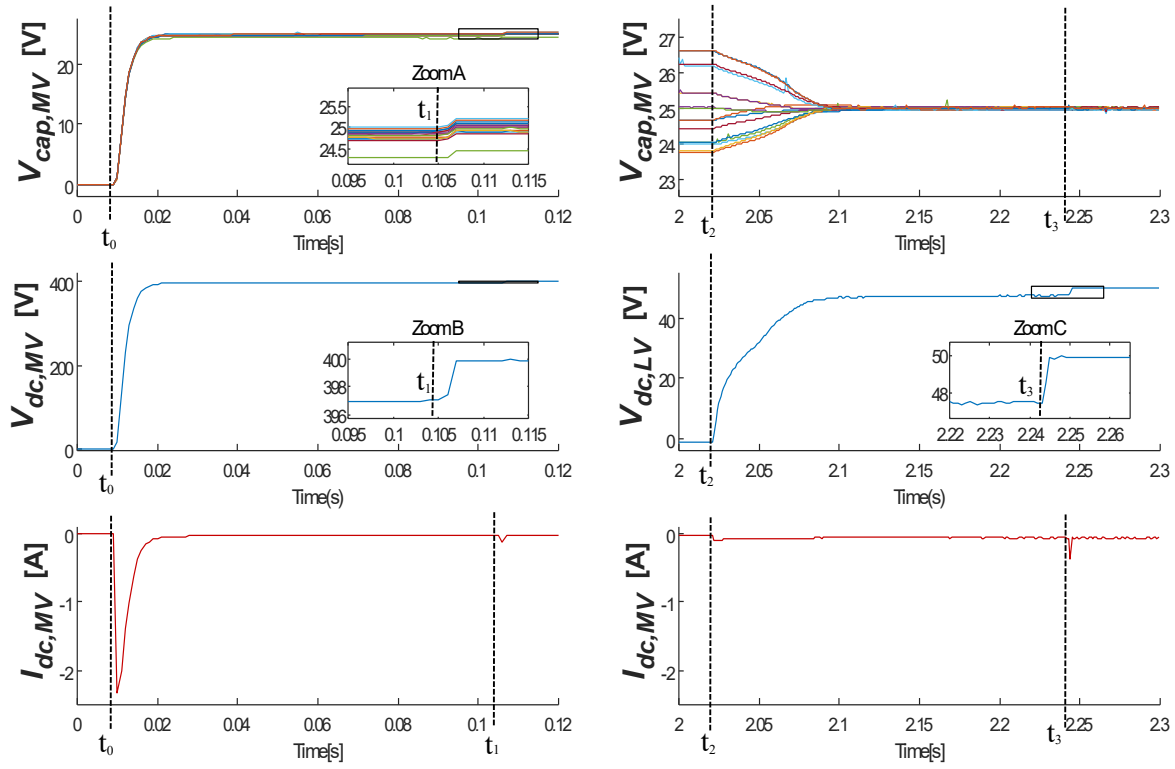
In order to emulate a fault of the wind turbine rectifier, a -4kA/s ramp from maximum power to 0 is applied.

Experimental results

Start-up sequence of the converter

In Fig. 9, at t_0, the closing of K_{pr1} starts the precharge of the MV side capacitors with the inrush current limited by the value of R_{pr}. At t_1, K_{pr2} is closed which creates a step in $V_{dc,MV}$ that induces the inrush current $I_{dc,MV}$.
It can be seen the plots of the 16 $V_{cap,MV}$ in Fig. 9 that at this point, between t_1 and t_2, the voltages across the different MV capacitors are not balanced due to the dissymmetry of the components but they find an equilibrium around 25VDC each.
At t_2, the precharge of the LV side capacitors begins. It can be seen that the charge is not exponential as would be a perfect RC circuit response. This can be explained by nonlinearities of the circuit. An interesting behavior to notice in Fig. 9, $V_{cap,MV}$, is that the MV capacitor voltages are being balanced at the start-up of the MV side half-bridges, at t_2. This balancing is not controlled but is a characteristic of the half-bridge topology: once the half-bridge is activated the imbalance of the capacitor voltages, due to dissymmetry of the capacitors characteristics, is naturally corrected by the current circulation between the two series connected capacitors.

The start of the control can be identified in Fig. 9, $V_{dc,LV}$, as the step of the low voltage at t_3, zoom C, since the converter passes from an equilibrium point of almost 48VDC where the low DC voltage is only the AC voltage rectified with the voltage drop of the diode to a voltage controlled by the converter at 50VDC.



a. b.

Fig. 9 – Measurements of the 16 MV side capacitor voltages ($V_{cap,MV}$), the total MV DC voltage ($V_{dc,MV}$) and MV DC current ($I_{dc,MV}$) during the MV precharge (a) ; Measurements of the 16 MV capacitor voltages ($V_{cap,MV}$), the LV DC voltage ($V_{dc,LV}$) and MV DC current ($I_{dc,MV}$) during the LV precharge (b)

Wind turbine power ramp

In Fig. 10, even if the overall LV voltage $V_{dc,LV}$ is close to 50VDC, the voltages of the individual LV capacitors $V_{cap,LV}$ diverge as power flow changes. This behavior is normal for NPC full-bridge converters running in square wave modulation due to the inevitable dissymmetry of the components. In order to limit this imbalance, an algorithm is used allowing to balance the voltages if the voltage difference reaches a threshold. This compensation can be observed on $V_{cap,LV}$ as it is activated multiple times in the third cell. Due to this compensation but also due to the power exchange between cells and the control loop time constant, some oscillations can be observed on $V_{dc,LV}$ and $V_{cap,MV}$. However, these oscillations stay very low compared to 50VDC (less than 0.5%). It is also interesting to notice that the LV DC current $I_{dc,LV}$ is perfectly balanced between the 4 cells (see $I_{stage,LV}$) even if the plot of the phase-shifts δ shows differences between them. This independence between the phase shifts allows to compensate the small differences of the hardware between the 4 cells, to ensure the balance of currents.

Since the MVDC/HVDC converter is controlling the MVDC voltage at its output, V_{dc,MV_PCC}, the voltage at the MV input of the LVDC/MVDC converter under test, $V_{dc,MV}$, is increasing while power is transferred due to the resistive behavior of the cable between the two converters. In consequence the low voltage increases proportionally, since the converter does not control a fix value for the LV DC bus but half of one stage total medium voltage.

Fig. 11 shows the AC measurements of one cell in steady state at maximum power. The primary with one of the secondary act as a Dual-Active-Bridge. The theoretical AC current should be trapezoidal, however, due to the relatively low voltage of the mock-up, the voltage drops in all the components are

not negligible. The resulting voltage across the small leakage inductance of the transformer (10µH) induces a di/dt when the current should be constant. The transient behavior of $V_{ac,a}$ at the rising and falling edges is due to the change of conducting diodes during the dead time when the sign of the current changes.

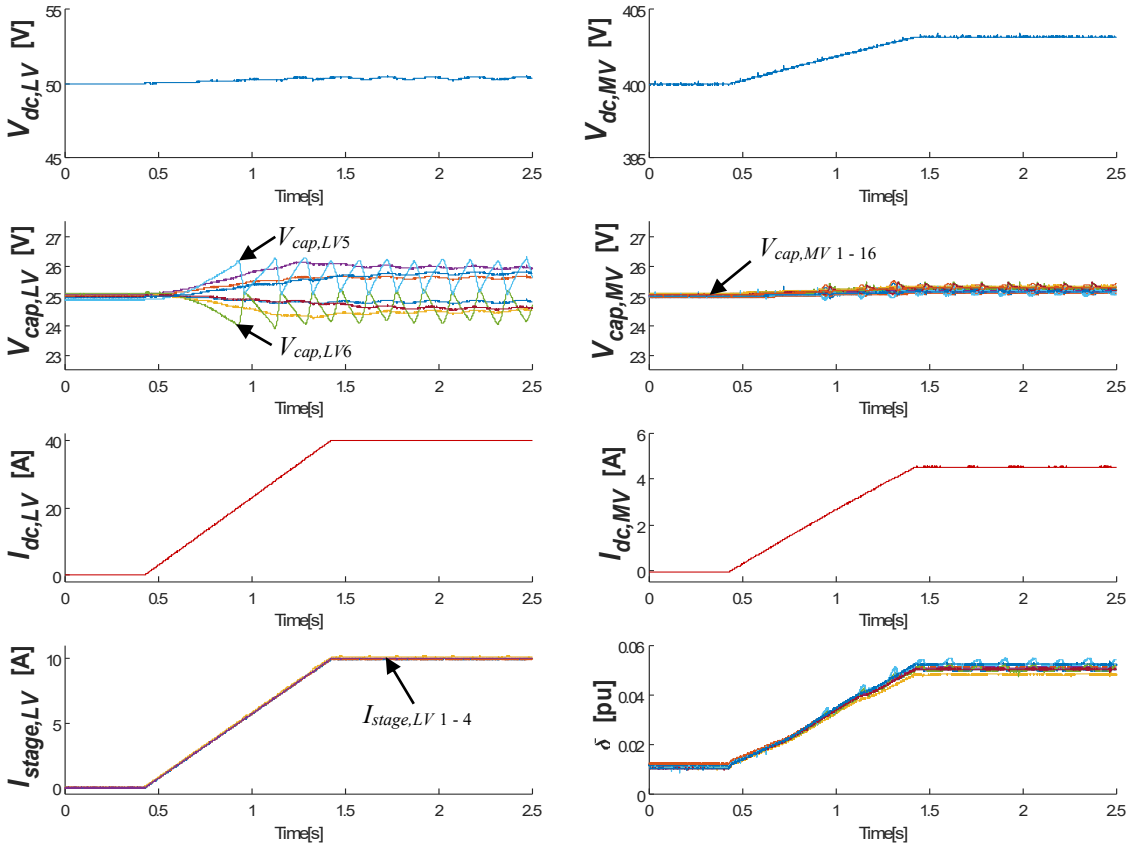


Fig. 10 - Measurements of the total LV DC voltage ($V_{dc,LV}$), total MV DC voltage ($V_{dc,MV}$), the 8 LV capacitors DC voltages ($V_{cap,LV}$), the 16 MV capacitors DC voltages ($V_{cap,MV}$), the total LV DC current ($I_{dc,LV}$), the MV DC current ($I_{dc,MV}$), the DC LV current for each of the 4 cells ($I_{stage,LV}$) and the 8 phase-shifts (δ) on the SSMU during the response to a power ramp of 2kW/s

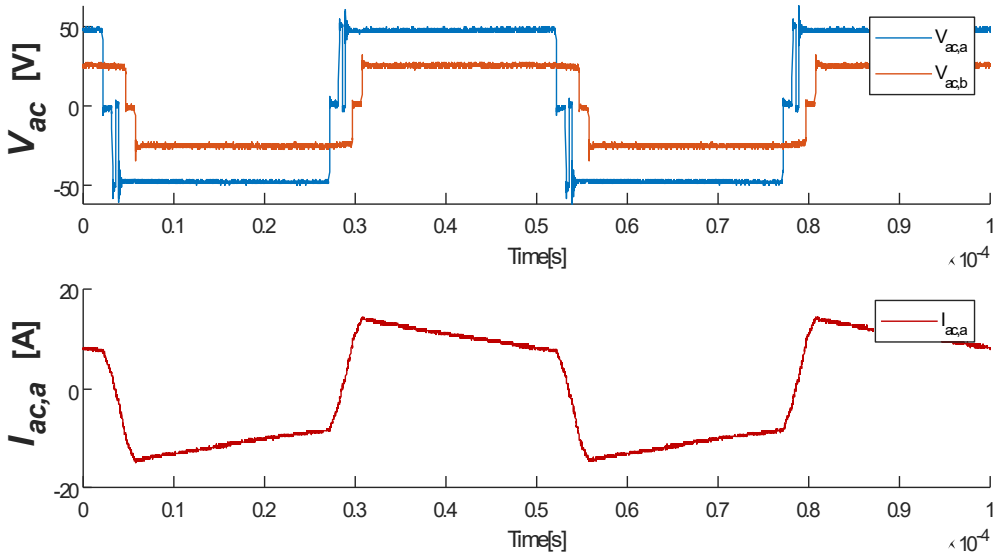


Fig. 11 - AC voltages ($V_{ac,a}$ et $V_{ac,b}$) and AC current ($I_{ac,a}$) measurement on one stage of the converter as illustrated in Fig. 4 (b) in steady state at Pmax

Wind turbine stop

The experimental results for a sudden stop of the wind power are presented in Fig. 12. A small voltage dip which is quickly corrected can be observed on the low voltage bus of the converter, $V_{dc,LV}$. After that, both LV side and MV side capacitor voltages are balanced. There is nothing to notice in the MVDC collector, $V_{dc,MV}$. The DC currents, $I_{dc,LV}$, $I_{stage,LV}$ and $I_{dc,MV}$, are all very clean even if there is a dip on the LV bus since the wind turbine is considered as a perfect current source and not a power source.

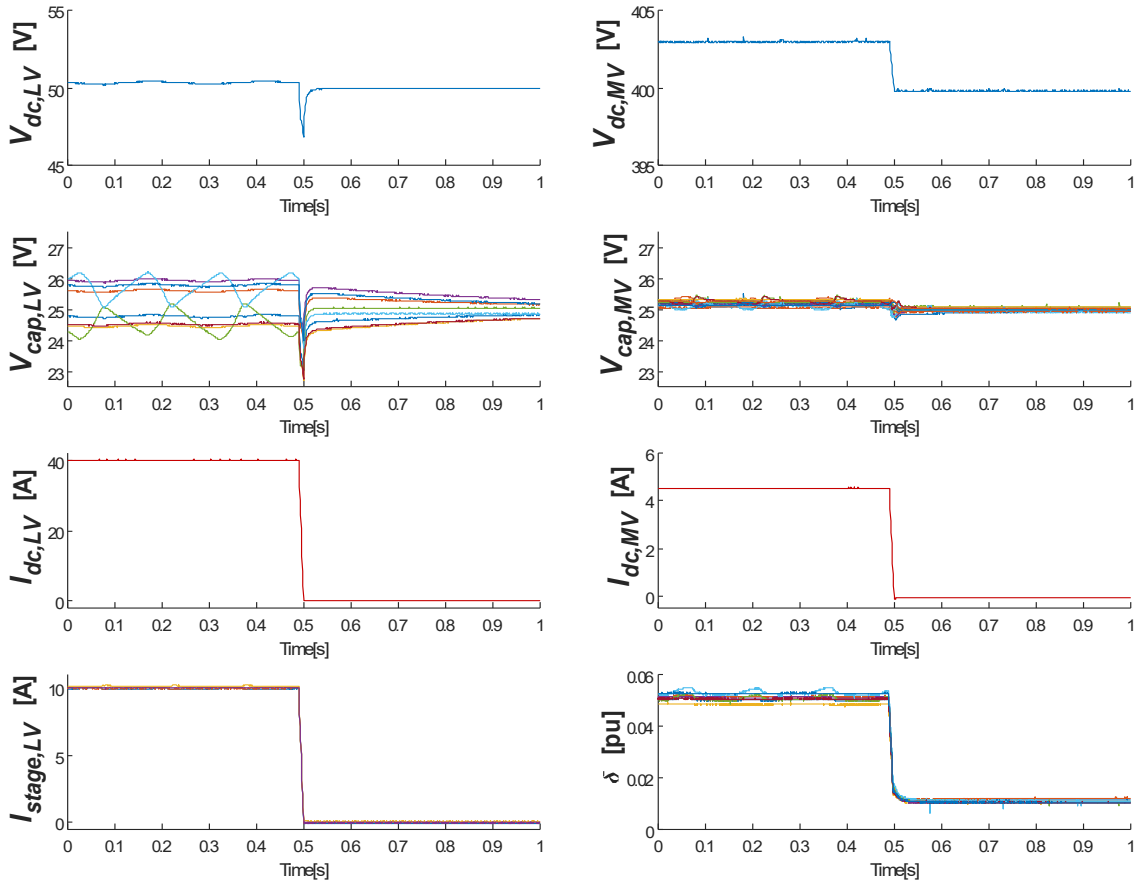


Fig. 12 - Measurements of the total LV DC voltage ($V_{dc,LV}$), total MV DC voltage ($V_{dc,MV}$), the 8 LV capacitors DC voltages ($V_{cap,LV}$), the 16 MV capacitors DC voltages ($V_{cap,MV}$), the total LV DC current ($I_{dc,LV}$), the MV DC current ($I_{dc,MV}$), the DC LV current for each of the 4 cells ($I_{stage,LV}$) and the 8 phase-shifts (δ) on the SSMU during a stop of the wind turbine (ramp of -4kA/s)

Conclusion and perspectives

The PHIL validation of a DC-DC power converter for offshore wind farm was presented. The selected case study was the full DC wind farm architecture with bidirectional DC-DC power converters. A simulation model of the complete wind farm was developed and implemented in a real-time target. A small scale mock-up of the wind turbine LVDC/MVDC converter was developed. The converter mock-up was implemented in a PHIL test bench and the normal operation was demonstrated with a simplified model of the system.

The PHIL approach becomes essential when validating the innovative power converter concepts where the HIL is pushed to their limits. Thanks to the small scale mock-up, the converter topology and controls can be easily validated within the power system environment. This approach minimizes the converter integration risks and reduces the product development time and cost. As an example, some sequences as the converter energization may be omitted while designing the converter. The fact to think about its

integration in an overall system early in the design process when considering PHIL helps to identify these aspects.

The preliminary PHIL results allow to validate the SSMU of the LVDC/MVDC converter and its interactions with the real-time simulation through the power amplifiers. The converter shows a very good behavior in different test scenarios. The bandwidth of the control loop allows the converter to react properly to fast ramp of power which can be useful for sudden stop after a fault detection in the system. The capacitor balancing algorithm seems acceptable since the residual oscillation on the overall voltage is very low however a more performant solution could be investigated. In fact, this solution increases the quantity of commutations, therefore increasing the losses and accelerating the ageing of passive components.

The authors will extend the PHIL tests using the real time simulation model of the complete wind farm which has been developed. Some further investigations are envisaged in different normal and degraded operating conditions.

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