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Impact of channel length on the operation of junctionless transistors with substrate-biasing

Dae-Young Jeon, Mireille Mouis, *Senior Member, IEEE*, Sylvain Barraud and Gérard Ghibaudo, *Fellow, IEEE*

***Abstract*—Junctionless transistors (JLTs) have promising advantages such as structural simplicity without PN-junctions and bulk conduction-based operation for the realization of advanced CMOS technologies. Here, channel length dependence on the operation of JLTs with substrate-biasing (V_{gb}) was investigated in detail. Parasitic series resistance (R_{sd}) was noticeably decreased as increasing V_{gb}. In addition, transconductance (g_m), its derivative (dg_m/dV_{gf}) and on-drain current (I_{on}) in a short-channel JLT were significantly affected by the V_{gb}-modulated R_{sd} with charge coupling effects. This work provides important information for better understanding and true estimation of intrinsic JLT performance, for practical applications based on polycrystalline Si, III-V semiconductors and TMDs nano-materials as well as advanced logic devices.**

***Index Terms*—Junctionless transistors (JLTs), substrate-biasing effect, channel length dependence, series resistance (R_{sd}), electrical parameters modulated by substrate bias.**

I. Introduction

Structural simplicity without PN-junctions of junctionless transistors (JLTs) is the most promising advantage for the realization of sub-5 nm complementary metal-oxide-semiconductor (CMOS) technologies [1-5].

The junctionless architecture with uniformly doped source (S), channel and drain (D) enables no need of precise gate-alignment and abrupt S/D junction formation with a low-thermal-budget [3-5]. Bulk conduction-based operation in JLTs also results in better reliability, lower 1/f noise and less mobility degradation against transverse electric-field (E-field) [6-9]. In addition, JLTs in a variety of materials, including polycrystalline silicon (Si), III-V semiconductors and 2-dimentional (2D) transition metal dichalcogenides (TMDs), have been reported for high performance thin-film transistors (TFTs), 3D vertical transistors, sensors and multi-functional devices with excellent short-channel characteristics [10-14].

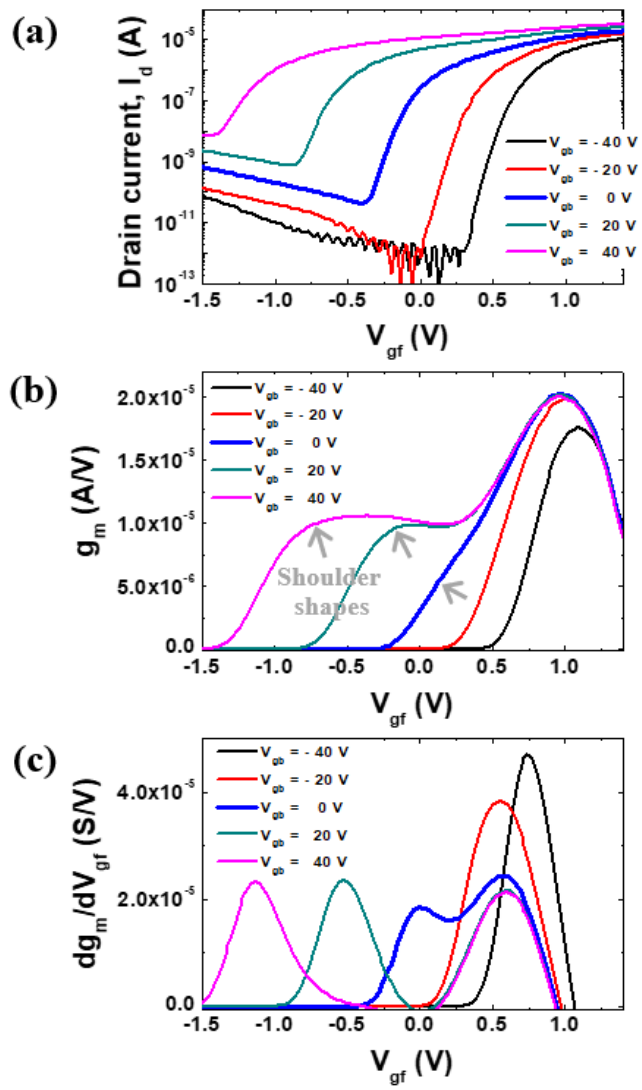

Fig. 1. (a) Transfer curves, (b) transconductance (g_m) and (c) derivative of g_m (dg_m/dV_{gf}) measured from a very long channel JLT of L_m = 10 µm with varying V_{gb}. The device was biased in the linear operation-regime with drain voltage V_d = 50 mV.

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D.-Y. Jeon is with Institute of Advanced Composite Materials, Korea Institute of Science and Technology, Joellabuk-do 55324, South Korea (e-mail: dyjeon@kist.re.kr).

M. Mouis and G. Ghibaudo are with IMEP-LAHC, Grenoble INP, Minatec, BP 257, 38016 Grenoble, France.

S. Barraud is with CEA-LETI Minatec, 17 rue des Martyrs, 38054 Grenoble, France.

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Silicon-on-insulator (SOI) technology based JLTs can be operated by both front-gate and back-gate [15,16]. In-depth studies about substrate-biasing effects and charge coupling between front and back interfaces are very important for optimizing performance and better understanding operation mechanism of JLTs.

In this paper, channel length dependent substrate-biasing effects on the operation of JLTs were investigated in detail. Parasitic series resistance (R_{sd}) of JLTs was noticeably modulated by the substrate bias. Transconductance (g_m), its derivative (dg_m/dV_{gf}) and effective mobility in a short-channel JLT were significantly affected by the substrate-bias-controlled R_{sd} with charge coupling effects between front and back interfaces.

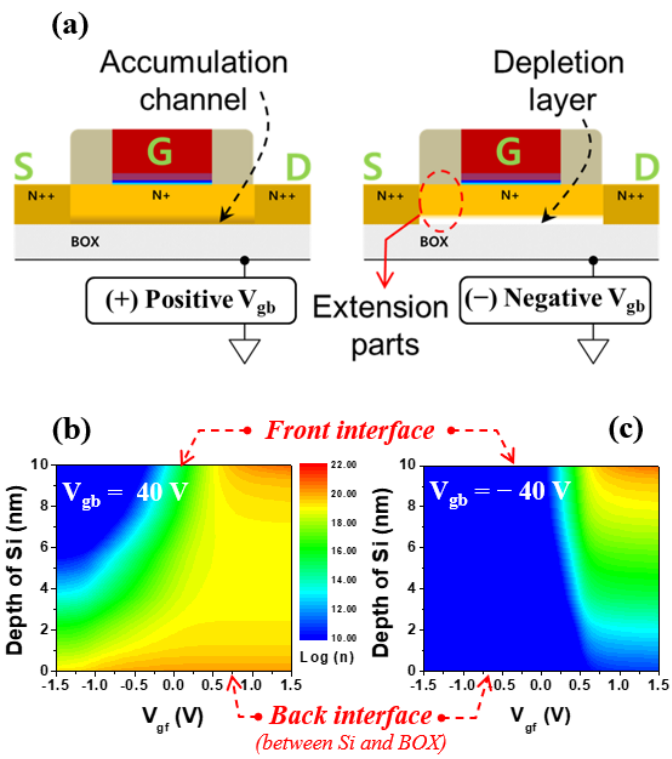

Fig. 2. (a) Schematic architecture of JLT describing the accumulated charge carriers at back interface for positive V_{gb}, and the depletion of charge carriers due to negative V_{gb}. Simulated distribution of electron carrier concentration per unit volume (n) along the depth of device Si varying V_{gf} with different V_{gb}, (b) V_{gb} = 40 V and (c) V_{gb} = − 40 V.

II. Experiments

JLTs with device Si ≈ 10 nm and high-k dielectric ≈ 1.2 nm were fabricated on (100) SOI wafers with thick buried oxide (BOX) ≈ 145 nm. Channel of JLTs was highly doped with phosphorus, and effective doping concentration was estimated as ≈ 5 × 10^{18}/cm^3. An additional S/D implantation was also performed to reduce access resistance. Further detail information with respect to fabrication and material parameters was described in previous works [17]. Electrical characteristics were measured by using HP 4155A semiconductor parameter analyzer, and simulated results were obtained by FlexPDE software, which is a numerical solver based on scripted finite element models.

III. Discussion

The bold blue plots as shown in Fig.1 show transfer curve, transconductance (g_m) and derivative of g_m (dg_m/dV_{gf}, where V_{gf} means front-gate voltage), obtained from a very long channel JLT (L_m = 10 μm) with back-gate voltage (substrate bias) V_{gb} = 0V. Shoulder shape on the g_m and two clear peaks on the dg_m/dV_{gf} in JLTs represent unique electrical properties based on both bulk neutral and surface accumulation conductions, which is very different from the operation of conventional inversion-mode (IM) transistors [8,17]. The first (left-hand side) and second peak (right-hand side) on dg_m/dV_{gf} denote conduction threshold voltage (V_{th}) and flat-band voltage (V_{fb}), i.e. threshold of accumulation conduction channel, respectively. The shoulder shape on g_m is also strongly associated with the amount of charge carriers on the operation at $V_{gf} = V_{fb}$ condition. As V_{gb} decreased, the shoulder shrunk in Fig. 1(b) and the two peaks merged as a single peak in Fig. 1(c), due to the effectively reduced bulk channel thickness resulted from the negative V_{gb}-induced depletion of free charge carriers at back interface between device Si and BOX [18]. On the other hand, bulk neutral channel of JLTs can be early turned on, and additional accumulation channel is newly created at the back interface with a positive V_{gb}. Those gave rise to the pronounced shoulder shape in Fig. 1(b) and left-shift of the first peak in Fig. 1(c), as V_{gb} increased.

Figure 2 shows the simulated substrate-biasing characteristics of JLTs. The distribution of electron carrier concentration per unit volume (n) along the depth of device Si was visualized by varying V_{gf} with different V_{gb}. One can clearly identified the shrunk bulk channel with negative V_{gb}, and the early turned-on

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bulk channel with the newly accumulated carriers for positive V_{gb}. Indeed, a depletion layer in blue color was observed at back interface for $V_{gb} = -40$ V in Fig. 2(c), while an additional accumulation layer in red or orange color was created at the back interface for $V_{gb} = 40$ V in Fig. 2(b).

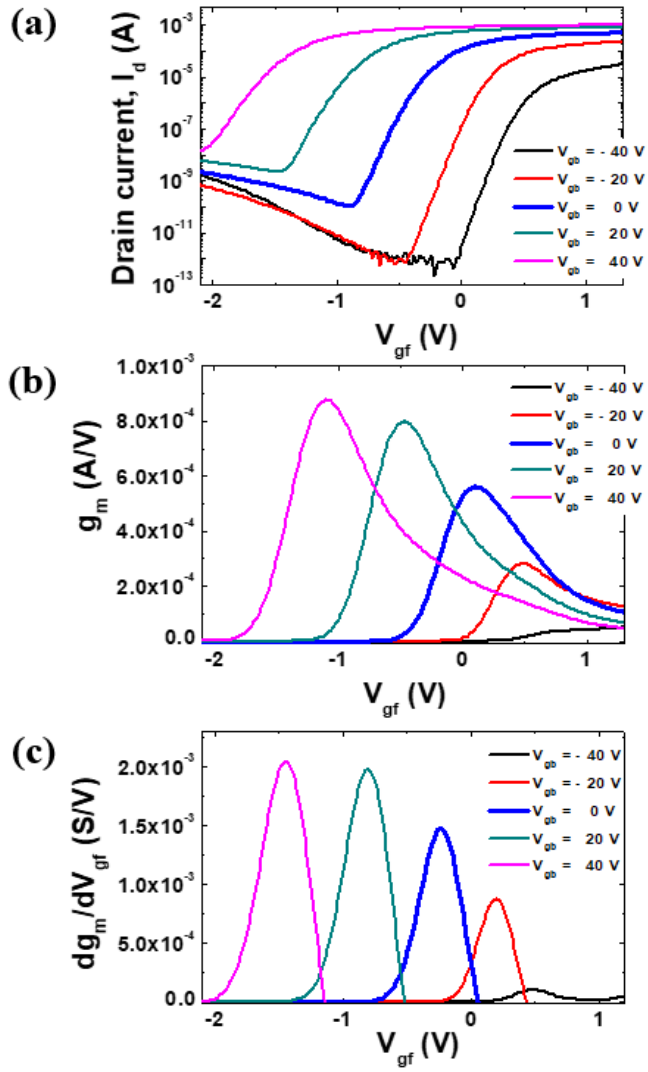

Fig. 3. (a) Transfer curves, (b) transconductance (g_m) and (c) derivative of g_m (dg_m/dV_{gf}) measured from a very short channel JLT of $L_m = 40$ nm with varying V_{gb}. The device was biased in the linear operation-regime with drain voltage $V_d = 50$ mV.

Completely different substrate-biasing behaviors were investigated in JLTs with a very short channel length ($L_m = 40$ nm), as shown in Fig. 3. A shoulder shape was not observed any more in Fig. 3(b), and only a single peak was shown in Fig. 3(c), since the parasitic series resistance (R_{sd}) considerably affects the short-channel JLTs characteristics [19,20]. In addition, the on-drain current (I_{on}, $V_{gf} > 1.0$ V) in Fig. 3(a) was dramatically changed by varying V_{gb}, as compared to that of the long channel JLT in Fig. 1(a). The g_m in Fig. 3(b) was also getting noticeably degraded as decreasing V_{gb}. The variation of V_{gb} could have an effect on the value of R_{sd}, and the R_{sd} modulated by V_{gb} could affect overall results related to substrate-biasing in the short channel JLTs.

V_{gb} controlled R_{sd} of JLTs was estimated by using transfer length method (TLM) in Fig. 4. Total resistance (R_{tot}) including JLT channel resistance (R_{ch}) and R_{sd} can be calculated as [21]:

$$R_{tot} = R_{ch} + R_{sd} = \rho_{ch} \times \frac{L_m - \Delta L}{W_m} + R_{sd} \qquad (1)$$

where ρ_{ch}, ΔL and W_m are channel sheet resistance, channel length reduction and on-mask channel width, respectively. The clear common intersection point of the linear fitted lines on the accumulation operation regime ($V_{gf} > V_{fb}$) successfully determined $R_{sd} \approx 104\ \Omega$ for $V_{gb} = 0$V, as shown in Fig. 4(a).

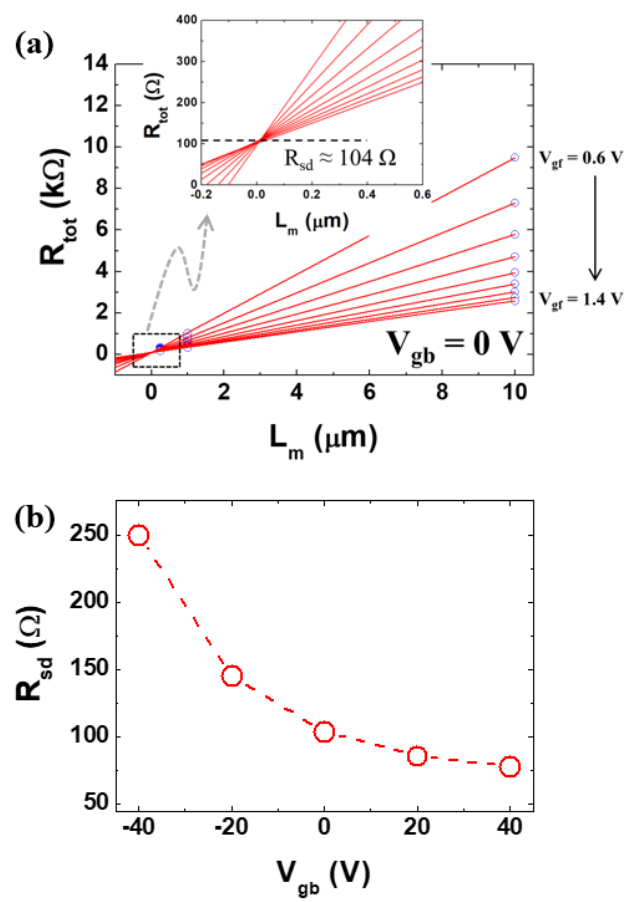

Fig. 4. (a) Total resistance (R_{tot}) versus channel lengths ($L_m = 250$ nm, 1 μm and 10 μm) with varying V_{gf}, for determination of series resistance (R_{sd}). The inset shows a clear common intersection of the linear fitted lines. (b) Extracted R_{sd} modulated by V_{gb}.

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Finally, V_{gb} dependent R_{sd} was plotted in Fig. 4(b) after the same procedure for R_{sd} extraction with different V_{gb} from −40 V to 40 V. Indeed, R_{sd} was decreasing for positive V_{gb}, while it was increasing when applying negative V_{gb}. Accumulated charge carriers at back interface for positive V_{gb} reduces resistance of the extension parts (R_{ext}), as illustrated in Fig. 2(a). R_{ext} can be also enhanced by the depletion of charge carriers due to negative V_{gb}. Similar trend of the substrate-bias affected R_{sd} have been also reported in SOI based transistors with lightly doped drain (LDD) [22].

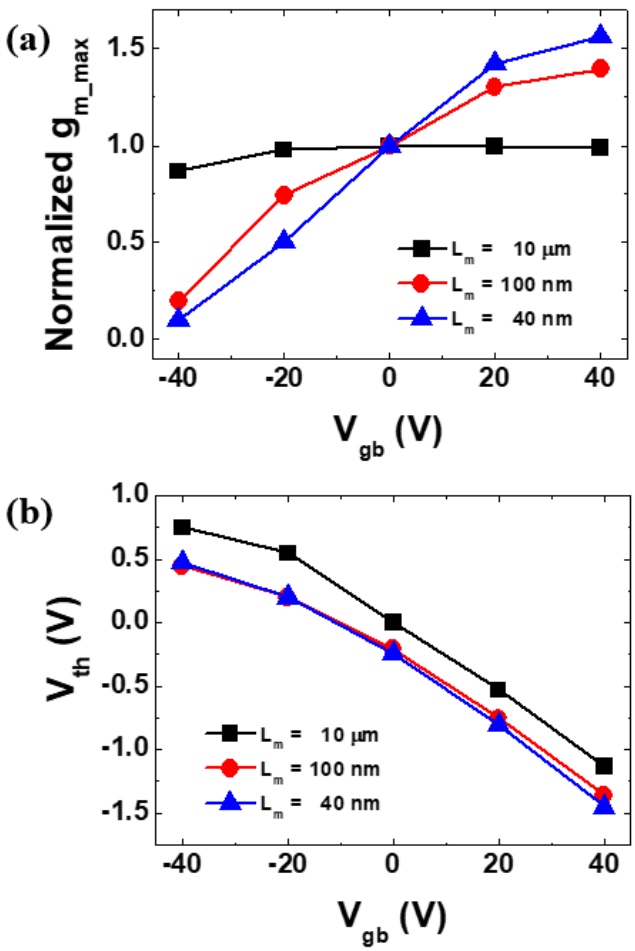

Fig. 5. (a) Normalized g_{m_max} [i.e. maximum-$g_m(V_{gb})$/maximum-gm(V_{gb} = 0 V)] versus V_{gb}, with different JLT lengths. (b) Threshold voltage (V_{th}) as a function of V_{gb} with different JLT lengths, the V_{th} was extracted from the first peak in the dg_m/dV_{gf} plots.

Figure 5(a) shows the normalized g_{m_max} [i.e. maximum-$g_m(V_{gb})$/maximum-$g_m(V_{gb}$ = 0 V)] versus V_{gb}, with different JLT lengths. It should be noted that the trend of g_m is closely related to characteristics of field-effect mobility behaviors [23]. There was a slight decrease in the normalized g_{m_max} of long length JLT (L_m = 10 µm) as decreasing V_{gb}. This feature is attributed to the lower mobility at the top interface, since the high-k dielectric (HfSiON) for top-gate insulator has poorer interface-properties than that in pure thermal oxide (SiO_2) of BOX at the back interface [15-17]. However, the variation of V_{gb} significantly changed the normalized g_{m_max} in JLTs with L_m = 40 nm. The increased value of R_{sd} at a negative V_{gb} caused the dramatically enhanced degradation of g_m and field-effect mobility in the short channel JLTs. Moreover, the threshold voltage (V_{th}) extracted from the first peak in the dg_m/dV_{gf} plots was plotted as a function of V_{gb} as shown in Fig. 5(b). As decreasing length of JLTs with a same V_{gb}, V_{th} was reduced due to short-channel effects [17]. Whereas the variation rate of V_{th} against V_{gb} changes was very similar regardless of JLT lengths. Interestingly, this means that substrate-biasing impact on the operation near V_{th} regime is independent of channel-length variation in JLTs.

IV. Conclusions

The operation of junctionless transistors (JLTs) with substrate-biasing (V_{gb}) has been investigated, and its channel length dependence was also discussed in detail. A shoulder shape on transconductance (g_m) and clear two peaks on derivative of g_m (dg_m/dV_{gf}) were observed in a long-channel (L_m = 10 µm) JLT with V_{gb} = 0V, since JLTs have both bulk neutral and surface accumulation conduction channels. The shoulder shape shrunk and the two peaks merged as a single peak when applying negative V_{gb}. For positive V_{gb}, the shoulder shape was pronounced and the first peak on the dg_m/dV_{gf} moved to the left-hand side. Completely different features (no shoulder shape on g_m and only a single peak on dg_m/dV_{gf}) were investigated in a very short-length (L_m = 40 nm) JLT due to parasitic series resistance (R_{sd}) effect. The R_{sd} was noticeably decreased as increasing V_{gb}, and this gave rise to the dramatical changes on-drain current (I_{on}) and field-effect mobility of the short-channel JLTs against the variation of V_{gb}. However, substrate-biasing impact on the operation near V_{th} regime was similar regardless of JLT lengths. Further calibration with the experimental data and stronger coupling

effects in ultra-thin body and buried oxide (UTBB) structures will be our future works [24,25].

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