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This letter presents magnetic tunnel junction based spintronic devices completely implemented in a hybrid semiconductor process that comprises a complementary metal oxide semiconductor and a magnetic tunnel junction technology. To demonstrate the coexistence of both complementary metal oxide semiconductor circuits and magnetic tunnel junction based spintronic devices, a proof-of-concept circuit prototype comprising 40 spintronic devices and a digital complementary metal oxide semiconductor serial peripheral interface is fabricated. According to measurement results, a selected spintronic device from the magnetic tunnel junction array, when surrounded by an external out-of-plane magnetic field of 1 kOe, emitted microwave signals from 2.235 to 2.464 GHz with an output power from 0.88 to 0.72 nW, when the DC current was increased from 0.6 to 1.0 mA. To the authors' best knowledge, this is the first work demonstrating the functionality of spintronic oscillators fully integrated in complementary metal oxide semiconductor circuit implemented in a hybrid complementary metal oxide semiconductor and magnetic tunnel junction process.

Introduction: Since a decade, there has been a rising interest in the development of magnetic tunnel junction (MTJ) devices due to their low-power consumption, compactness, complementary metal oxide semiconductor (CMOS) compatibility and multi-functionalities for both memory- and microwave-related applications. Spin-transfer torque (STT) based memory, for instance, is a promising candidate for universal memory technology where the MTJ's STT and tunnel magnetoresistance (TMR) effects are exploited [1]. Moreover, based on the STT effect, via injection of a DC current into an MTJ, such devices can also emit microwave signals [2]. The MTJ device of this type is known as spintronic oscillator (STO), a natural current-controlled microwave oscillator and particularly attractive for microwave engineering due to its advantages compared to conventional semiconductor oscillators. For instance, STOs usually occupy an area of $< 0.1\ \mu m^2$, which are much more compact than their semiconductor counterparts such as LC voltage controlled oscillators ($0.1-1\ mm^2$) and ring oscillators ($0.01-0.1\ mm^2$). In addition, they also offer benefits such as design and control simplicity, broad frequency range (1−20 GHz) as well as CMOS compatibility [3].

State of the art: Despite the intensive developments so far, all these unique properties of MTJs have been realised separately, using dedicatedly optimised MTJ stacks. Especially for the microwave functionalities, although MTJ-based STOs are claimed to be compatible with CMOS technologies [3], their functionality that has been demonstrated comes only from STOs fabricated in standalone MTJ processes. For instance, the spintronic devices used for GHz-signal generation in [3, 4], signal modulation in [5–7], wireless communication in [8, 9], as well as ultra-fast spectrum analysis in [10], are all standalone MTJ devices fabricated on a single MTJ stack without any other active semiconductor devices. Therefore, to bring spintronic devices into radio frequency (RF)-related markets, it is hence a milestone step to merge the microwave-oriented MTJs with conventional CMOS technologies and to verify the feasibility.

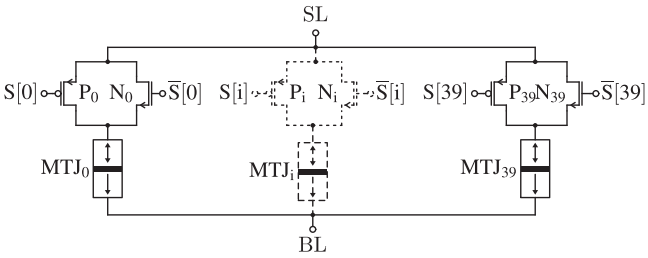

Fig 1 *Simplified schematic of the proposed 40 MTJ-based STO array*

In fact, one of our recent works in [11] has demonstrated the sensor and RF functionalities of the MTJ-based spintronic devices in a hybrid CMOS–MTJ process. However, the MTJs from [11] were still MTJ individuals neither employed in nor combined with any other CMOS circuits. As a follow-up step, this work is aimed to demonstrate the microwave functionality of spintronic devices utilised in CMOS circuits fully implemented in an optimised CMOS–MTJ process that is based on the technology developed in [11]. To the best knowledge of the authors, this is the first work demonstrating the RF functionalities of the spintronic devices with CMOS circuits in a single semiconductor process.

Circuit design and implementation: To demonstrate the compatibility of MTJ-based STO devices with CMOS technology, a minimal structural unit is implemented, where an STO individual is connected in series with a CMOS switch. This switch is implemented using a transmission gate (TG) to provide a bi-directional current flow through the STO. The on–off state of the STO device can be defined via the TG, which is controlled through an on-chip SPI. Moreover, the W/L ratio of the nMOS and pMOS transistors comprising the TG are 20/0.18 and 30/0.18, respectively, which is a design compromise between DC resistance and parasitic capacitance of the TG. The simulated TG's DC series resistance and parasitic capacitance are 30 Ω and 20 fF, respectively. The diameter of a single STO is set to be 100 nm, which is, according to simulation results based on our Verilog-A model proposed in [12], an optimised result to provide the STO with the optimal overall performance. Furthermore, to efficiently characterise a certain number of STO devices and to save silicon area required by the pads for wire-bonding purposes, an STO device array is designed, where forty 1 STO−1 TG units are connected with each other in parallel. The number *forty* is chosen as a result of design compromise between the STO device number and parasitic capacitance and inductance introduced by the connections and wiring among the 1 STO−1 TG units. Simulation results show that the connections, wiring with the input source line (SL) or output bit line (BL) pad of the array have a total parasitic capacitance of 1.2 pF.

Figure 1 shows the simplified schematic of the 40 STO arrays. A circuit prototype was fabricated in a hybrid CMOS–MTJ technology that consists of a front-end-of-line implemented in a TowerJazz 180 nm CMOS, an MTJ stack optimised, deposited and tempered in Singulus as well as a back-end-of-line (BEOL) implemented in a TowerJazz 130 nm CMOS. The two different CMOS flows were combined together due to design trade-offs between device performances and fabrication costs. Figure 2(a) depicts the layer composition of the MTJ stack dedicated to provide MTJ-based STO devices with the microwave generation functionality. Figure 2(b) details the layer composition of the entire hybrid CMOS–MTJ process. The CMOS active layer, the first and second metal layers M1 and M2 were fabricated in a TowerJazz 180 nm CMOS technology. The MTJ stack with its top and bottom electrodes MM1 and MM2 was located between the third and the fourth metal layers M3 and M4. The BEOL comprising the metal layer M4 and the other layers above it was implemented in a TowerJazz 130 nm CMOS technology. Figure 2(c) shows the layout view and chip photograph of the fabricated MTJ array. The MTJ array that contains 40 1 STO–1 TG units occupies only a silicon area of 80 μm × 90 μm.

Experimental results: The circuit prototype was wire-bonded and measured on a test PCB, where its supply voltage V_{DD} was set to 1.8 V. An external 0.5 MHz−26.5 GHz bias tee (Marki BTN1-0026) was used to extract the generated signal V_{MTJ} from the MTJ array output SL. V_{MTJ}

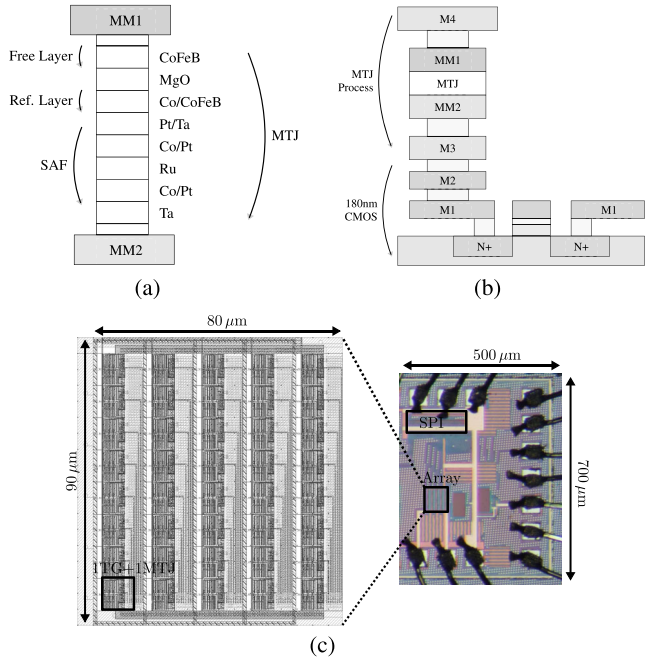

Fig 2 *(a) Layer composition of a perpendicular MTJ nanopillar. Thickness of each layer of the MTJ is as follows (in nm): MgO, FeCoB(0.5), MgO, FeCoB(1), Co(0.9), Pt(0.2), Ta(0.15), 3×[0.5 Co/0.2 Pt], Ru(0.8), 6×[0.5 Co/0.2 Pt(6). (b) Layer composition of the hybrid CMOS–MTJ technology. (c) Layout of the MTJ array and photograph of the MTJ array prototype chip*

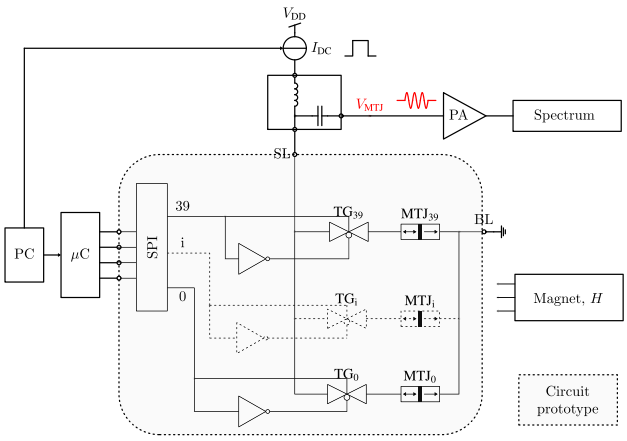

Fig 3 *Experimental set-up in verification of the MTJ's functionalities*

was then amplified by an external 1−10 GHz power amplifier (PA) with a gain of 40 dB (Miteq AMF-50), and finally registered in a spectrum analyser (Rohde \& Schwarz FSW43). Figure 3 shows the principle diagram of the measurement set-up.

Using an off-board STM micro-controller (μC), the input (write) and output (read) of the slave SPI on the circuit were compared at a clock frequency of 1 MHz with a bit frame length of 80 bit. The frame error rate is below 0.1 %, thus proving the functionality of the SPI.

A permanent magnet with its north pole on the top side was placed to the bottom of the test PCB with a vertical distance of 5 mm. As measured via a gauss metre (Lakeshore425), the permanent magnet generated an out-of-plane magnetic field H with around 1 kOe at the bottom of the PCB card. In addition, a DC current I_{DC} of 10 μA was injected. Via a self-developed software program that ran on the μC board, the STOs in the array were swept sequentially and their DC resistances were registered. As the first step, an MTJ device with a DC resistance of 920 Ω was chosen to be the device under test (DUT). To prove that the TMR effect exists in the selected MTJ, the magnet was flipped at the same location. Here, a 500-Ω increment of the DUT's resistance was seen, thus having verified the TMR effect in the DUT.

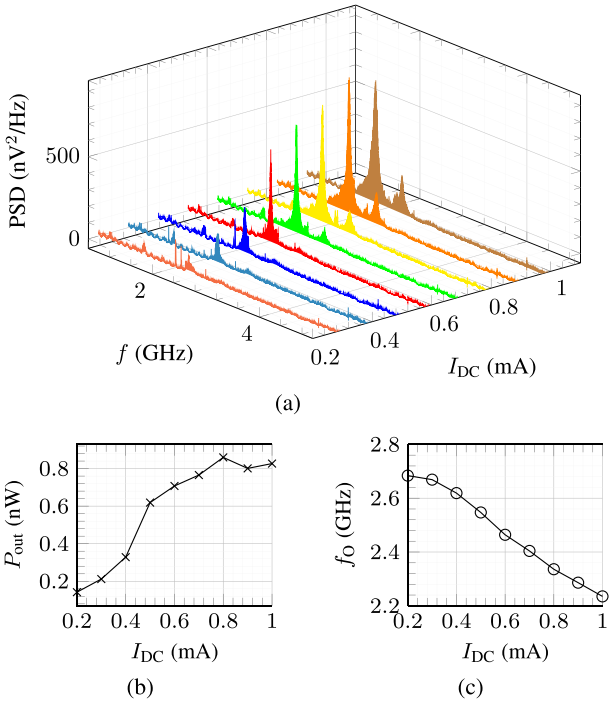

Fig 4 *(a) Measured output frequency spectra in dependence of I_{DC} for $H = 1$ kOe. (b) Measured MTJ-based STO's output power P_{out} and (c) centre oscillation frequency f_o in dependence of injected DC current I_{DC}*

To verify the microwave signal emission ability of the DUT, I_{DC} was swept from 0.3 to 1 mA with a step of 0.1 mA. Figure 4(a) depicts the measured power spectral density (PSD) versus I_{DC} of the DUT. Here, a clear PSD peak in dependency of I_{DC} can be seen, thereby proving that the DUT was able to generate microwave signals in accordance to its DC bias current. To better quantitatively analyse the MTJ-based STO's output power and oscillation frequency versus the injected DC current, the primary frequency peaks from Figure 4(a) are re-plotted in Figure 4(b) and (c), where the power gain of the PA and the power loss (−15 dB) due to the parasitics that arise in the inter-connections among STOs and switches, the PCB and cable losses are de-embedded. As can be seen, the steady-state oscillations appear in the range between 0.6 and 1.0 mA, where the centre frequency decreases from 2.464 to 2.235 GHz, the linewidth is below 200 MHz, the output power is between 0.72 and 0.88 nW, and the slope $\frac{\Delta f}{\Delta I_{DC}}$ is −229 MHz per 0.5 mA.

Conclusion: This letter has reported an MTJ-based 40 spintronic device array fully implemented in a hybrid CMOS–MTJ technology. According to measurement results, an STO from the array emitted microwave signals between 2.464 and 2.235 GHz with a power of 0.72−0.88 nW, when the external out-of-plane magnetic field was fixed at 1 kOe and the DC current varied from 0.6 to 1.0 mA. To the authors' best knowledge, this work has for the first time demonstrated the functionality of STOs that are fully implemented in a CMOS circuit.

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