Single-Event Latchup sensitivity: Temperature effects and the role of the collected charge

S. Guagliardo, Frédéric Wrobel, Ygor Quadros de Aguiar, Jean-Luc Autran, Paul Leroux, Frédéric Saigné, Vincent Pouget, Antoine Touboul

Cite this article as: S. Guagliardo et al., "Single-Event Latchup sensitivity: temperature effects and the role of the collected charge," in Microelectronics Reliability, vol. 119, April 2021, doi: 10.1016/j.microrel.2021.114087

Single-Event Latchup sensitivity: temperature effects and the role of the collected charge

S. Guagliardo[1], F. Wrobel[1], Y. Q. Aguiar[1,4], J-L Autran[2], P. Leroux[3], F. Saigné[1], V. Pouget[1] and A.D. Touboul[1]

[1]IES-UMR UM/CNRS 5214, Université de Montpellier, Montpellier, France, email : guagliardo@ies.univ-montp2.fr
[2]Institut Matériaux Microélectronique Nanoscience de Provence, Aix-Marseille Université, Marseille, France.
[3]Advanced Integrated Sensing Lab, KU Leuven University, Leuven, Belgium
[4]European Organization for Nuclear Research (CERN), CH-1211 Geneva, Switzerland

***Abstract* - Single-Event Latchup (SEL) is considered as a major reliability issue for the CMOS technology due to its capability of permanently damaging electronic components. In this work, the impact of temperature variation on the SEL mechanism is investigated. As the SEL sensitivity is influenced by design and environment parameters, the temperature variation is also evaluated along the variation of three parameters related to the geometry and to the design of the component: the doping profile, the anode to cathode spacing (A-C spacing) and the substrate and well taps placement. Moreover, the charge collection process has been analyzed. The goal was to verify whether the concept of critical charge, through studying the collected charge by the source implants, can be used for SEL, as it is used for upsets. 2D TCAD simulations have been performed, using an NPNP structure based on 65nm CMOS inverter. From these simulations, we have analyzed the threshold LET and SEL rate. Results show that temperature impact is stronger when the component is less sensitive to SEL. Moreover, charge collected has shown promising results about its usage for SEL.**

***Index Terms* – Single-Event Latchup, TCAD simulations, Cross section, temperature effects, Collected charge**

I. Introduction

SINGLE-Event Latchup (SEL) is a serious reliability concern for CMOS devices. It arises from the parasitic bipolar transistors that are structurally intrinsic to this technology [1]–[4]. General-purpose electronics are usually designed to operate at room temperature, i.e. 20 to 25 °C (68 to 77 °F). However, critical systems such as spacecraft electronics are subjected to large variation of temperature during a mission [5], [6]. As temperature is one of the most important parameters that influences the SEL sensitivity, the system vulnerability to SEL, if not well-understood, could be catastrophic due to a rise of temperature. Literature results have shown that the impact on the SEL cross section is dependent on the range of temperature considered [7]–[9]. Nonetheless, the SEL sensitivity is also influenced by a combination of numerous factors. For example, beside the environment impact, the component design characteristics must be carefully considered to determine the probability of SEL in a device. Different studies have been performed in which the vulnerability to SEL is investigated considering different design approaches. For instance, the doping profile, the substrate and well taps placement and the anode to cathode spacing have been investigated in the literature, revealing that the susceptibility to SEL is directly related to these parameters and they could be used to harden a component at design level [10]–[18].

However, it is of utmost importance to analyze the behavior of the SEL cross-section when these design methodologies are evaluated under the temperature variation. In our work, TCAD simulations have been performed to investigate the coupled effects of circuit design modifications and temperature variation. Firstly, we have analyzed the impact of the variation of the design parameters (the doping profile, the substrate and well taps placement and the anode to cathode spacing) on the SEL sensitivity. Then, considering a specific range of temperatures, we have investigated what is the role of the temperature on the SEL sensitivity when design parameters are modified. In order to achieve our goal, we have calculated the SEL cross-sections, following a 2D approach. In addition, the analysis has also been extended to address the implications on the in-orbit SEL rate for the Geostationary Earth Orbit (GEO).

Furthermore, TCAD simulators allow the calculation of the charge density induced by an energetic particle hitting in a device and the collected charge by the sensitive nodes of within the circuit. Generally, as for others Single-Event Effects, the Single-Event Upset (SEU) and the Single-Event Transient (SET), the charge collected in specific nodes can be used as an indicator of the SEE vulnerability of the circuit [19], [20]. Although the SEL triggering mechanism are also dependent on the charge deposition [21], due to its high complexity, it is not clear how a critical charge can be estimated to evaluate the overall sensitivity of a given design. In this context, in the second part of this paper, we investigated whether a critical charge collected in the source implants can be used as a figure-of-merit for the SEL evaluation of CMOS circuits.

The structure of the paper is the following: from the circuit design to the calculation of the SEL cross-section curves and estimation of the SEL rate, in Section II we explained the complete SEL characterization methodology used in this work. Additionally, we have also presented the two techniques used to calculate the collected charge involved during a particle event. In Section III, the results for the temperature effect analysis and for the different calculation of the collected charge are presented and discussed. Finally, Section IV includes an overview of the paper and our conclusions.

This work was realized within RADSAGA project. The RADSAGA Innovative Training Network project has received funding from the European Union's Horizon 2020 research and innovation program under the Marie-Skłodowska-Curie grant agreement number 721624.

II. METHODOLOGY

In order to investigate the SEL mechanism, a complete characterization methodology is proposed and shown in Fig. 1. It can be classified into three steps comprising from the circuit design and validation of the circuit structure to the in-orbit SEL rate estimation. The following subsection describe each step in further detail.

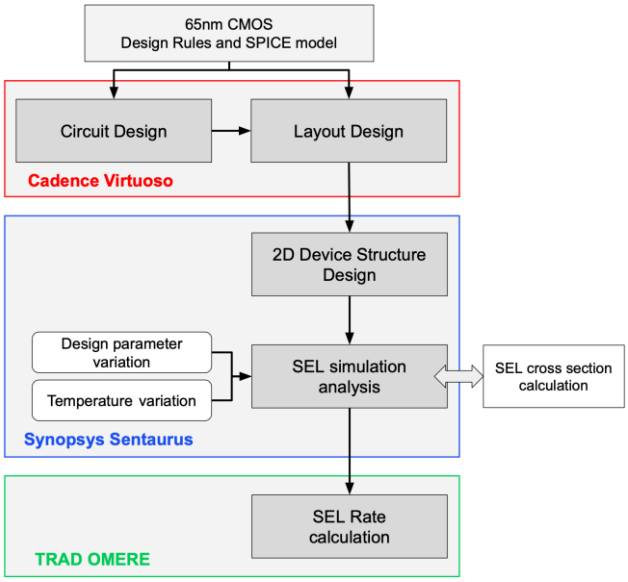


Fig. 1 Characterization methodology for Single-Event Latchup (SEL)..

A. *Device structure*

The first step was to design the physical layout of a CMOS inverter following the design rules of a commercially available bulk 65nm technology with Cadence Virtuoso. After the electrical and logical validation of the circuit, important parameters were extracted from the circuit and layout design for the device structure design using a TCAD tool. Based on the dimensions in the physical layout of the minimum-sized inverter, an NPNP structure (as shown in Fig. 3) has been retrieved for our analysis. This structure is formed by the PMOS and the NMOS source and well and substrate taps. This structure was chosen because it is not necessary to simulate the full CMOS inverter structure (Fig. *2*) to investigate SEL mechanisms [1].

The analysis has been performed with a specific TCAD simulator, called Sentaurus Synopsys. TCAD simulations have been extensively used in the literature and thanks to them, it is possible to investigate the mechanism of SEL by providing an insight view of the device. Due to the well-developed physical models available in TCAD tools, it is also possible to retrieve data that are useful to calculate parameters that are strictly related to radiation sensitivity, such as the cross-section and collected charge.

B. *Physical models*

In order to perform simulations on Sentaurus Synopsys we needed to choose between 2D or 3D simulations and the physical models to use. To achieve our goal, we have decided

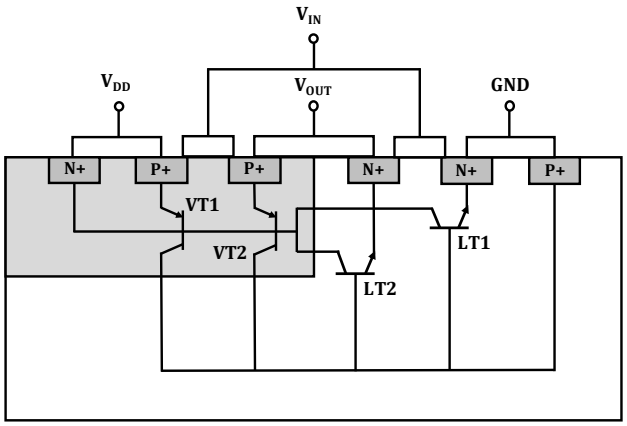


Fig. 2 Full CMOS inverter structure and the Latchup paths.

to perform 2D simulations. Despite the three-dimensional nature of the SEL mechanism, it has been demonstrated that 3D simulations follow the same trend as in 2D simulations [11], [22]. Thus, considering that we are interested in the trend of the cross-section, we have chosen to perform 2D simulations

As for the physical models, we have chosen proper models for a 65 nm technology and they have been based on previous works [9], [23], [24]. The hydrodynamic model has been chosen along with Fermi statistics as carrier transport model. The mobility was modelled with the built-in model by Arora [25], which is a doping and temperature dependent model. For recombination, the doping dependent Shockley-Read-Hall, Auger recombination and avalanche generation have been chosen. Finally, bandgap narrowing for high doped region has been selected.

Ion track has been generated through the built-in tool on Sentaurus Synopsys. A range of 2.3 µm in order to cover the entire structure with a constant linear energy transfer has been selected. The radial distribution has been set with a Gaussian profile with a 50 nm radius [12], [24].

C. *Temperature effects and cross-section calculation*

We have decided to investigate the effect of temperature on these design parameters: the doping profile of the whole structure, the well and substrate taps placement and the anode to cathode spacing (A-C spacing). The range of temperature chosen for this analysis was: 350 K, 375 K, 400 K and 425 K. As we have mentioned before, the susceptibility to SEL increases with the increase in temperature. Accordingly, we have chosen a set of temperature in which it was more likely to observe a Single-Event Latchup in the analyzed NPNP structure. Understanding the design parameters implications under high temperature will provide guidelines on how to harden components under extreme environments. Thus, we have chosen five values for each parameter to explore a broad range of possibilities. The substrate and well taps placement were investigated by symmetrically placing them further from the center of the physical layout, i.e. the boundary between the N-well and the P-substrate. The placement distances were the following: 1.05 µm, 1.25 µm, 1.55 µm, 1.85 µm and 2.15 µm by moving taps symmetrically further from the center, where 1.25 µm is the nominal value. In terms of doping concentration,

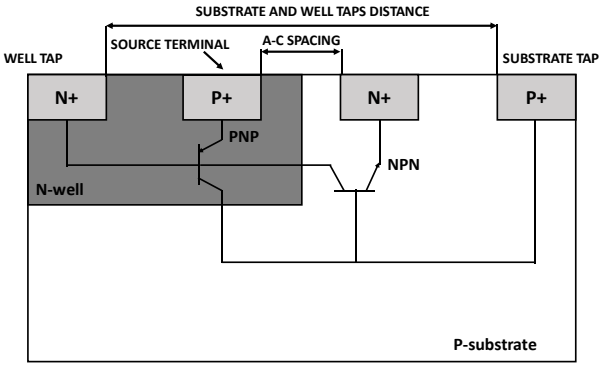


Fig. 3 Simplified NPNP structure used in our work. A-C spacing is depicted and substrate and well taps distance is depicted.

the reference doping profile of the whole structure is based on the information from a commercial bulk 65nm process. The modification was considered in the whole structure as the reference doping profile was multiplied by 0.75, 0.85, 1.15 and 1.25. And lastly, the evaluation of the A-C spacing was carried adopting the following values: 0.25 µm, 0.27 µm, 0.32 µm, 0.37 µm and 0.40 µm, where 0.32 µm is the nominal value.

After the implementation and validation of the NPNP structures considering each parameter variation, the following step is to calculate the SEL cross-section for every study case. To do so, we followed the approach as reported in [26]. To perform this step, it is necessary to identify the particle Linear Energy Transfer (LET) value that triggers the SEL mechanism for different positions along the device (strike position in Fig. 5). The particle LET refers to the amount of energy that an ionizing particle deposit along the ionizing track. Thus, in this procedure, we seek to obtain the minimum LET value in which a particle is able to induce a steady current in the P+ diffusion, i.e. an SEL. As an example, in Fig. 4, the P+ diffusion currents are shown when the SEL is triggered and when it is not. Then, with the threshold LET value for each position along the device structure, a sensitivity mapping, as the one shown in Fig. 5, is created for the estimation of the sensitive zones. For a given LET value LET_x, the sensitive zone refers to the portion of the device where the minimum LET to induce an SEL is lower than LET_x. After identifying the sensitive zone of the device for a given particle LET, the SEL cross-section can be estimated by multiplying the sensitive zone by the width of the component, which is constant and equal to 0.88 µm. What we obtain is the area of the device (seen from the top) in which the impact of an ion with a specific LET, would trigger SEL. An example of an SEL cross-section curve is shown in Fig. 6. In this figure, it is shown the SEL cross-section for four different temperature versus the LET. In the last step in Fig. 1, the 2D cross-section curves have been used to evaluate the SEL rate. In this way, we have analyzed the sensitivity of the device for the whole LET range and not only in the term of threshold LET. Hence, when specific parameters are selected for a design, these results can indicate if temperature variation will strongly modify the SEL vulnerability of the circuit. The in-orbit SEL rate is estimated through the convolution of the cross-section curve with particle flux in the Geostationary Earth Orbit (GEO) under solar minima. For this purpose, the software OMERE is used which is a well-known tool dedicated to space environments [27].

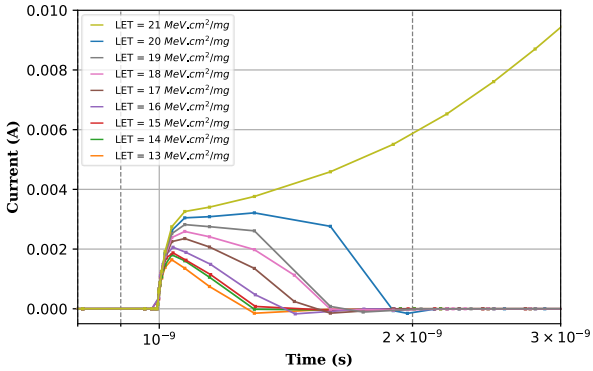


Fig. 4 P+ diffusion currents for sustained latchup current (red) and non-sustaining current for different LET values.

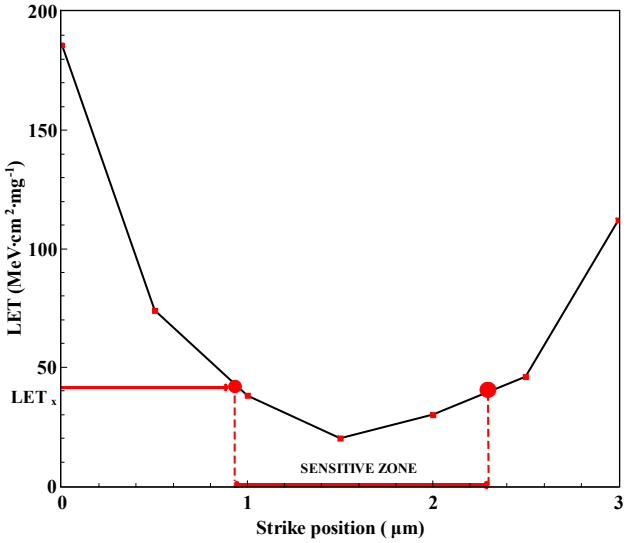


Fig. 5 Minimum LET value to trigger SEL versus position along the component.

D. *Charge collection calculation*

Besides the verification of the temperature and design variation impact on the circuit robustness to SEL, we have also investigated the role of the charge collection in the triggering mechanism. Accordingly, as it is usually used in the SEL characterization simulation using SPICE, the charge collection is calculated at the source terminal [24]. As aforementioned, the threshold LET has been calculated for each different position in the component structure. In order to calculate the threshold LET, we have performed simulations, for each position where the LET is increased by a 1 MeV.cm^2/mg step, until the SEL is observed. Once the SEL occurs, we have retrieved the induced current at the source terminal for the threshold LET and for the previous LET value in which SEL does not occur (that we called "NO SEL").

Eventually, the collected charge (Q_{COLL}) is calculated by integrating the current over time. The time interval has been chosen with two different criteria. To explain the first criterion, we need to observe the Fig. 7 in which the source current is shown for increasing LET. When the SEL is not triggered, after the ion strike, the source current increases, it reaches a peak, and then it drops to zero. As the LET increases, more charge is

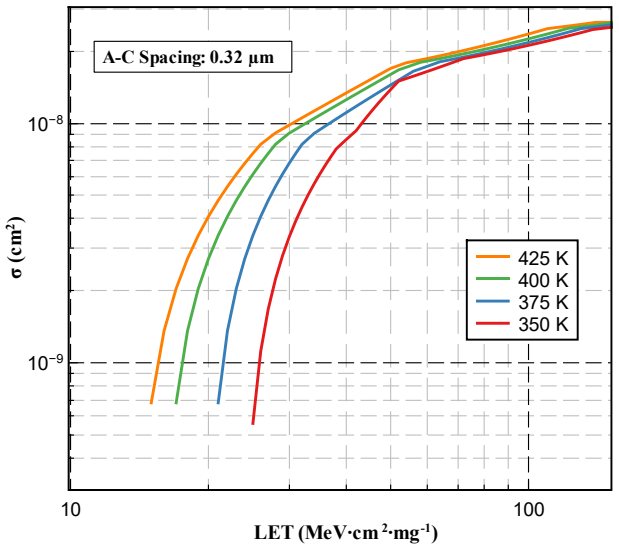


Fig. 6 Example of SEL cross-section curve calculated by 2D approach. It shows the variation of cross-section (σ) for different temperatures.

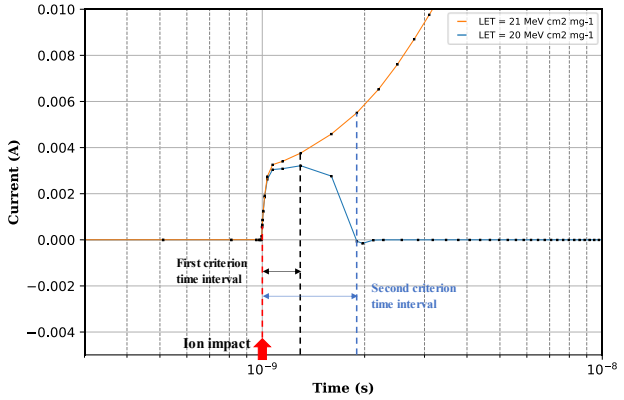


Fig. 7 Representation in the current versus time chart of the two different time intervals used as criterion in this work.

deposited in the device, then the peak increases. When the SEL occurs, the current follows the same trend until a certain timestep, when the current increases and reaches a saturation value. Then, we can assume that the time at which the peak is reached, it is the time at which the parasitic transistors are turning off and so, the time in which the SEL is no longer sustained in the device. In conclusion, the time interval is taken from the moment the ion impacts within the structure ($1x10^{-9}$ s) until it reaches the peak for the no-SEL case. The same interval is used when SEL occurs, as indicated in Fig. 7.

Instead, the second criterion takes into account the time at which the current (for no-SEL) reaches zero. At this timestep, we can assume that the parasitic transistors are definitively off. This timestep is used also for the case in which SEL occurs. So, the time interval would be between the impact of the ion and the moment in which the current drops to zero, also shown in Fig. 7.

For both criteria, aside the collected charge, we have also calculated another parameter, that we called the charge collection rate, Q_R and it is calculated following Eq. 1:

$$Q_R = Q_{COLL}/\Delta t \qquad (1)$$

where Q_{COLL} is the charge collected in the source terminal and Δt is the time interval in which the charge is collected. In this way, we are able to consider if the time in which the charge is collected plays a role in the Single-Event Latchup triggering mechanism. Eventually, the two used criteria for the time intervals are depicted in Fig. 7.

III. Results and Discussion

A. *Threshold LET*

First, in Fig. 8, the threshold LET trend for the doping profile is shown. As expected, threshold LET decreases as the temperature increases and increases as the doping profile increases [10]. If we consider the condition in which the device design is more favorable to induce Single-Event Latchup, as the worst-case scenario (lowest threshold LET, i.e. lower doping level) and the best-case scenario as the opposite, we can observe that the threshold LET difference for each single doping case, increases as the conditions become less favorable to SEL. In fact, in the worst-case scenario, the difference between the threshold LET at 425 K and at 350 K is about 50%. On the other hand, when considering the best-case scenario, i.e. high doping profile concentration, the design goes from being SEL-hardened to SEL-sensitive. For example, at 350 K, no SEL is observed for the designs with doping profile concentration x1.15 and x1.25, which are thus the best condition for immunity.

In Fig. 9, the threshold LET curves for substrate and well taps placement are shown. The threshold LET decreases as the temperature increases; at the same time, if the distance between the substrate and the well taps increases, the threshold LET also decreases. Furthermore, temperature influence can be also seen in this case. In the worst-case scenario, the difference between 350 K and 425 K is about 50% and as we have seen previously, for the best-case scenario the temperature impact becomes more prominent. Indeed, threshold LET is increased by 75% just between 425 K and 375 K and at 350 K SEL is not even observed.

Eventually, in Fig. 10 threshold LET curves for anode to cathode spacing are shown. The trend that has been observed for the previous parameters is also verified for the A-C spacing. Regarding this condition, in the worst case, threshold LET between the lower and the higher temperature increases by 58%, meanwhile in the best-case scenario threshold increases by 53% between 425 K and 375 K and SEL is not reached for 350 K. In this case, the difference is smaller with respect to previous examples. The reason may be that the effects of anode to cathode spacing variation is lower with respect to the previous parameters.

In conclusion, for all the parameters investigated herein, the temperature influence on SEL sensitivity is lower when conditions are more favorable to SEL and increases as parameters are modified to make the component less sensitive (i.e. higher threshold LET). In other words, it means that by adopting hardening approaches considering only a nominal temperature, the designer might be worsening the robustness of

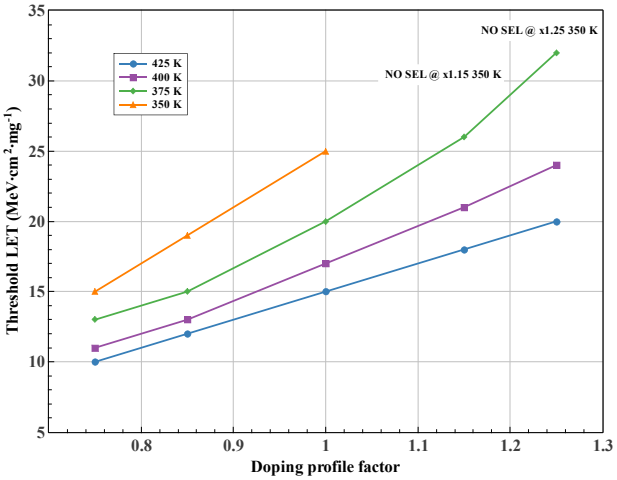


Fig. 8 Threshold LET vs doping profile for four different temperatures (350 K, 375 K, 400 K and 425 K).

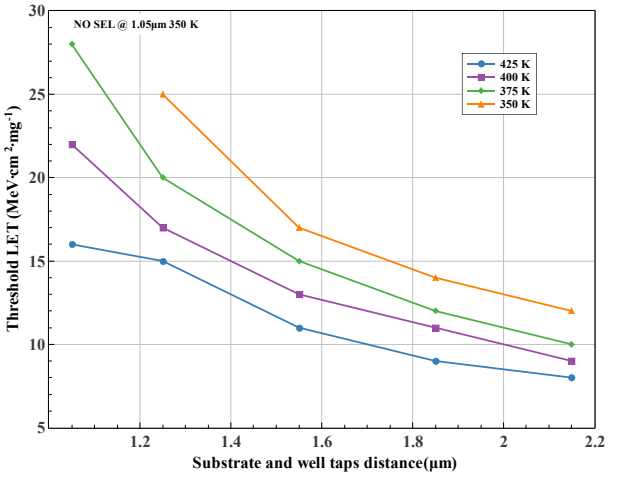


Fig. 9 Threshold LET vs substrate and well taps distance for four different temperatures (350 K, 375 K, 400 K and 425 K).

the circuit under temperature variation. To further investigate this phenomenon, in the next subsection we provide the SEL rate for each scenario.

B. *SEL rate*

The cross-sections curves calculated with the 2D approach, as the one shown in Fig. 6, have been used to calculate the SEL rate. The results for the doping profile, presented in Fig. 11, indicate that the SEL rate follow the same trend observed for threshold LET.

Considering that SEL rate takes into consideration the whole cross-section, it means that the trend that has been seen for the threshold LET is present even for higher LET. Considering 425 K as a reference, SEL rate increases from 30% (between 425 K and 400 K) to 40% (between 375 K and 350 K) for the worst case (x0.75), it increases from 40% to 80% when reference doping profile is analyzed, and increases from 70% to 97% for the best-case scenario (x1.25, which is not calculated at 350 K because no SEL was observed). In Fig. 12, it is shown the SEL rate for substrate and well taps placement. Even in this case, the trend is also verified. SEL rate increases from 35% to 40% for the best-case scenario and it increases from 65% to 88% in the

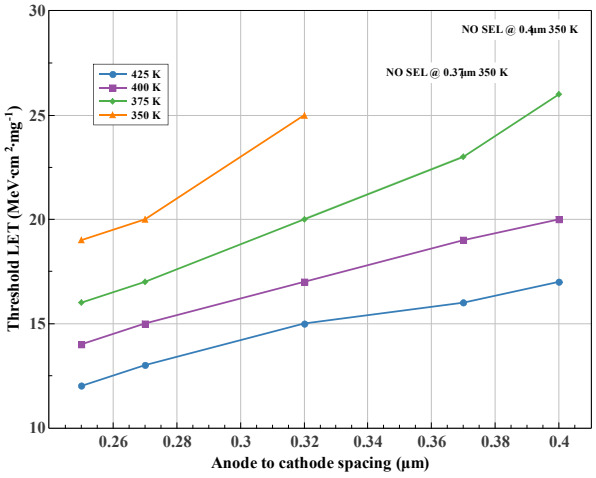


Fig. 10 Threshold LET vs anode to cathode spacing for four different temperatures (350 K, 375 K, 400 K and 425 K).

worst-case scenario. Eventually, SEL rate for A-C spacing is presented in Fig. 13 where it varies from 46% to 82% for the best case and from 37% to 54% in the worst case.

C. *Collected charge*

When an ion hits a component, electron-hole pairs are generated along its track and carrier diffusion and drift take place within the device [28]. If the charge collected is enough to switch the parasitic transistor *on*, an SEL will occur [21]. In this context, we have investigated the charge collection for the different cases to verify whether the concept of the "critical charge", as used for other Single-Event Effects, can be used for SEL.

In order to calculate the collected charge Q_{COLL}, we have used the two methodologies shown in section II-D. In the next figures, we show the charge collected for each temperature simulated, when the SEL is observed (red dots) and when it is not (blue dots) for all parameter modification. As we want to define a critical charge for SEL, we should be able to distinguish the collected charge that activates the Latchup mechanism from the case where SEL is not observed. In other words, the charge collection calculation methods presented in II-D should be reliable on defining the boundary between the SEL case and no-SEL case so the critical charge can be effectively identified. In Fig. 14, the results for the four different temperatures (350 K, 375 K, 400 K, 425 K), are shown. Based on this data, we cannot identify clear distinction from the Q_{COLL} that leads to SEL or not. Thus, it is not possible to define a critical charge that would trigger the SEL. Furthermore, we have calculated the charge collection rate Q_R, with the previous methodology and also in this case, results show no distinction.

Despite a clearer difference, the goal is not reached also when the second criterion is applied as shown in Fig. 15. At all temperature the Q_{COLL} that induced an SEL overlaps with the cases where no-SEL is observed in the circuit. In Fig. 16, we present the Q_R estimated with the Q_{COLL} calculated with the second criterion. With this method, the difference between the charge collected for SEL and no-SEL is more distinct. Considering all the cases (which represents 420 simulations), only in 10 cases the results overlap. Also, at lower temperature

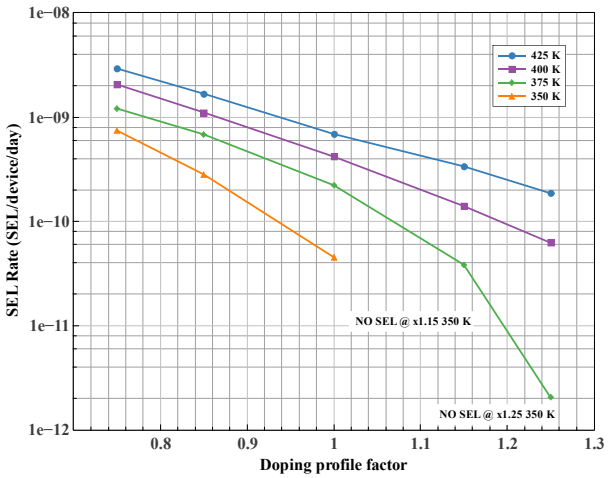


Fig. 11 SEL rate vs doping profile for four different temperatures at GEO orbit (350 K, 375 K, 400 K and 425 K).

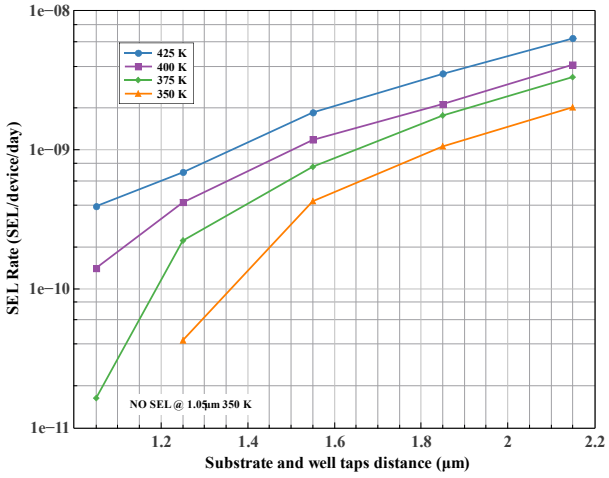


Fig. 12 SEL rate vs substrate and well taps distance for four different temperatures at GEO orbit (350 K, 375 K, 400 K and 425 K).

the results are slightly worse with respect to higher temperatures.

D. Discussion

1) Threshold LET and SEL Rate

From the results it can be observed that temperature plays a complex role depending on the condition of the device. When conditions of the device are favorable to SEL, i.e. low threshold or high SEL rate, the temperature variation is affecting threshold LET and SEL rate less relevantly than it would in the case where device is more hardened, i.e. high threshold LET or low SEL rate. It means that, in the end, by adopting process or design based hardening techniques, the applicability of the hardened design will be constrained by the temperature variation more than an unhardened design.

In order to explain that, SEL triggering conditions must be considered. The structure of the CMOS creates two parasitic transistors inside it. The activation of these transistors is the initial step for the Single-Event Latchup. Hence, a parasitic circuit is created within the structure as depicted in Fig. 1. It was shown that the characteristic of this parasitic circuit is related to the design of the device [29]. Accordingly, any variation of a design parameter leads to a variation of the

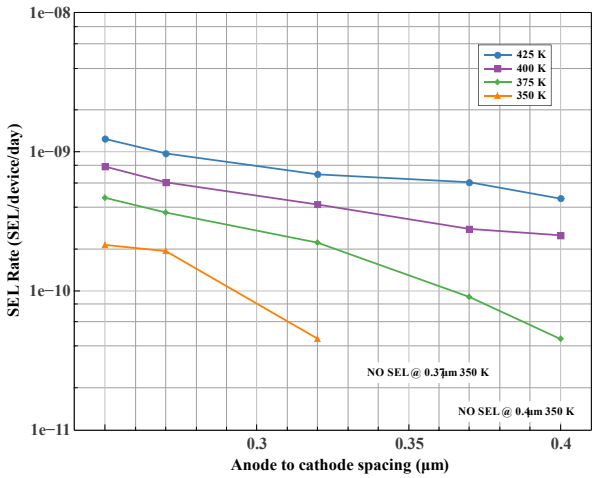


Fig. 13 SEL rate vs anode to cathode spacing for four different temperatures at GEO orbit (350 K, 375 K, 400 K and 425 K).

response of the circuit, i.e. a variation on the SEL sensitivity. Specifically, the doping profile influences the PNP bipolar current gain and the resistances inside the device [10]. For instance, a lower doping profile leads to a higher resistance. This mean that for the same amount of charge a higher potential drop can be obtained inside the structure and thus it is more likely to trigger the parasitic transistor. Similarly, the substrate and well taps placement variation causes a modification of the resistances present inside the device. A lower resistance (i.e. smaller distance between the taps) will reduce SEL sensitivity, meanwhile a higher resistance will increase it. Concerning the A-C spacing, if it is increased, the bipolar current gain is decreased (similar to what is observed for the doping profile). Eventually, temperature modification will cause a change on the resistances and it will modify the forward bias voltage of the base-emitter junction [30]. A variation of this parameter leads to a variation of the potential barrier needed to trigger an SEL [24].

However, the SEL sensitivity is clearly dependent not only to a single parameter directly, but to the combination of them in a very complex way. This work shows that for all the parameters (doping profile, substrate and well taps placement and A-C spacing) a more relevant variation of threshold LET and SEL rate is obtained for the best-case scenario, with respect to the worst-case scenario. We can say that in the best-case scenario, the conditions are already favorable for the SEL immunity and then the decrease of temperature will help to increase SEL immunity of the device. Meanwhile, in the worst-case scenario, the device situation is already on SEL favor. Then, temperature will have a lower impact on SEL sensitivity. In general, it can be considered that temperature impact is not equal in all conditions and it is not independent from device design.

2) Charge collection

As aforementioned, the goal was to obtain a value of critical charge able to trigger an SEL. Once obtained, this value can be used in SPICE and Monte Carlo simulations to estimate SEL sensitivity of the devices.

The collected charge has been calculated following two different procedures for the time interval. Furthermore, a

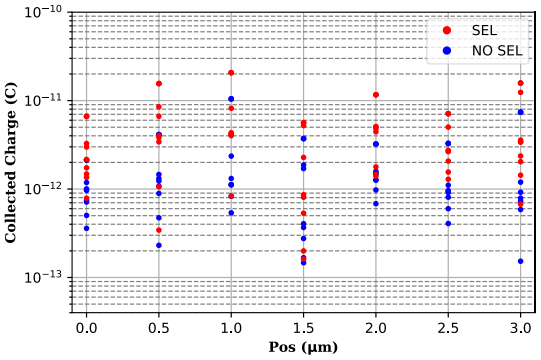


Fig. 14 Collected charge when no clear distinction is achieved.

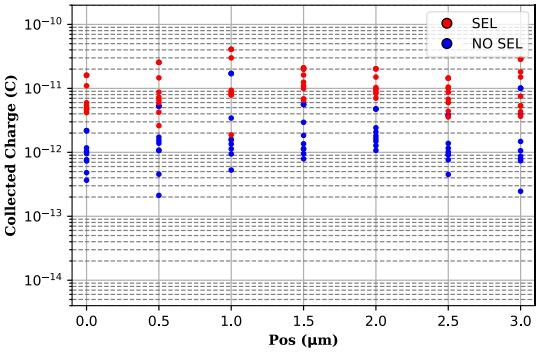
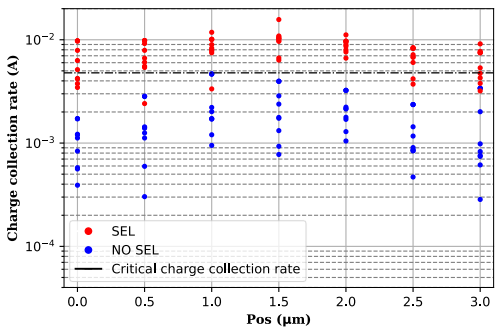
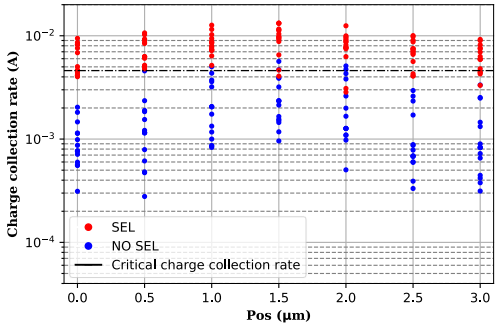


Fig. 15 Collected charge calculated base on the second criterion. No possible distinction among the SEL and no-SEL cases.

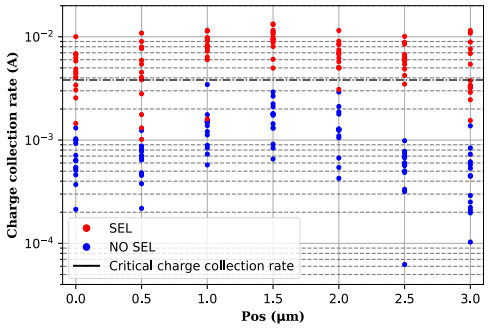
second parameter has been calculated, that is the charge collection rate. In the following figures (Fig. 14, Fig. 15, Fig. 16), each single dot represents a single simulation, with different parameters. The only common value
is the temperature. In Fig. 14, we show an example of the results, where no critical charge value has been found for these cases. Indeed, it is not possible to find a threshold value for the collected charge or for the charge collection rate. More specifically, when the first criterion is used, SEL and NO SEL collected charge overlap continuously for all the temperature investigated. Meanwhile, when the second criterion is applied, they overlap less in comparison to the previous criterion. Furthermore, when the second criterion is applied and the charge collection rate is calculated, the results show a clearer distinction between SEL and NO SEL collected charge (Fig. 16). Moreover, in Fig. 16, we depicted what we called critical charge collection rate. Specifically, this value is the mean of all the values collected at the same temperature. In this way, we represent the average value of the charge collection rate needed to trigger the SEL, regardless the position. We can see that, using these values as a critical value, will allow to obtain a SEL in most of the cases. Also, these values decrease as temperature increases. This means that at higher temperature less charge is needed to trigger an SEL, explaining why at higher temperature SEL sensitivity increases.



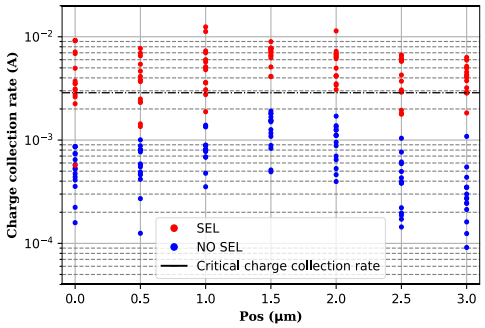
(a)



(b)



(c)



(d)

Fig. 16 Charge collection rate using the second criterion at 350 K (a), 375 K (b), 400 K (c) and 425 K (d).

To conclude, from these data, it can be said that the first criterion is not useful for our purpose. Meanwhile, the second criterion seems more promising and specifically, it shows that the time in which the charge is collected can play an important role in SEL triggering. This method can be refined by using a smaller maximum simulation timestep, which would help to refine the time interval used in the calculation.

IV. Conclusion

Single-Event Latchup (SEL) poses a threat to the reliability of critical systems. Due to its high thermal dependence, circuit designers must imperatively characterize electronic components under the temperature variation foreseen for the system application. In this context, this work has provided an in-depth analysis of the implications of hardening strategies in the design levels under temperature effects, such as the variation on the doping profile, the well and substrate taps placement and the A-C spacing.

The cross-section curves for each parameter have been calculated using 2D TCAD simulations and then the SEL rate has been estimated considering the GEO orbit. For every parameter, the temperature increase has shown a decrease in the threshold LET and an increase in the SEL rate. However, this thermal effect shows to be more prominent for the designs considered more radiation tolerant in the room temperature characterization. These findings highlight the importance of evaluating electronic components under temperature variation, especially when adopting hardening techniques. In the second part of this paper, we have also investigated whether the charge collection by the source terminal of a device can be used as a figure-of-merit for the SEL characterization at circuit level.

Two estimation techniques have been proposed to calculate the collected charge involved in the SEL triggering. The results show that the collected charge divided by the time interval in which it is collected is a promising methodology.

Acknowledgement

This work was realized within RADSAGA project. The RADSAGA Innovative Training Network project has received funding from the European Union's Horizon 2020 research and innovation program under the Marie-Skłodowska-Curie grant agreement number 721624.

References

[1] G. Bruguier and J.-M. Palau, 'Single particle-induced latchup', *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, pp. 522–532, Apr. 1996, doi: 10.1109/23.490898.

[2] T. Aoki, 'Dynamics of heavy-ion induced latchup in CMOS structures', *IEEE Transactions on Electron Devices*, vol. 35, no. 11, pp. 1885–1891, Nov. 1998.

[3] M. Shoga and D. Binder, 'Theory of Single Event Latchup in Complementary Metal-Oxide Semiconductor Integrated Circuits', *IEEE Trans. Nucl. Sci.*, vol. 33, no. 6, pp. 1714–1717, 1986, doi: 10.1109/TNS.1986.4334671.

[4] A. H. Johnston, 'Mechanisms for single-particle latchup in CMOS structures', in *RADECS 93. Second European Conference on Radiation and its Effects on Components and Systems (Cat. No.93TH0616-3)*, St. Malo, France, 1994, pp. 433–437, doi: 10.1109/RADECS.1993.316564.

[5] W. A. Kolasinski, R. Koga, E. Schnauss, and J. Duffey, 'The effect of elevated temperature on latchup and bit errors in CMOS devices', *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, pp. 1605–1609, 1986.

[6] R. L. Patterson, A. Hammoud, and M. Elbuluk, 'Electronic components for use in extreme temperature aerospace applications', 2008, p. 28.

[7] A. H. Johnston, B. W. Hughlock, M. P. Baze, and R. E. Plaag, 'The effect of temperature on single-particle latchup', *IEEE Trans. Nucl. Sci.*, vol. 38, no. 6, pp. 1435–1441, Dec. 1991, doi: 10.1109/23.124129.

[8] H. Iwata and T. Ohzone, 'Numerical simulation of single event latchup in the temperature range of 77-450 K', *IEEE Trans. Nucl. Sci.*, vol. 42, no. 3, pp. 148–154, Jun. 1995, doi: 10.1109/23.387354.

[9] A. A. Youssef, L. Artola, S. Ducret, G. Hubert, and F. Perrier, 'Analysis of low temperature on single event Latchup mechanisms by TCAD simulations for applications down to 50K', in *2016 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Bremen, Sep. 2016, pp. 1–5, doi: 10.1109/RADECS.2016.8093175.

[10] N. Rezzak and J.-J. Wang, 'Single Event Latch-Up Hardening Using TCAD Simulations in 130nm and 65nm Embedded SRAM in Flash-Based FPGAs', *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1599–1608, Aug. 2015, doi: 10.1109/TNS.2015.2450210.

[11] J. M. Hutson, R. D. Schrimpf, and L. M. Massengill, 'The Effects of Scaling and Well and Substrate Contact Placement on Single Event Latchup in Bulk CMOS Technology', in *2005 8th European Conference on Radiation and Its Effects on Components and Systems*, Cap d'Agde, France, Sep. 2005, pp. PC24-1-PC24-5, doi: 10.1109/RADECS.2005.4365577.

[12] A. A. Youssef, 'Etude par modélisation des évènements singuliers (SET/SEU/SEL) induits par l'environnement radiatif dans les composants électroniques', Université Toulouse 3 Paul Sabatier, 2017.

[13] H. de La Rochette, G. Bruguier, J. M. Palau, J. Gasiot, and R. Ecoffet, 'The effect of layout modification on latchup triggering in CMOS by experimental and simulation approaches', *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2222–2228, Dec. 1994, doi: 10.1109/23.340566.

[14] J. M. Hutson *et al.*, 'Evidence for Lateral Angle Effect on Single-Event Latchup in 65 nm SRAMs', *IEEE Trans. Nucl. Sci.*, vol. 56, no. 1, pp. 208–213, Feb. 2009, doi: 10.1109/TNS.2008.2010395.

[15] J. M. Hutson, 'Single event Latchup in a deep submicron CMOS technology', Vanderbilt University, Nashville, TN, 2008.

[16] A. A. Youssef, L. Artola, S. Ducret, G. Hubert, and F. Perrier, 'Investigation of Electrical Latchup and SEL Mechanisms at Low Temperature for Applications down to 50K', *IEEE Trans. Nucl. Sci.*, pp. 1–1, 2017, doi: 10.1109/TNS.2017.2726684.

[17] A. H. Johnston, 'The influence of VLSI technology evolution on radiation-induced latchup in space systems', *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 505–521, Apr. 1996, doi: 10.1109/23.490897.

[18] N. A. Dodds *et al.*, 'SEL-Sensitive Area Mapping and the Effects of Reflection and Diffraction From Metal Lines on Laser SEE Testing', *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2550–2558, Aug. 2013, doi: 10.1109/TNS.2013.2246189.

[19] T. Heijmen, D. Giot, and P. Roche, 'Factors That Impact the Critical Charge of Memory Elements', in *12th IEEE International On-Line Testing Symposium (IOLTS'06)*, Como, Italy, 2006, pp. 57–62, doi: 10.1109/IOLTS.2006.35.

[20] R. B. Schvittz, Y. Q. Aguiar, F. Wrobel, J.-L. Autran, L. S. Rosa jr, and P. F. Butzen, 'Comparing analytical and Monte-Carlo-based simulation methods for logic gates SET sensitivity evaluation', *Microelectronics Reliability*, p. 6, 2020.

[21] Steven H. Voldman, *Latchup*. John Wiley & Sons, 2007.

[22] Y. Moreau *et al.*, 'The latchup risk of CMOS-technology in space', *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1831–1837, Dec. 1993, doi: 10.1109/23.273473.

[23] Y. Gawlina, L. Borucki, G. Georgakos, and G. Wachutka, 'Transient 3D Simulation of Single Event Latchup in Deep Submicron CMOS-SRAMs', in *2009 International Conference on Simulation of Semiconductor Processes and Devices*, San Diego, CA, USA, Sep. 2009, pp. 1–4, doi: 10.1109/SISPAD.2009.5290213.

[24] L. Artola, G. Hubert, and T. Rousselin, 'Single-Event Latchup Modeling Based on Coupled Physical and Electrical Transient Simulations in CMOS Technology', *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3543–3549, Dec. 2014, doi: 10.1109/TNS.2014.2362857.

[25] N. D. Arora, J. R. Hauser, and D. J. Roulston, 'Electron and hole mobilities in silicon as a function of concentration and temperature', *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 292–295, Feb. 1982, doi: 10.1109/T-ED.1982.20698.

[26] H. de La Rochette, G. Bruguier, J.-M. Palau, J. Gasiot, and R. Ecoffet, 'Simulation of heavy ion latchup cross section curves', in *Proceedings of the Third European Conference on Radiation and its Effects on Components and Systems*, Arcachon, France, 1996, pp. 359–364, doi: 10.1109/RADECS.1995.509803.

[27] A. Varotsou, 'OMERE 5.0, 2017, [Online]'. http://www.trad.fr/en/download/omere-us/.

[28] P. E. Dodd, 'Physics-based simulation of single-event effects', *IEEE Trans. Device Mater. Relib.*, vol. 5, no. 3, pp. 343–357, Sep. 2005, doi: 10.1109/TDMR.2005.855826.

[29] S. Guagliardo *et al.*, 'Single Event Latchup Cross Section Calculation from TCAD Simulations – Effects of the Doping Profiles and Anode to Cathode Spacing', *19th European Conference on Radiation and Its Effects on Components and Systems (RADECS), to be published*, p. 4.

[30] S. Guagliardo *et al.*, 'Effect of Temperature on Single Event Latchup Sensitivity', in *2020 15th Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Marrakech, Morocco, Apr. 2020, pp. 1–5, doi: 10.1109/DTIS48698.2020.9081275.