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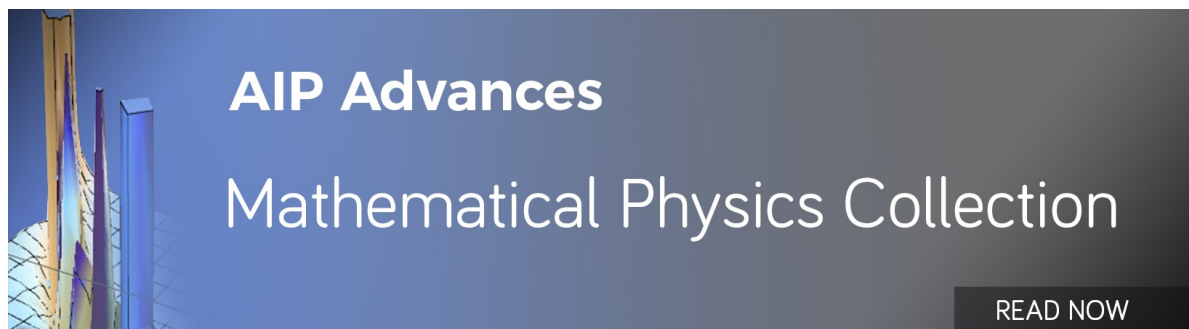
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Optimization of pentacene double floating gate memories based on charge injection regulated by SAM functionalization

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Pentacene based double nano-floating gate memories (NFGM) by using gold nanoparticles (Au NPs) and reduced graphene oxide (rGO) sheets as charge trapping layers are prepared and demonstrated. Particularly, the NFGM chemically treated by 2,3,4,5,6-pentafluorobenzenethiol (PFBT) self-assembled monolayers (SAM) exhibits excellent memory performances, including high mobility of $0.23 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, the large memory window of 51 V, and the stable retention property more than 10^8 s. Comparing the performances of NFGM without treating with PFBT SAM, the improving performances of the memory devices by SAM modification are explained by the increase of charge injection, which could be further investigated by XPS and UPS. In particular, the results highlight the utility of SAM modulations and controlling of charge transport in the development of organic transistor memories. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>). <https://doi.org/10.1063/1.5010403>

I. INTRODUCTION

Nonvolatile organic memories have been extensively studied and considered as the candidate of next-generation flash memories because of the advanced advantages, such as flexibility, low-cost fabrication, and large areas.^{1–6} Among the many possible device configurations of organic memories, tremendous efforts have been devoted to the development of nano-floating gate memory (NFGM) towards high performance memory devices, due to its spatially discrete floating-gate elements effectively as a charge trapping site between two dielectrics to store and erase the information.⁷ As a consequence, NFGM exhibit high speed operation, superior reliability, and to be scaled down.^{8–10}

In the past of years, much works has been focused on developing new materials and structures to get higher performances of NFGM.¹¹ For instance, Dong-Yu Kim et al used different kinds of charge trap metallic nanoparticles to obtain larger memory window,¹² the authors in Refs. 3, 13 achieved the NFGM with better retention properties by altering gold nanoparticles (Au NPs) and rGO sheets as double floating-gate, Wei Huang et al improved the operation current on/off ratio by changing the properties of tunneling layer,¹⁴ very recently, Ye Zhou et al deduced the working voltage through tuning the way of storing signals.¹⁵ Nevertheless, all the research reported in the previous is related to modify the trap levels, trap sites, structures, or semiconductors. Therefore, developing a new and an appropriate way to tune the number of charge traps or charge carriers is necessary for technological applications in NFGM.

As the connection of semiconductor to peripheral circuitry in electronic device, it signifies to explore the way of the charge transport between semiconductors and electrodes.¹⁶ On the research

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of organic transistors, an important approach to tuning charge transport is inserting self-assemble monolayers (SAM) on the surface of electrodes.^{17–19} A number of thiol-based SAM such as 1-hexadecanethiol,²⁰ 4-fluorothiophenol, and 2,3,4,5,6-pentafluorobenzenethiol (PFBT),^{21,22} deposited on the electrodes have demonstrated improvements to the charge injection and channel transistor performance. However, concerning about the influence of charge injection on the performances of NFGM has not been reported yet. In this paper, we present the pentacene based double NFGM with/without PFBT SAM modification by using Au NPs and rGO sheets as charge trapping layers. Particularly, the NFGM with PFBT SAM modification demonstrated optimized memory performances, which further highlights the utility of surface modulations to tune the charge storage/release behaviors in transistor memories.

II. EXPERIMENT

In this work, N-type Si (380~400 μm thick, resistivity of 0.001-0.003 $\Omega\text{-cm}$) with 200 nm thick SiO_2 were used as the substrate, acting as the gate and blocking dielectric layers, respectively. The substrate was cleaned by sonication in sequential baths of acetone, and isopropanol for 10 min each, and dried by blowing N_2 gas (99.9 % purity) at room temperature, then oxidized the surface with ultraviolet ozone for 25 min and immersed in piranha solution for 15 min to get silanol Si-OH anchoring groups for SAM. Then, the sample was immersed into solution of (3-Aminopropyl)trimethoxysilane for 1 h to form a positively charged $\text{NH}_2/\text{NH}_3^+$ -terminated SAM, and dipped into the negatively charged citrate-reduced Au NPs solution (the average diameter of the Au NPs is 10 nm) for 2 h to obtain the lower floating gate layer of Au NPs matrix.

To prepare the upper floating gate layer, the pristine graphene monolayer flakes solution (purchased from graphene laboratories Inc. with concentration of 1 mg/L, average thickness of 0.35 nm and lateral size of ~ 550 nm) was drop casted five times with an annealing at 80 $^\circ\text{C}$ for 5 min after each drop to form rGO sheets. The same preparation processes of Au NPs and rGO has been reported by our group refs. 13, 23. After the fabrication of floating gates, a 10 nm thin layer Al_2O_3 was deposited by atom layer deposition method to be a tunneling layer, and the thickness of Al_2O_3 was verified by ellipsometry. The bottom contact of gold source and drain electrodes were fabricated by e-beam lithography with a channel length of 5 μm and a width 1000 μm , respectively. SAM molecules of PFBT were prepared by immersing in the solutions of PFBT mixed in ethanol with a ratio of 1:10 for 18 hours. At last, 30 nm thick pentacene semiconductor was deposited by using a thermal evaporator at a deposition rate of 0.2 $\text{\AA}/\text{s}$ under 2×10^{-6} Torr at room temperature. A sample of pentacene transistor without SAM treatment was fabricated as a reference.

During the measurements, the atom force microscopy (AFM) and scanning electrons microscopy (SEM) were used to analyze the thin film surface morphology. The modification of Au electrodes with PFBT and pentacene deposited with SAM were analyzed by x-ray photoelectron spectroscopy (XPS) and UV-photoelectron spectroscopy (UPS). The electrical performances are operated in the glove box ($\text{O}_2 < 1$ ppm, $\text{H}_2\text{O} < 1$ ppm) by using the Semiconductor Measurement Unit “Agilent 4156C instrument”.

III. RESULTS AND DISCUSSION

The configuration of pentacene based double NFGM device with PFBT SAM modification surfaces is shown in figure 1(a). Figure 1(b) shows the high resolution of XPS spectrum of PFBT modified Au with a clear peak at 687.5 eV associated with F 1s, a clear signature of PFBT molecules,²¹ indicating that the PFBT monolayer is well deposited on the gold and without any molecular clusters. Figure 1(c) and (d) show the SEM images of Au NPs and Au NPs covered with rGO sheets, respectively. As we can see, the Au NPs with 10 nm diameter were uniformly dispersed on the solid surface without aggregation, which could limit the flow of charges by electrostatic repulsion between neighboring Au NPs. The density of Au NP reaches up to $\sim 1.1 \times 10^{11}$ cm^{-2} and the rGO sheets formed on the Au NPs with a surface cover percentage $\sim 70\%$, which is sufficiently obtain high performance of NFGM from the report of Ref. 3. Figure 1(e) displays the AFM morphology of pentacene thin

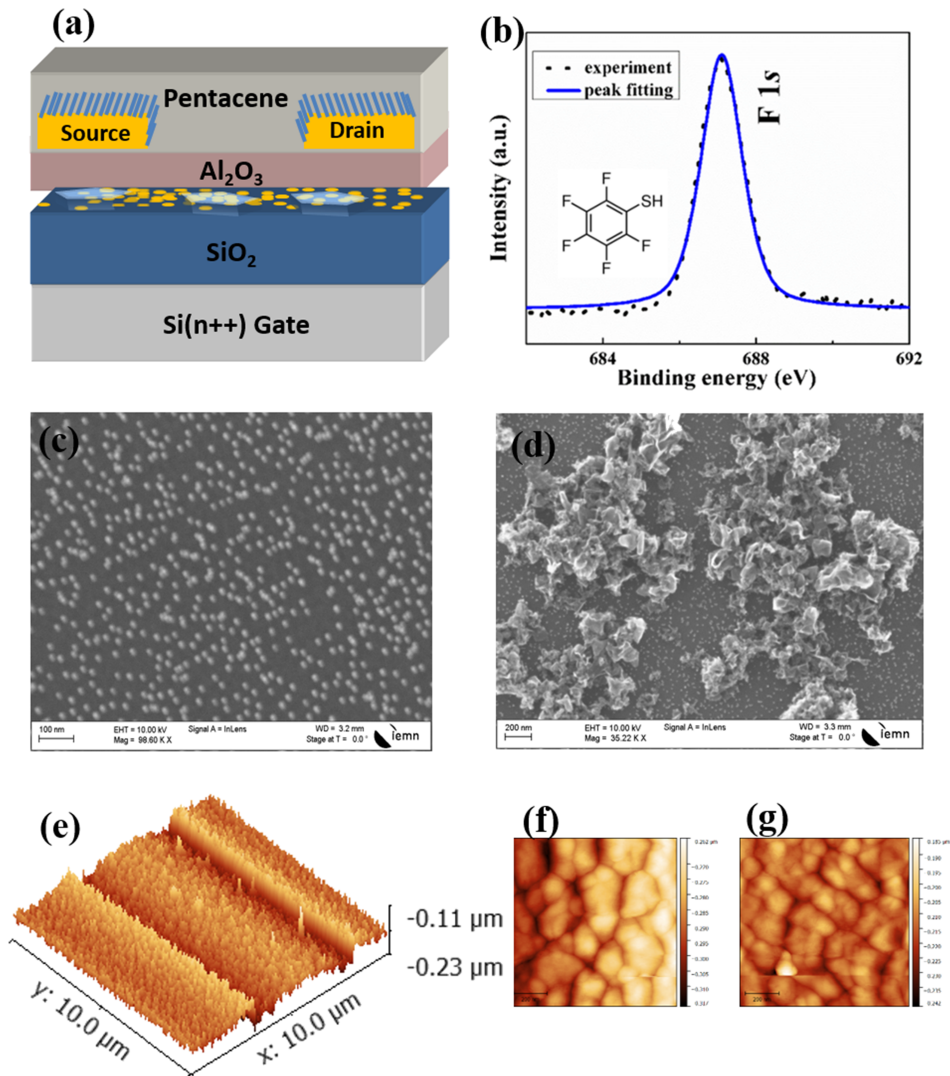


FIG. 1. (a) The configuration of pentacene based double NFGM device with PFBT SAM modification, (b) the high resolution of XPS spectrum with F 1s of PFBT, (c) the SEM image of Au NPs, (d) the SEM image of Au NPs covered with rGO sheets, (e) the 3d AFM morphology of pentacene thin films deposited on PFBT modified electrodes and dielectric. (f) and (g) the zoom of AFM.

films deposited on PFBT modified electrodes. The pentacene shows a root mean square roughness 7.8 nm on electrodes areas and 10.8 nm on SiO₂. The zoom AFM images of pentacene on electrode and SiO₂ are displayed in figure 1(f) and (g), respectively.

To get more information of gate bias operation during the measurement of memory, at beginning, the bias hysteresis under the application of V_{GS} sweeping ranging from ± 30 V to ± 100 V with a fixed V_{DS} value of -40 V for were carried out and showed in figure 2(a). The large bias hysteresis means the large shifts of the V_{th} . We can see that the reversible bias hysteresis is obviously observed with the application of $V_{GS} \geq \pm 70$ V. As a result, a sequential programming and erasing operations performed by applying of $V_{GS} -90$ V and $V_{GS} +90$ V in our following experiments. Figure 2(b) shows the change in the threshold voltage respect to the different program/erase speeds (changes from 10^{-4} s to 10^1 s). Initially, the V_{th1} is -25 V after programming and V_{th2} is -13 V after erasing at a gate bias ± 90 V for 10^{-4} s. The V_{th} shift is increased with the increase of program/erase operation time. The memory window is defined as shift value of V_{th} respect to the applied program/erase bias pulses.⁷ Overall, we found that the memory window increased up to 51 V with the program/erase operation time of 10 s.

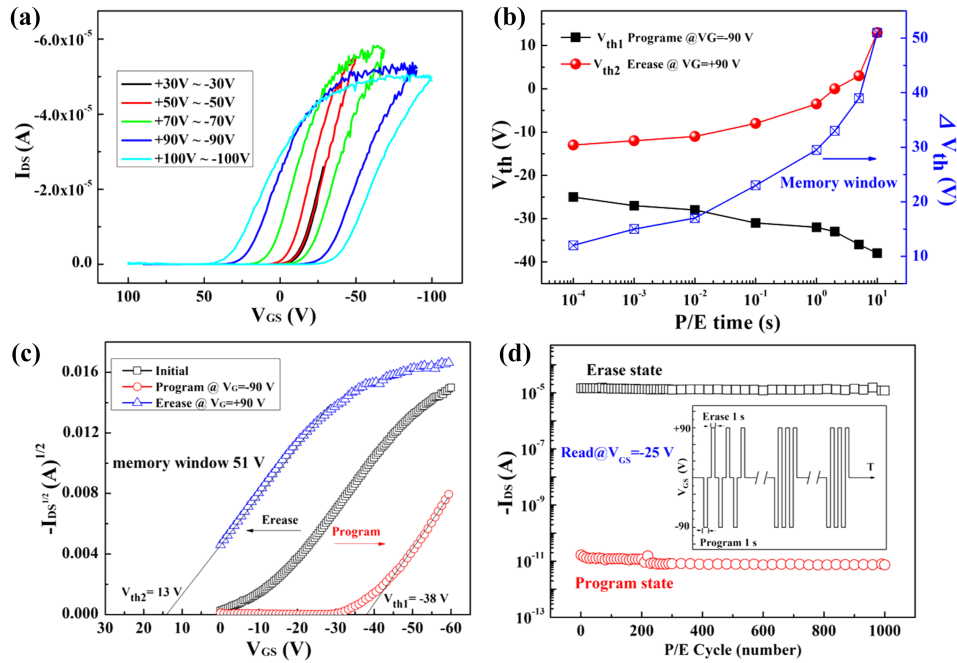


FIG. 2. (a) The bias hysteresis under the application of V_{GS} sweeping ranging from ± 30 V to ± 100 V with a fixed V_{DS} value of -40 V, (b) the change in the threshold voltage (memory window) respect to the different program/erase speeds, (c) the typical memory transfer curves plotted with $(I_{DS})^{1/2}$ versus V_{GS} after gate bias pulses ± 90 V for 10 s, (d) the endurance property of the NFGM with SAM modification.

The typical memory transfer curves plotted with $(I_{DS})^{1/2}$ versus V_{GS} at gate bias pulses ± 90 V for 10 s is displayed in figure 2(c). After obtaining the initial curve (black line) with gate sweep from 0 V to -60 V, a negative voltage -90 V is applied to the gate, thus, holes are ejected from the pentacene channel to the floating layers through the thin tunneling layer, and the holes are preferably first charged in the lower floating gate (Au NPs) according to the Ref. 24. When the Au NPs getting saturated to trap the holes under the constant programming voltage, the extra could be trapped by the upper rGO sheets.²⁵ Therefore, the transfer curve shift to the negative bias (red line), it confirms that the charges are trapped in the floating gate. Then applying $+90$ V to the gate, the holes stored in the Au NPs are rejected back to the channel, resulting in a positive V_{th} shift (blue line). It signify to indicate that the holes stored in the Au NPs would overcome the energy barrier height induced by the difference Fermi levels between rGO and Au NPs first, then transferred back to the channel. In this case, the memory fabricated with rGO and Au NPs double floating gate could perform better retention properties than single floating gate memory.^{3,23,26} Generally, the transfer curve should almost shift back to the same position of initial state after erasing operation. But here a lot of difference (the shift of black line blue line) is found for the device, which means that the charge density is quite different from the initial state. The explanation for this phenomenon would be presented in the later discussion.

The charge endurance and retention capabilities are the important merits for nonvolatile memories. Figure 2(d) shows the endurance property of the NFGM with SAM modification. The I_{DS} character was measured by repeating continuous program/erase (P/E) operations with bias pulse of ± 90 V for 1 s, as shown in inset of figure 2(d). A reading voltage of $V_{GS} -25$ V was applied to verify the distinguishable I_{DS} current state (lies in between program V_{th} and erase V_{th}) for reliability. As a result, we can see almost no degradation and break down were observed until 1000 repeated P/E cycles.

To compare performances of the double NFGM with and without PFBT, figure 3(a) displays the transfer curves of the NFGM without PFBT modification. We can see that the memory window is 37 V, and the erase state is almost transfer back to the initial state after the sequential program to erase operation, indicating that the PFBT SAM affect the performances of the NFGM. Figure 3(b) shows

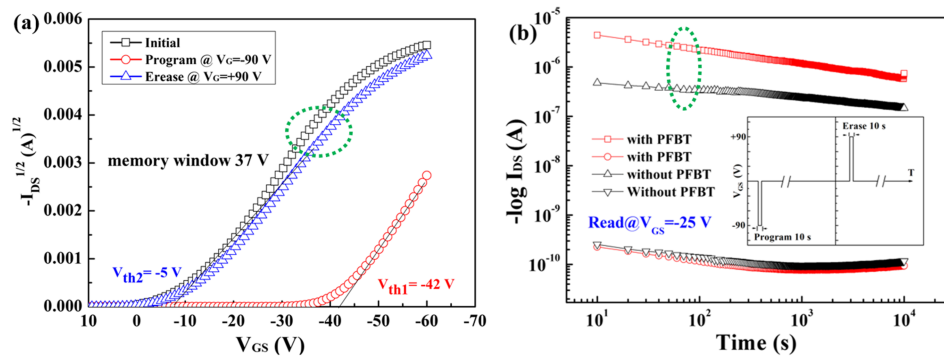


FIG. 3. (a) The transfer curves of the NFGM without PFBT modification, (b) the retention characteristics of the NFGM with and without PFBT. The I_{DS} values were read (at $V_{GS} = -25$ V) over a time interval of 10 s after the application of P/E bias pulse of +90 V/-90 V.

the retention characteristics of the NFGM with and without PFBT. The I_{DS} values were read over a time interval of 10 s after the application of P/E bias pulse, as shown in inset of figure 3(b). The values of the retention of time of NFGM with and without PFBT is determined to be more than 10^8 . The program state is almost on the same stage for the two devices, whereas a distinguishable erase state is found, which means that after the erase operation, the number of charges released from the Au NPs back to the semiconductor is different for the two devices.

The trapped charge density in the NFGM device is estimate using the sample equation $Q = C \Delta V_{th}$ (Where C is the capacitance per unit area and ΔV_{th} is the memory window).^{7,27} For our NFGM devices, C is measured by C-V characteristic with a value of 2.3×10^{-7} F/cm². Consequently, the electrical parameters extracted from different measurements for the two devices are also summarized in table. For better compassion, the values shown in Table I is extracted by 1 device. The average mobility of 12 devices with and without SAM is $0.21 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $0.048 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. The average memory window of 12 devices with and without SAM is 48 V and 33 V, respectively. We can see that the trapped charge density is increased after the PFBT modification and the performances of the memory are improved.

The effects of PFBT on the pentacene and electrodes could be directly analyzed by XPS and UPS. Figure 4(a) shows the respective C1s spectra of PFBT and pentacene deposited on PFBT, the C 1s peak of PFBT/Au shows the C-C bond and C-F bond at 284.8 eV and 286.7 eV, respectively. And the C 1s peak of pentacene/PFBT/Au shows symmetric shape with a peak centered at 284.4 eV. The shift of the C-C peak after pentacene deposition with 0.4 eV implies the electronic interaction between pentacene and the PFBT thiol surface due to the molecule dipoles with different directions and moments within the PFBT thiol.²⁰ In figure 4(b), the UPS results of bare gold the PFBT-modified gold are presented. From the spectra, the work function values of bare gold and PFBT modified gold are calculated with 4.74 eV and 5.25 eV, respectively. It implies the PFBT-modified gold increase the work function of bare gold, and resulting in a reduction of hole injection barrier into pentacene semiconductor, in good agreement with previous reports.^{28,29} Thus, in the NFGM device with PFBT modification, more charges from the electrodes injection are trapped in the Au NPs after the programming operation, resulting in the increase of charges released back to the pentacene during the erase operation.

In addition, to better understanding the effect of PFBT on the performances of NFGM device. The schematic diagrams of physical mechanisms for the charge transport during the P/E operation

TABLE I. Comparison of the electrical parameters for NFGM with/without SAM modification.

PFBT	Carrier mobility ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	Memory Window (V)	Trapped charge density (C)	Subthreshold swing (V/decade)	P/E current ratio
with	0.23	51	1.19×10^{-6}	0.8	$> 10^5$
Without	0.053	37	8.6×10^{-7}	1.2	$> 10^4$

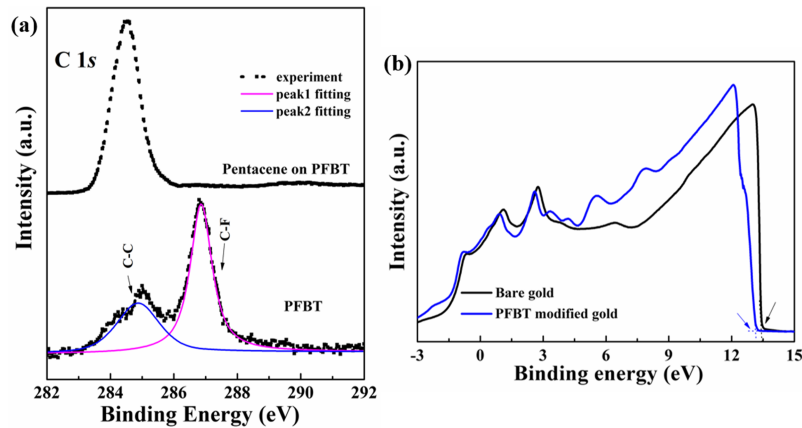


FIG. 4. (a) The respective C1s spectra of PFBT and pentacene on the PFBT, (b) the UPS He I (21.2 eV) spectra under 3 eV results of bare gold the PFBT-modified gold.

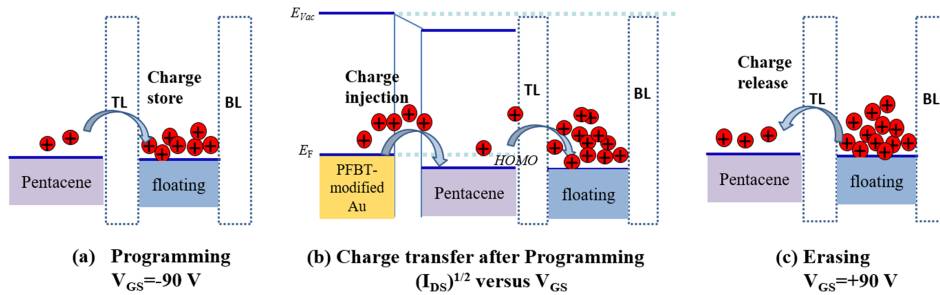


FIG. 5. The schematic diagrams of physical mechanisms for the charge transport during the P/E operation in NFGM with PFBT.

in NFGM with PFBT are depicted in figure 5. When pulses -90 V was operated on gate, the intrinsic charges in pentacene are rejected to the floating gate and be stored. Then, the programming transfer curve is measured with gate sweep from 0 V to -60 V. during this process, because of the PFBT modification, more charges are injected in the semiconductor and even transfer to the floating gate under the gate voltage, inducing more charges trapped in the floating gate, shown in figure 5(b). On the contrary, when the gate bias pulses +90 V was operated, the charges are all released back to the pentacene, shown in figure 5(c), and resulting in the conclusion that charge density in pentacene is quite different from the intrinsic state and increased. It further explains the erase state shifts from the initial state in figure 2(c).

In conclusion, the performances of pentacene based NFGM with and without chemical treating of PFBT SAM are presented and compared. The NFGM with PFBT exhibits excellent memory performances, including high mobility of $0.23 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, the large memory window of 51 V, and the stable retention property more than 10^8 s . The optimized performances of the NFGM are explained by the increase of charge injection, resulting the increase of trapped charge density in Au NPs floating gate. In particular, the results highlight the utility of SAM modulations and controlling of charge transport in the development of transistor memories.

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