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Abstract:

Predictive direct power control (P-DPC) has been suggested as an effective alternative to the conventional direct power control (DPC) applied to PWM converter such as active power filter (APF) and PWM rectifier. It is characterized by a high transient dynamic, which makes it an interesting alternative for conventional direct power control (DPC). Furthermore, in the existence of a non-linear load, the source currents would become highly distorted under perturbed and unbalanced voltage grid conditions. In order to resolve the problems mentioned above, the present paper proposes an improved P-DPC control for APF based on disturbance rejection principle, which is able to operate under balanced, unbalanced and distorted grid voltages conditions and can attain sinusoidal source currents with a respectable total harmonic distortion (THD) meets with IEEE-519 standard. Simulation results and comparative study are presented to confirm the efficiency of the proposed approaches.

Keywords: Disturbance rejection, Shunt Active Power Filter, Predictive Direct Power Control, Total Harmonic Distortion.

Nomenclature

AC: alternative current	$\mathbf{e_{s\ 1,2,3}}$: grid voltages (V)
DC: direct current	$\mathbf{Is}_{\ 1,2,3}$: grid currents (A)
PI: proportional-integral controller	$\mathbf{I}_{\alpha\beta}$: grid currents in αβ reference frame (A)
Kp Proportional gain	$\mathbf{e}_{\alpha\beta}$: grid voltages in αβ reference frame (V)
Ki Integral gain	$\mathbf{V}_{a,b,c}$: inverter output voltages (V)
Ts simple time	$\mathbf{V_{dc}}$, $\mathbf{V_{dc\ ref}}$: actual and reference DC bus voltage (V)
DB: diode bridge	$\mathbf{P}_{ref}$: Reference active power (W)
APF: active power filtering	$\mathbf{Q}_{ref\ :}$ Reference reactive power (Var)
DTC: direct torque control	$\mathbf{L}_{S1,2,3}$: source inductance (H)
DPC: direct power control	$\mathbf{R}_{S1,2,3}$: source resistance (Ω)
P-DPC: predictive direct power control	$\mathbf{L}_{f1,2,3}$: Output filter inductance (H)
THD: total harmonic distortion coefficient	$\mathbf{L}_{C1,2,3}$: Input DB inductance (H)
PLL: phase locked loop	$\mathbf{L}_{L}$: load inductance (H)
C: DC bus capacitor	$\mathbf{R}_{L}$: load resistance (Ω)
ξ : damping coefficient	**Sa,Sb,Sc :** switching state
$\boldsymbol{\omega_n}$: natural frequency	**ε:** error
θ: angle phase	**F**: cost function

1. Introduction

The use of non-linear loads, such as switching power supply, rectifiers with diodes or thyristors, etc., causes an enormous quantity of current harmonics to be injected into the distribution grids [1]. These harmonics cause distortions in the current form of the source, which leads to additional losses in line capacitances and transformers, and dysfunctions of sensitive electronic equipment [2], [3]. As a solution, the parallel active power filter (APF) is recognized as a flexible solution for harmonic compensation. It is connected in parallel with the grid, and injects to the grid currents equal to those generated by the non-linear loads, but in opposite phases [3]. Active power filter (APF) performance is dependent on its control strategy. Several controls have been proposed in the literature, among control methods existed, such as current hysteresis control [5], [6], [7], voltage oriented control [8] and direct power control [9]. In recent years, researchers are more attentive in direct power control (DPC) strategy in various applications due to its noticeable skills: no internal current loops, good dynamics and performances [9], [10]. This method coming from the famous direct torque control (DTC) [11] is applied in electrical machine control. Nevertheless, this classic DPC has a major drawback, related to the uncontrolled switching control signals periodicity. To remedy this problem, authors suggest associating the DPC principle with space vector modulation (DPC-SVM) [11], or with predictive approaches (P-DPC) [4], [12], [13], [14], [15]. All the control strategies that have been mentioned do not perform sinusoidal current when the line voltage is distorted or unbalanced. Nowadays, only few papers have addressed the subject of control under unbalanced or distorted grid voltage conditions [16], [17], [18], [19]. This paper suggests a new P-DPC configuration that aims to attain sinusoidal source currents operation of shunt active power filter (SAPF) under different source voltage conditions. This control strategy is based on the principle of disturbance rejection to eliminate the effect of any unbalanced or distorted grid voltages. The proposed P-DPC strategy was compared with the conventional P-DPC in simulation studies proposed in [9], [10]. The results approve the efficiency and the high performance of the proposed

DPC controller compared to the conventional one. The rest of the paper is organized as follows: in section 2, the description of the system is given, while in section 3, all proposed control techniques are detailed. To test the efficiency of these approaches, section 4 shows and comments the attained results. Finally, section 5 concludes this study.

2. Modeling System

The proposed system is made up of three main blocks: the first is the three-phase grid. The second is the active power filter APF controlled by P-DPC based on disturbance rejection principle. Finally, DC bus controller, the PI regulator is used to control DC bus voltage and generate the active power reference for the power control strategy as show in figure 1.

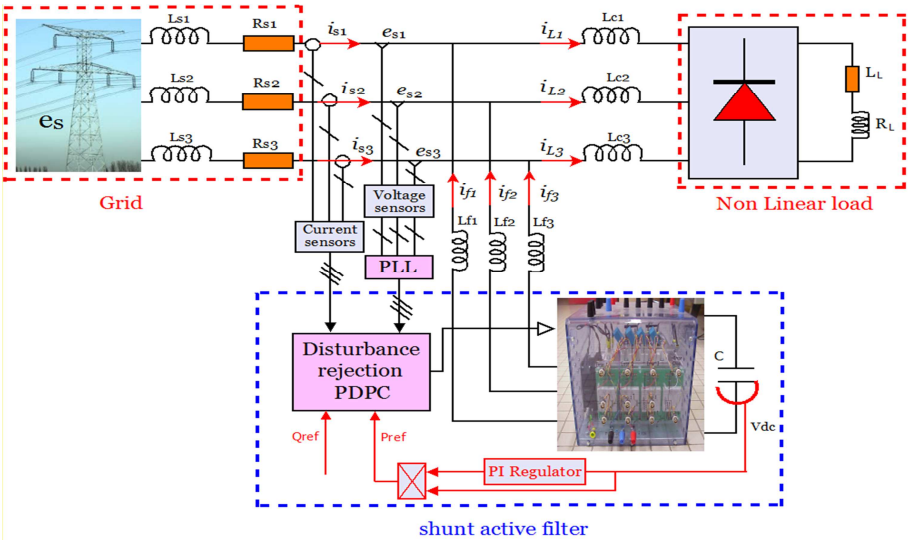
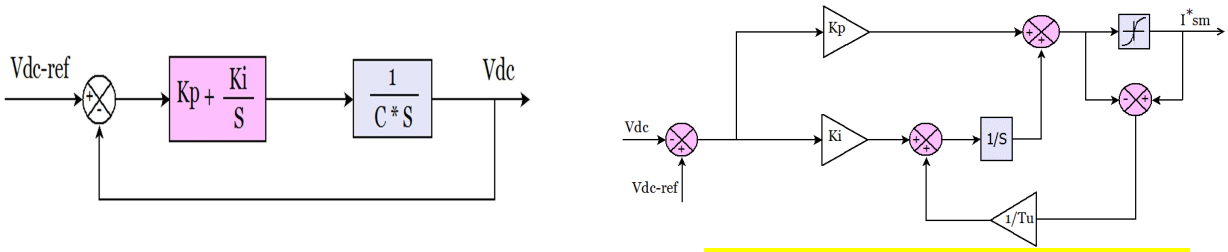


Figure 1: Synoptic description of the studied system

3. Control approaches

3.1. DC bus regulator

In order to minimize the voltage fluctuations and ensure the best operation of P-DPC, it is appropriate to maintain the DC bus voltage to a well-determined value. A PI controller with an anti-windup compensation is proposed to adjust the DC bus voltage [10], [20] and also to estimate the maximum current Imax, which is used to calculate the reference power [21]. Its general structure is illustrated in Figure 2 below:



(a) Simplified scheme (b) PI scheme with an anti-windup return

Figure 2: Schemes for regulating the DC bus voltage by a PI controller

From the simplified scheme of figure 2.a, the transfer function of the closed loop system can be written:

$$\frac{V_{dc}(s)}{V_{dc-ref}(s)} = \frac{K_p.s+K_i}{C.s^2+K_p.s+K_i} = \frac{K_p/C.(s+K_i/K_p)}{s^2+K_p/C.s+K_i/C} \quad (1)$$

From equation (1), the relation between V_{dc} and V_{dc-ref} is a second order transfer function:

$$\frac{V_{dc}(s)}{V_{dc-ref}(s)} = \frac{2.\xi.\omega_n.s+\omega_n^2}{s^2+2.\xi.\omega_n.s+\omega_n} \quad (2)$$

After matching between the two relations (1) and (2), we get:

$$K_p = 2.\xi.\omega_n.C \quad (3)$$

$$K_i = C.\omega_n^2 \quad (4)$$

Where ω_n is the natural frequency and ξ is the damping coefficient. For ξ = 0.0707, K_p and K_i can be determinate.

3.2. Phase-locked loop

PLL is one of the circuits frequently used in electronic power control, as in active power filters. Its main role in electronic applications; is to identify the frequency or angular position of a periodic signal, for generating another signal synchronized with the last [22]. However, many power applications require a phase of an ideal sinusoidal signal locked to the operating voltages. Since the public service voltages are not always sinusoidal and balanced, PLL is used to extract the fundamental component. The basic form of the PLL containing a phase detector PD (coordinate transformation), a corrector (loop filter LF) and a voltage controlled oscillator VCO (integrator) as show in figure 3 [23].

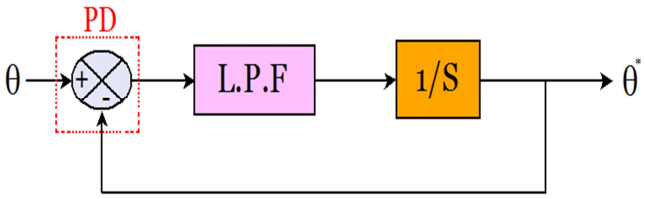


Figure 3: basic structure of a three-phase PLL

In figure 4, a robust solution based on a multi-variable filter (MVF), which is the most important part of this PLL is proposed. This filter is developed by Hong-seok Song [24]. Thereby making it insensitive to disturbances, and to properly filtering the currents in the α-β axis, which provides very good results in distorted voltage. The structural form MVF filter is given by figure 5:

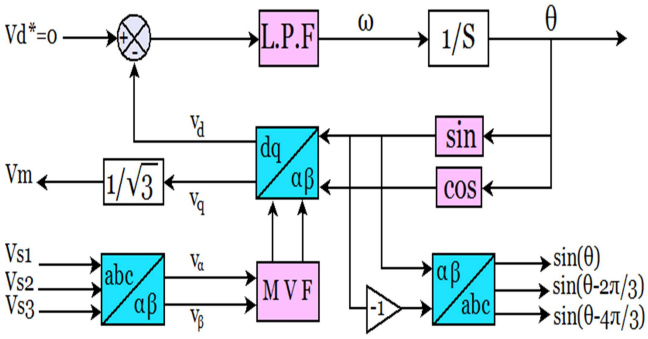


Figure 4: Diagram structure of the PLL with MVF

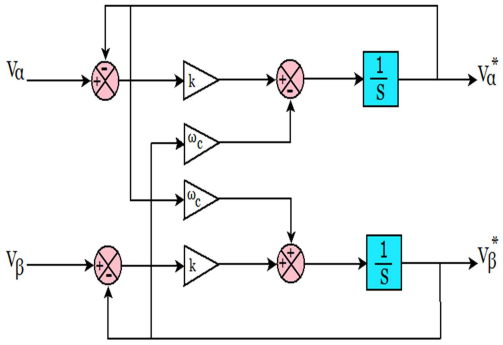


Figure 5 : Circuit diagram of MVF

The transfer function of MVF filter expressed by the following expression:

$$H(s)=\frac{v^{*}_{\alpha\beta}(s)}{v_{\alpha\beta}(s)}=k\frac{(s+k)+j\omega_c}{(s+k)^2+\omega_c^{\,2}} \tag{5}$$

From the previous expression (5) and according to α-β axes, expressions binding components $v^{*}_{\alpha\beta}$ output MVF to the input components $v_{\alpha\beta}$ are the following:

$$\begin{cases} v^{*}_{\alpha}=\dfrac{k}{s}\left[v_{\alpha}(s)-v^{*}_{\alpha}(s)\right]-\dfrac{\omega_c}{s}v^{*}_{\beta}(s) \\ v^{*}_{\beta}=\dfrac{k}{s}\left[v_{\beta}(s)-v^{*}_{\beta}(s)\right]-\dfrac{\omega_c}{s}v^{*}_{\alpha}(s) \end{cases} \tag{6}$$

where:

$v_{\alpha\beta}$: The input voltage along the α-β axes.

$v^*_{\alpha\beta}$: The component of the voltage through the filter MVF.

K: dynamic constant determined by the Bode diagram and ω_c the cut-off frequency

To check the strength of the proposed PLL, a simple test is achieved; it is based on the visualization of the voltage source signals at the input and output of PLL as viewing in figure 6.

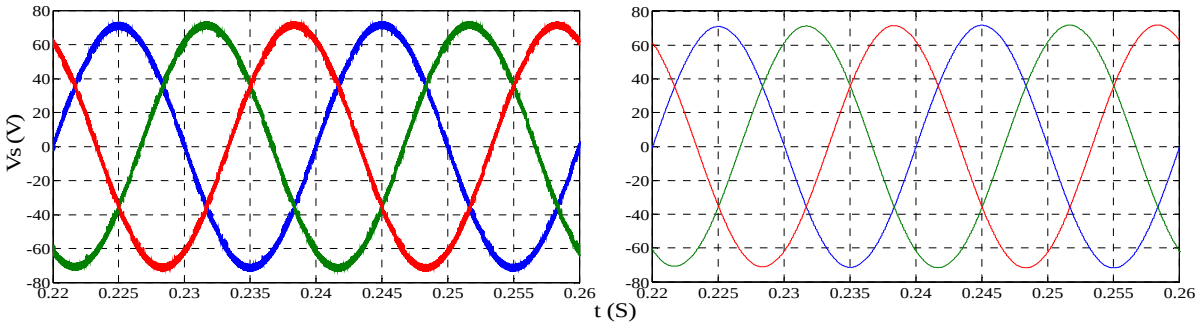


Figure 6: Simulation result of voltage source in the input (a) and the output(b) of PLL

by comparing the signals at the input and the output of the PLL, one can see that, the output signals are smooth and purely sinusoidal, however, the input signals are polluted and disturbed. Therefore, this result demonstrated that the proposed PLL deliver quality signals in the case of distorted source voltage. Therefore, this PLL structure with MVF permits filtering the stationary reference frame components of the main voltages at the network frequency (50 Hz), without introducing neither a phase shift nor a voltage change amplitude.

3.3. Predictive direct power control strategy

Predictive direct control power P-DPC is proposed to improve the direct control power DPC, this strategy was presented in [25] to control the three-phase rectifier with two levels and three levels. The main idea is to minimize a cost function; this function is based on the sum of quadratic differences of active and reactive power and their predicted values. In order to develop predictive direct control algorithm P-DPC, it is necessary first to establish a predictive model of the three-phase voltage inverter controlled using active and reactive instantaneous power. The figure 7 shows the

synoptic of the P-DPC strategy, where the approach which leads to this aim is explained in the following steps [26]:

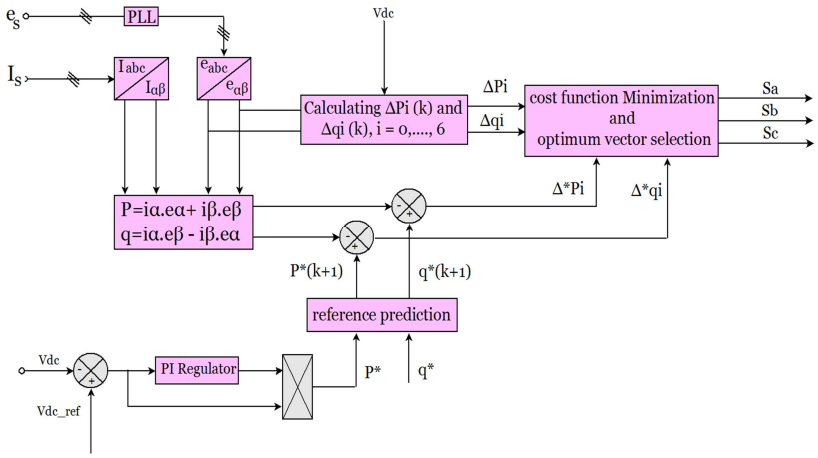


Figure 7: Synoptic of the P-DPC strategy

If assuming that the sampling period Ts is sufficiently small relative to the period of the mains voltage (Ts << T), network components of the voltage vector, $e_{\alpha\beta}$ can be regarded as constant during the sampling period. This assumption gives:

$$e_{\alpha\beta}(k) = e_{\alpha\beta}(k+1) \tag{7}$$

The variations in active and reactive power between two consecutive sampling instants are given by the following formula:

$$\begin{bmatrix} P(k+1) - P(k) \\ Q(k+1) - Q(k) \end{bmatrix} = \begin{bmatrix} e_{\alpha}(k) & e_{\alpha}(k) \\ e_{\beta}(k) & -e_{\beta}(k) \end{bmatrix} \cdot \begin{bmatrix} i_{\alpha}(k+1) & -i_{\alpha}(k) \\ i_{\beta}(k+1) & -i_{\beta}(k) \end{bmatrix} \tag{8}$$

Furthermore, the evolution of the current vector absorbed by the voltage inverter is governed by the differential equation of the first order:

$$L_f \frac{d}{dt} \begin{bmatrix} i_{\alpha}(t) \\ i_{\beta}(t) \end{bmatrix} = \begin{bmatrix} e_{\alpha}(t) \\ e_{\beta}(t) \end{bmatrix} - \begin{bmatrix} v_{\alpha}(t) \\ v_{\beta}(t) \end{bmatrix} - r_f \cdot \begin{bmatrix} i_{\alpha}(t) \\ i_{\beta}(t) \end{bmatrix} \tag{9}$$

By neglecting the effect of the series resistance of the coupling inductance r_f, the equation (9) becomes as the following form:

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{L_f}\left(\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} - \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}\right) \tag{10}$$

By using a discretization of the first order of equation (10) over a sampling period Ts, then we obtain the variation of the vector of currents between the two successive sampling instants "k" and "(k + 1) ", which is expressed by the equation below:

$$\begin{bmatrix} i_\alpha(k+1) - i_\alpha(k) \\ i_\beta(k+1) - i_\beta(k) \end{bmatrix} = \frac{T_S}{L_f}\left(\begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} - \begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix}\right) \tag{11}$$

By substituting the expression of the equation (11) into (8) we obtain the predictive model of the voltage inverter, based on the instantaneous active and reactive powers, below:

$$\begin{bmatrix} P(k+1) \\ Q(k+1) \end{bmatrix} = \begin{bmatrix} P(k) \\ Q(k) \end{bmatrix} + \frac{T_S}{L_f}\begin{bmatrix} e_\alpha(k) & e_\alpha(k) \\ e_\beta(k) & -e_\beta(k) \end{bmatrix} \cdot \begin{bmatrix} e_\alpha(k) - v_\alpha(k) \\ e_\beta(k) - v_\beta(k) \end{bmatrix} \tag{12}$$

From the equation (12), it is notable that the coupling inductance Lf, and the sampling period Ts are the only parameters involved in this predictive model system.

Ideally, the convergence of controlled active and reactive powers to their instructions is reached if the following condition is verified:

$$\begin{aligned} P^*(k+1) - P(k+1) &= 0 \\ Q^*(k+1) - Q(k+1) &= 0 \end{aligned} \tag{13}$$

The condition in equation (13) cannot be satisfied until changes in active and reactive power during the switching period, take the following values:

$$\begin{aligned} \Delta P^*(k) &= P^*(k+1) - P(k) \\ \Delta Q^*(k) &= Q^*(k+1) - Q(k) \end{aligned} \tag{14}$$

The errors $\varepsilon_P(k)$ *and* $\varepsilon_Q(k)$ are defined as follows:

$$\begin{aligned} \varepsilon_P(k) &= \Delta P^*(k) - \Delta P_i \\ \varepsilon_Q(k) &= \Delta Q^*(k) - \Delta Q_i \end{aligned} \quad i = 0, 1, \ldots\ldots, 6 \tag{15}$$

Where ΔP_i and ΔQ_i are the points of variation of the instantaneous powers active and reactive distribute on the four quadrants of the plane (ΔP, ΔQ).

The cost function is defined as follows:

$$F = \varepsilon_P(k)^2 + \varepsilon_Q(k)^2 \quad (16)$$

The P-DPC requires the prediction of the references of the active and reactive instantaneous powers with a step in advance, P * (k + 1) and Q * (k + 1). The reference active power is calculated from the output of the DC bus voltage regulator Vdc; against the reference of the reactive power is set to zero to ensure a unit power factor. For this, the prediction of the references of the active and reactive powers are given by the following relation:

$$\begin{aligned} P^*(k+1) &= 2.P^*(k) - P^*(k-1) \\ Q^*(k+1) &= Q^*(k) \end{aligned} \quad (17)$$

The principle of prediction of active power is shown in the figure 8 below. The tracking error of DC bus voltage is assumed constant over two successive sampling periods, so the active power command at the next sampling instant (k+1) can be estimated using a linear extrapolation.

Figure 8: Principle of prediction of the active powers reference

3.4. P-DPC control based on disturbance rejection

In reference frame, active and reactive power amounts exchanged with the grid are given by:

$$\begin{aligned} p_h &= e_\alpha i_{\alpha_h} + e_\beta i_{\beta_h} \\ Q_h &= e_\beta i_{\alpha_h} - e_\alpha i_{\beta_h} \end{aligned} \quad (18)$$

From the principle diagram in Figure 9 we have:

$$\begin{bmatrix} i_{s1_h} \\ i_{s2_h} \\ i_{s3_h} \end{bmatrix} = \begin{bmatrix} i_{s1} \\ i_{s2} \\ i_{s3} \end{bmatrix} - \begin{bmatrix} i_{s1}^{*} \\ i_{s2}^{*} \\ i_{s3}^{*} \end{bmatrix} \quad (19)$$

In the proposed P-DPC control, the amplitude of the currents input I_{max} is provided from the output of PI controller of Dc-bus voltage, as shown in Fig. 2. Therefore, the fundamental of these currents are is generated by using a robust PLL as shown in fig. 9:

$$\begin{bmatrix} i_{s1}^{*} \\ i_{s2}^{*} \\ i_{s3}^{*} \end{bmatrix} = \begin{bmatrix} \mathrm{I}_{\max} \sin(\omega t) \\ \mathrm{I}_{\max} \sin(\omega t - 2\pi/3) \\ \mathrm{I}_{\max} \sin(\omega t - 4\pi/3) \end{bmatrix} \quad (20)$$

After submission (20) in (19), we have:

$$\begin{bmatrix} i_{s1_h} \\ i_{s2_h} \\ i_{s3_h} \end{bmatrix} = \begin{bmatrix} i_{s1} \\ i_{s2} \\ i_{s3} \end{bmatrix} - \begin{bmatrix} \mathrm{I}_{\max} \sin(\omega t) \\ \mathrm{I}_{\max} \sin(\omega t - 2\pi/3) \\ \mathrm{I}_{\max} \sin(\omega t - 4\pi/3) \end{bmatrix} \quad (21)$$

Since *Ph** and *Qh** are fixed to zero, tracking errors of controlled powers at sample instant *k* are given by:

$$\begin{cases} \Delta_{P_h}(k) = -P_h(k) \\ \Delta_{Q_h}(k) = -Q_h(k) \end{cases} \quad (22)$$

At the next control period, the predicted tracking power errors values $\Delta_{P_h}(k+1)$ et $\Delta_{Q_h}(k+1)$ are computed as follows with i = 0, 1,…,6 :

$$\begin{cases} \Delta_{P_h}(k+1) = \Delta_{P_h}(k) - \Delta P_i(k) \\ \Delta_{Q_h}(k+1) = \Delta_{Q_h}(k) - \Delta Q_i(k) \end{cases} \quad (23)$$

The predictive model of the voltage inverter, based on the instantaneous active and reactive power below:

$$\begin{bmatrix} P_h(k+1) \\ Q_h(k+1) \end{bmatrix} = \begin{bmatrix} P_h(k) \\ Q_h(k) \end{bmatrix} + \frac{T_S}{L_f} \cdot \begin{bmatrix} e_\alpha(k) & e_\beta(k) \\ e_\beta(k) & -e_\alpha(k) \end{bmatrix} \cdot \begin{bmatrix} e_\alpha(k) - v_\alpha(k) \\ e_\beta(k) - v_\beta(k) \end{bmatrix} \quad (24)$$

The optimum voltage vector, applied in the next control period, is given by minimizing the cost function:

$$F = \Delta_{P_h}(k+1)^2 + \Delta_{Q_h}(k+1)^2 \quad (25)$$

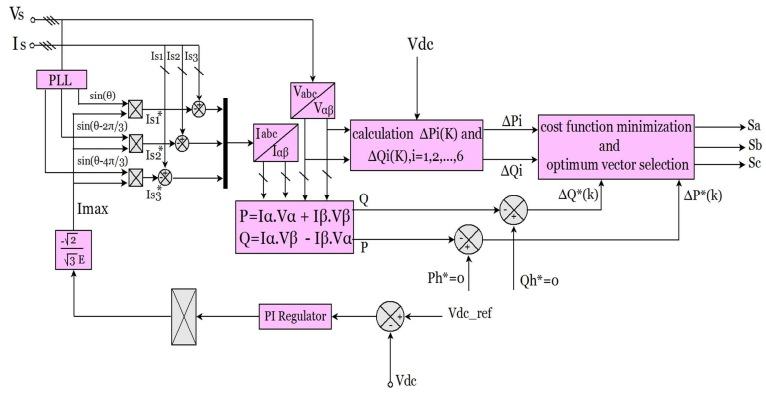


Figure 9: Synoptic of P-DPC based on disturbance rejection

4. Simulation results

Several simulations were carried out to evaluate the proposed control methods. The simulation models were developed in Matlab\Simulink®. Table I presents the electrical parameters of modeled power circuit.

Parameters	Values
Sampling period	1.10^{-6} s
Source voltage Vs	53 V rms
Source resistance Rs	0.33 Ω,
Source inductance Ls	1.32 mH
Load resistance R_{L1} R_{L2}	12 Ω, 24 Ω
Load inductance L_L	0.56 mH
Input DB inductance Lc	1 mH
Output filter inductance Lf	3 mH
DC-bus Capacitor C,	1100 µF
DC bus voltage reference Vdc	173 V

Table I: Simulation parameters

4.1. Balanced grid voltages

Figures 10-13, illustration the simulation results of the SAPF for the both conventional P-DPC and the proposed P-DPC scheme under balanced grid voltage conditions (Figure 10). Besides, both control strategies achieve a purely sinusoidal source current with a good THDi, with a slight superiority for the proposed P-DPC strategy (Figure 11). Obviously, we can say that both control strategies, conventional P-DPC and proposed full rejection P- DPC can track there references of active and reactive power. Whereas, the proposed P-DPC keeps both tracking errors of controlled

powers close to zero (Figure 13), the conventional P-DPC keeps the active power at Pref = 1160 W and the reactive power near zero (Figure 12).

- Conventionnel P-DPC
- Proposed P-DPC

a b

Figure 10: Phase source current THDi under balanced grid voltage

a b

Figure 11: Voltage and current source under balanced grid voltage

Figure 12: Active and reactive power under balanced grid voltage

Figure 13: Tracking errors of controlled active and reactive power

4.2. Unbalanced grid Voltages

To test the robustness of the proposed control, a first test based on unbalanced grid voltages is performed. In this case, the amplitudes of the network voltage were changed as follows:

$Vs_1 = 75$ V, $Vs_2 = 90$ V, $Vs_3 = 60$ V.

179

180

- Conventionnel P-DPC
- Proposed P-DPC

a b

Figure 14: Voltage and current source under unbalanced grid voltages

a b

Figure 15: Phase source current THDi under unbalanced grid voltage

Figure 16: Active and reactive power under unbalanced grid voltages

Figure 17: Tracking errors of controlled active and reactive power

181 The simulation results represented in Figures 14-17 corroborate that the proposed P-DPC can handle
182 the unbalance of voltage source phases. Sinusoidal source current is achieved (Figure 14-b) with a
183 good THDi = 0.62% (Fig. 15-b), which is better than the conventional P-DPC that cannot handle this
184 unbalance voltage. The current is disturbed (Figure 14-a) with THDi = 11.99% due to the presence of

185 the 3rd harmonic (Figure 15-a). The power ripple (Figure 16) is more important compared to the
186 proposed P-DPC (Figure 17), where active and reactive powers are close to their references which
187 guarantees the full rejection of grid voltage disturbance.

188 **4.3. Distorted Grid Voltages**

189 A 2nd test, based on the distortion of the grid voltage is performed to test the robustness of the
190 proposed P-DPC control. In this case, fifth harmonic voltage is superposed on grid voltages.

- Conventionnel P-DPC
- Proposed P-DPC

a b

Figure 18: Voltage and current source under distorted grid voltages

a b

Figure 19: Source current THD under distorted grid voltages

Figure 20: Active and reactive power under distorted grid voltages

Figure 21: Tracking errors of controlled active and reactive power

This test results shown in Figures 18-21, also confirms the robustness of the proposed P-DPC control, which is able to give a purely-sinusoidal current source (Fig.18-b) under disturbed condition with a good THDi = 1.20% (Fig. 19-b), unlike the conventional P-DPC which cannot keep up with this distortion incident (Fig. 18-a) with a degraded THD = 20.36% because of the presence of the 7^{th} harmonic (Figure 19-a). The power ripple (Figure 20) is also more important compared to the proposed P-DPC (Figure 21), where active and reactive powers are close to their references which guarantees the full rejection of grid voltage disturbance as mentioned in the previous section.

To recapitulate the results, the following table presents a comparison analysis based on source current THDi between both strategy controls studied in this paper:

Voltage Conditions / Control	balanced	Unbalanced	Distorted
Conventional P-DPC (THDi)	0.63%	11.99%	20.36%
Proposed P-DPC (THDi)	0.59%	0.62%	1.20%

Table I: Comparative analysis

According to this table, it is clear that the proposed P-DPC based on rejected perturbation principle yields better results than the conventional P-DPC under balanced or distorted grid voltage condition, which confirms the robustness of this control strategy.

Conclusion

In this paper, a simulation comparative study between a conventional P-DPC and a proposed P-DPC based on rejected perturbation principle is presented. For this purpose, active and reactive powers provided by harmonic component are chosen as controlled variables. Both power commands, Ph* and Qh* respectively, are given from the outside of the controller and are set to zero to achieve full rejection of any grid disturbance. The simulation results show that the proposed control is able to handle all of balanced, unbalanced and distorted voltage conditions incident in grid and give a purely sinusoidal source current with a good THDi that meets standards IEEE-519, contrary to what is found with the conventional P-DPC under the same voltage conditions. Also, the validity and

efficiency of the proposed methodology have been proved through exposed results. Thus, future work can include a study of the influence of sample period and parametric errors on energy quality into the network system.

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