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A Design of Solid State Power Controller for a bidirectional DC-DC Converter in an aeronautic context

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Keywords

« Energy Storage System », « Solid State Power Controller (SSPC) », « Bidirectional converter (BDC) », « Silicon MOSFET ».

Abstract

This paper deals with the design of a solid state power controller (SSPC) for a DC-DC converter in an aeronautic application. First, the specifications are drawn appropriately with the aeronautic environment. Then the design and experimental validation are described.

Introduction

The protection against the reversibility of the supply polarity, inrush current or short-circuit become inevitable in high power application. Moreover in an aeronautic application, the power density is one of the most important priorities [1]–[3]. The electromechanical circuit breakers that have historically been used for aeronautic application have to be challenged regarding the mass and volume [1].

Instead, power transistors can be connected back-to-back as shown in Fig. 1 either in common source or drain to completely isolate the power source from the load, or from another power source. This solution based on semiconductor devices is called Solid State Power Controller (SSPC). In addition, the SSPC requires a minimum maintenance and provides fast interruption of the current thanks to the fast commutation of MOSFETs (a few microseconds) [4].

This protection have been integrated in the SUNSET equipment detailed in [5]. The SUNSET equipment targets energy recovery from the final breaking of an aircraft into a battery pack through the aircraft high-voltage network. The battery management system (BMS) monitors permanently the voltage, temperature and current of the battery pack. Depending on data collect, the BMS turns on (safe mode) or cuts off (security mode) the SSPC.

This paper deals with the design of a SSPC board that will be implemented between a DC-DC converter and a battery pack (350 V). A parallel array of 4 Si-MOSFETs has been used to supply 35 A nominal current and 350A as short-circuit current. Results analysing on-state losses, thermal performance, inrush current limiting, inductive load breaking, and over-current response times will be discussed.

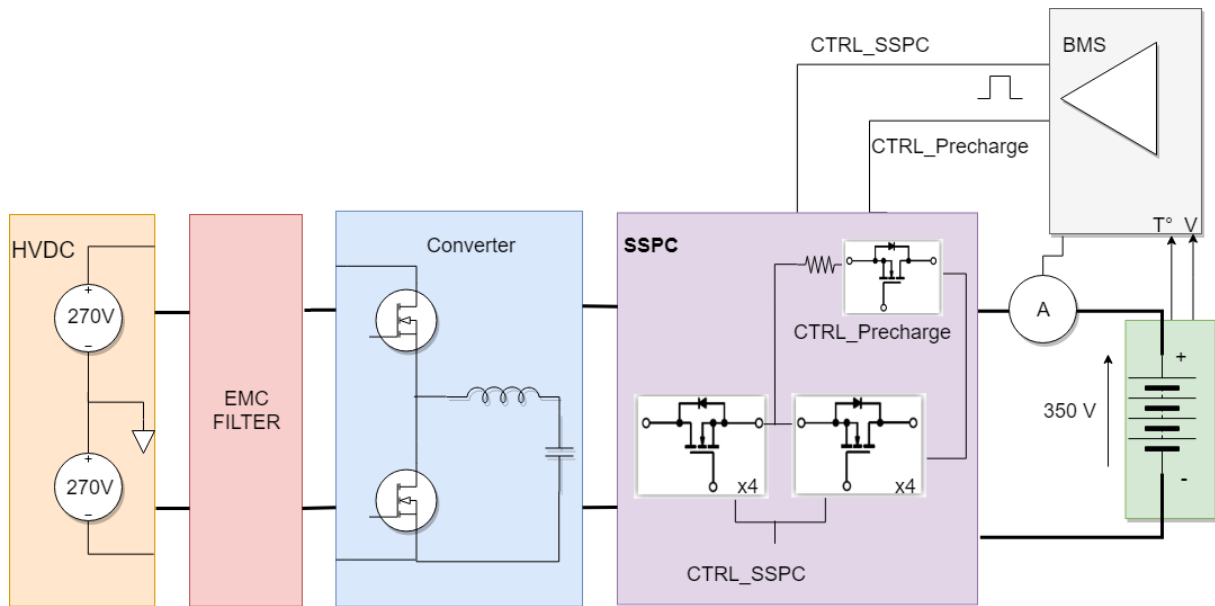


Fig. 1: Synopsis of the SSPC environment

SSPC specifications

This section describes the main environment characteristics to draw the mandatory specifications of the SSPC. The voltage level of the battery is around 350 V with a nominal current of 35 A. Hence the breakdown voltage (V_{BR}) of the SSPC transistors must be larger. Therefore, the V_{BR} taking into account a safety margin (0.7), will be at least 500 V. Regarding the heat sink, the thermal study has defined 20 W as the maximum dissipation for each array of transistors. It is worth to be noted that the switching losses appear only one time at the beginning and the end of charging thus they are negligible relatively to conduction losses. Table 1 summarizes the main specifications to be met in the design.

Table I: The specifications of the SSPC

Hypothesis	ESR Battery	1 Ω (minimal)
	Inductance: cables + connections	1 μH
	Output capacitor	3.3 μF
SSPC Constraints	DC Voltage	500 V
	Nominal Current (I_n)	35 A
	Maximum allowed Current	40 A
	Maximum absolute current	350 A
	Instantaneous cut-off	$I > 5 I_n$
	I^2t Protection	$1.15 I_n < I < 5 I_n$
	Power losses	20 W

SOA curves

The most important characteristic of an SSPC is its capability of dissipating energy during opening. The current limit during the switching time is given by datasheet in Safe Operation Area (SOA). Several datasheets of 650 V MOSFET have been compared. The best candidates show the ability of conducting 200 A under 650 V for 1 μs . In our application, the short-circuit current (350 A) has been calculated based on the assumption of 1 Ohm as internal impedance of the battery pack (350 V). The batteries as well as the SSPC must be able to carry this current until the default is eliminated. Thus, at least two parallel transistors are needed.

The circuit loop in the case of SSPC opening is equivalent to an inductive circuit whose current rise depends on the values of $\tau = L / R$. The inductance of connection and cables is estimated to $1 \mu\text{H}$ which means $\tau = 1 \mu\text{s}$ with the latter impedance assumption. Thus, the steady state current will reach 350 A in only 5 μs . Therefore, in a real case the fault must be eliminated in 10 μs maximum. So, all the transistors connected in parallel must stand 350 A for 10 μs at reduced V_{DS} (ohmic region). This leads us to compare the maximum current per MOSFET to deduce the number of devices to be connected in parallel. However, the most dimensioning parameter is the power dissipated during the switching ON-OFF because of the dynamic voltages and currents that MOSFETs must handle during the switching. Thus, the energy to be dissipated during the turn-off of the MOSFET is equivalent to the product of the power dissipated by the switching time (1 μs). The following equation calculates roughly the maximum energy by getting the maximum current and voltage divided by $\sqrt{3}$ to compensate the decrease in current during the switching.

$$E = U * I * t = (670\text{V} * 350\text{A} / \sqrt{3}) * 1\mu\text{s} = 123\text{mJ}.$$

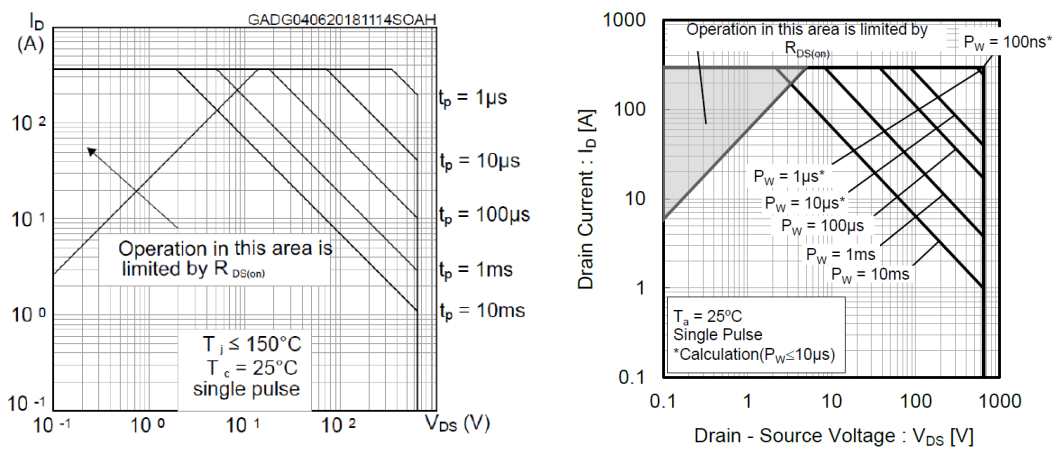


Fig. 2: Safe operation Area (SOA) for SPTH90N65G2V device (left) and SCT3017AL device (right)

Choice of the MOSFET

As mentioned, several 650 V MOSFET have been compared. Figure 3 shows the continuous power losses due only to $R_{\text{DS-on}}$. It shows the decrease in power losses as function of the number of parallel MOSFETs. Even if STW77N65M5 exhibits the highest conduction losses, it is still within the specifications if '4' MOSFETs are in parallel. Therefore, the choice of 4 MOSFETs (STW77N65M5) seems to make a good trade-off by minimizing the cost / mass / losses while guaranteeing robustness in case of opening the circuit in short-circuit.

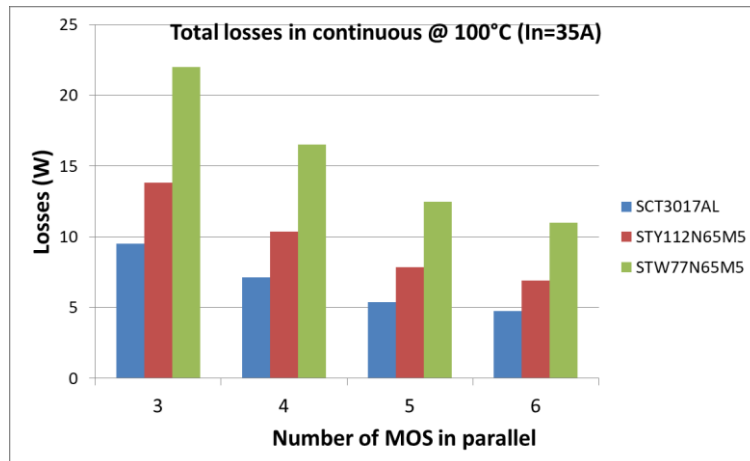


Fig. 3 Power losses during conduction mode for several MOSFETs

PCB design

As mentioned before, the SSPC board is inserted between the converter and the battery pack. So, it has a particular form (like a T) imposed by the space environment (see Figure 4).

Layout PCB

For EMI issues, the ground potential is linked to some layers of the PCB. This reduces the loop of the current return. In order to limit the current density at 15 A/mm² in the copper track, two layers have been used for the return current and for the drain connection. As a result, six layers have been used in total.

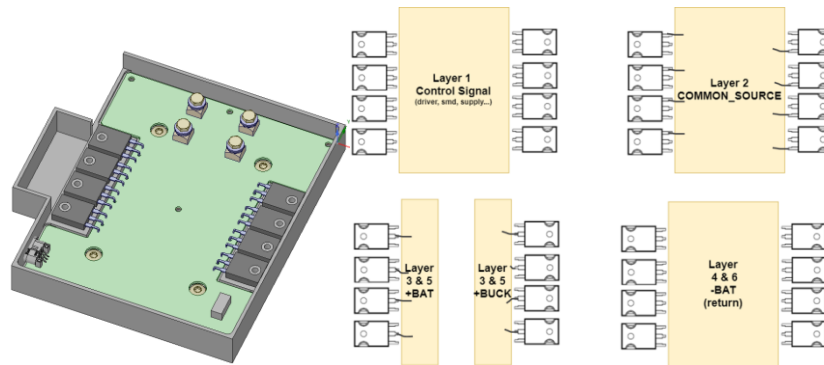


Fig. 4 3D modeling and layer decomposition of the SSPC board

Overvoltage protection

The SSPC MOSFETs should interrupt current in case of a short circuit or overcurrent. While opening an inductive circuit, an overvoltage is unavoidable ($L di/dt$). In order to prevent breakdown and false turn-on, two solutions have been implemented as shown in Figure 5: Active Clamping and Advanced Active Clamping [6]. These solutions can work both or separately. However, this paper discusses only the first one.

Active clamping is a technique that keeps a transient overvoltage below the critical limits when the MOSFET turns off. TVS voltage should be higher than nominal voltage and lower than breakdown voltage. As shown in Figure 5, the standard approach for active clamping is to use TVS Diodes connected between the drain and the gate. When the V_{DS} voltage exceeds the TVS breakdown voltage, the TVS starts to conduct and this current will cause the gate-source voltage to increase. Thus, the MOSFET is still held in an active mode and the turnoff process is prolonged. As a result, voltage overshoot and turn-off overvoltage ΔV_{DS} are reduced.

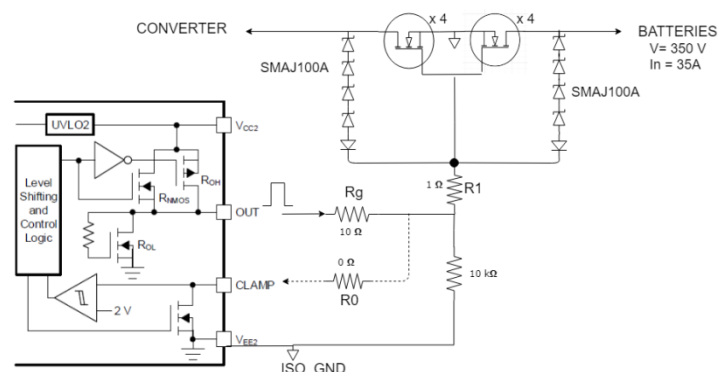


Fig. 5 Circuit design of TVS and driver clamping to prevent both: false turn-on and overvoltage

An LtSpice simulation of the turn-off of 35 Amps has been done using SPICE model of the used component: TVS (4 SMAJ100 in series) and MOSFET (4 STW77N65M5 in parallel). As seen in Figure 6, no overvoltage V_{DS} has been detected and voltage is maintained less than 600 V during turn-off. During the 8 μs for turning-off, the total dissipated energy is 92 mJ for each array of transistors which is in compliant with the specifications in table 1.

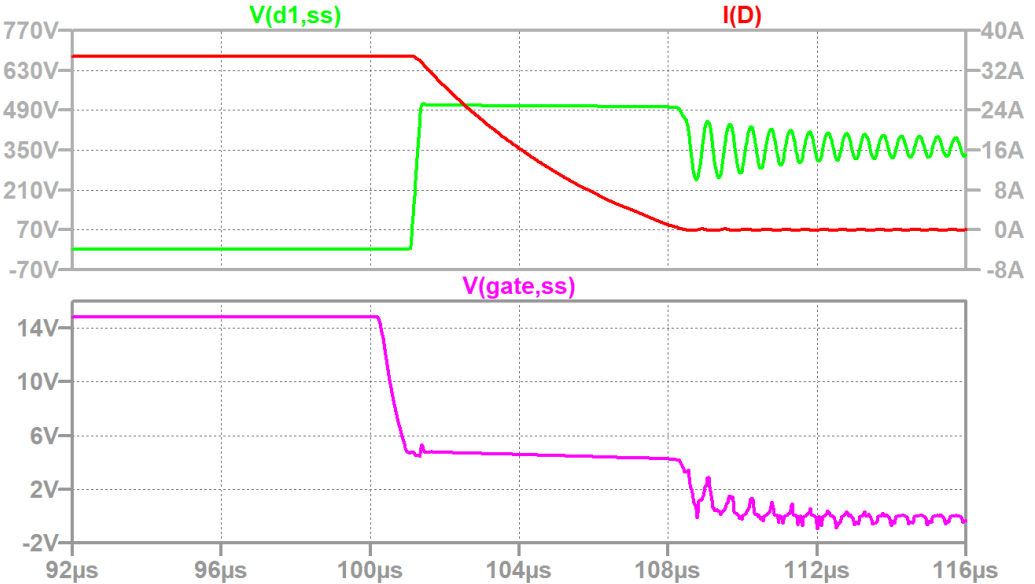


Fig. 6 Simulation of turn-off MOSFET showing: V_{DS} (green), I_D (red) and V_{GS} (purple).

Experimental results

The PCB has been manufactured as shown in the Fig. 7-b following the thermal study done in the paragraph III. In order to test the performances of the PCB, the synopsis in the Fig.1 has been applied. At this stage, both the converter and the EMC filter are not connected. As seen in the Fig.7-a, the battery pack has been replaced by an inductive load ($R= 10 \Omega$, $L=7.5 \mu H$); the HVDC is represented by the power supply (350V).

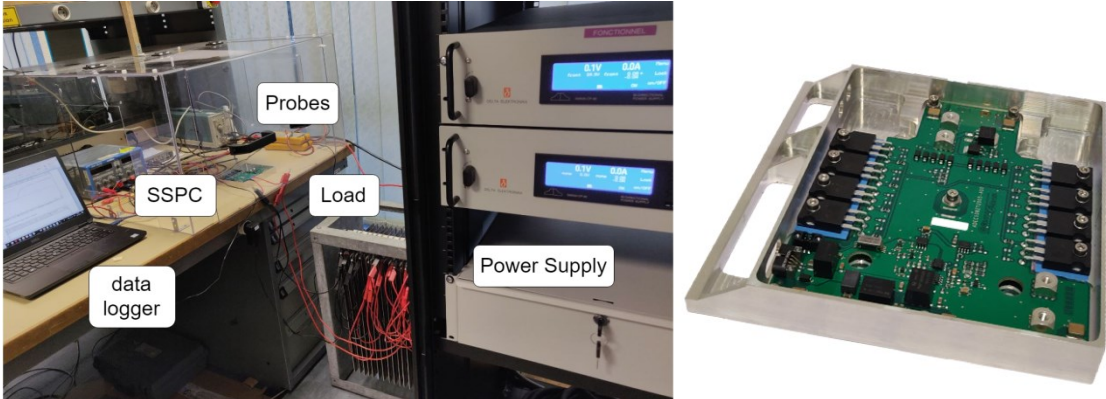


Fig. 7 The SSPC: (a) Setup of the test, (b) picture of the PCB designed

The measurements show a very good agreement with the simulations. The turn-off is as simulated before around 10 μs ; the overshoot voltage is limited by the TVS up to 500 V which is lower than the breakdown voltage of the MOSFET. The dissipated switching energy is found to be 11 mJ. Indeed, the current falls to zero much shorter in the experience.

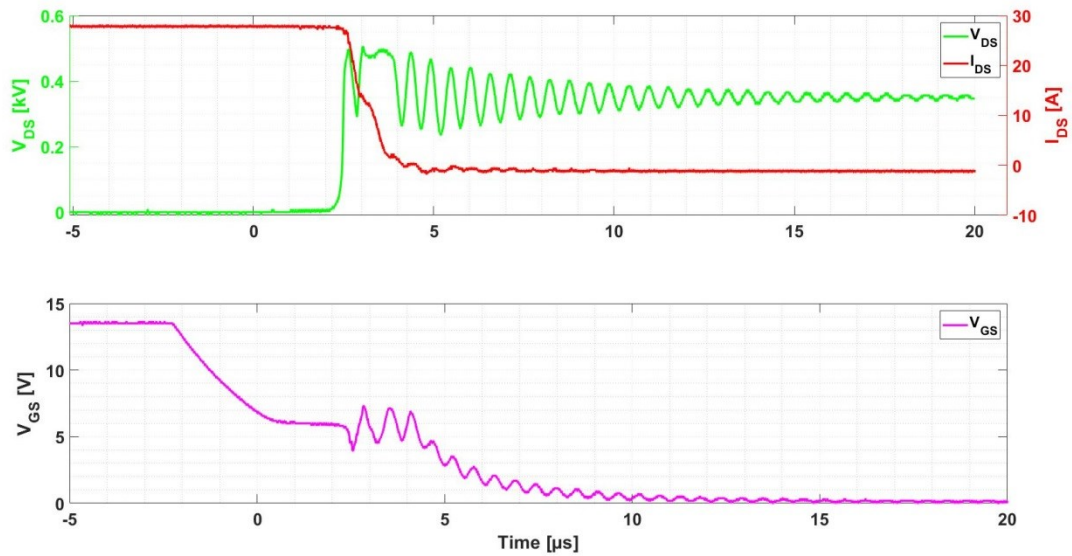


Fig. 8 Measurement of the turn-off MOSFET showing: V_{DS} (green), I_D (red) and V_{GS} (blue).

Conclusion

For better power density, SSPC replaces advantageously heavy circuit breaker dedicated to high power application. This paper proposes a methodology to draw the specifications regarding environmental conditions. At the same time, it shows a design of SSPC which is able to cut off current up to 350 A under 650 V nominal voltage. Active clamping is integrated to reduce drain-source over-voltage during cut-off. A PCB has been manufactured and tested. A very good agreement has been shown between the simulation and the measurements at the nominal current (35 A). The next step would be the test at the short-circuit current (350 A).

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