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Voltage controlled sub-THz detection with gated planar asymmetric nanochannels

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This letter reports on room temperature sub-THz detection using self-switching diodes based on an AlGaIn/GaN heterostructure on a Si substrate. By means of free-space measurements at 300 GHz, we demonstrate that the responsivity and noise equivalent power (NEP) of sub-THz detectors based on planar asymmetric nanochannels can be improved and voltage controlled by means of a top gate electrode. A simple quasi-static model based on the DC measurements of the current-voltage curves is able to predict the role of the gate bias in its performance. The best values of voltage responsivity and NEP are achieved when the gate bias approaches the threshold voltage, around 600 V/W and 50 pW/Hz^{1/2}, respectively. A good agreement is found between modeled results and those obtained from RF measurements under probes at low frequency (900 MHz) and in free-space at 300 GHz. *Published by AIP Publishing.* <https://doi.org/10.1063/1.5041507>

In the last few years, different THz detectors have been investigated, looking for larger bandwidth and lower noise, with increasing practical interest in security, medical imaging, and high speed short range communications, among other fields.¹ A non-classic architecture based on a single nanolithography step allowing to define an asymmetric planar diode so-called Self-Switching diode (SSD) was proposed by Song in 2003.² This particular geometry propagates the applied bias into a lateral field effect, which depending on the polarity is able to open or close the channel because of electrostatic and surface effects.³ The use of high mobility materials like InGaAs,⁴ InAs,⁵ or graphene⁶ for fabricating SSDs has allowed envisaging its use in relevant THz applications such as zero-bias detectors for passive imaging. In addition, GaN despite its lower mobility is also suitable for sub-THz detection.⁷ In all the cases, reducing the channel width is the first strategy to enhance the performance of SSDs as detectors.⁸ However, this has a drawback: the variability on their performance. It is difficult to precisely control such a stringent fabrication process and reproducibly fabricate SSDs with channel widths below 100 nm. Moreover, the detection performance depends on the non-linearity of the I-V curve of the SSDs, which critically depends on the presence of surface charges at the sidewalls of the channels, so that many unknown trap mechanisms, especially in the GaN technology, arise.⁹

In order to control the conductance of planar nanochannels, different solutions based on the field effect have been proposed: (i) in-plane gates, where the confining electric field is parallel to the two-dimensional electron gas (2DEG),^{10–13} which provide the transistor effect and voltage-tunability of their I-V curves or (ii) top Schottky contact (SC) gates,¹⁴ used not only in FETs but also in

countless semiconductor devices including ballistic devices¹⁵ and Gunn diodes.¹⁶ In this work, we explore the benefits on the main figures of merit of RF detectors, i.e., responsivity (β) and noise equivalent power (NEP), of adding a SC gate on the top of SSDs fabricated on GaN, as sketched in Fig. 1(a). The conventional vertical field effect mechanism for gating the carrier density in these devices, which we will call gated-SSDs (G-SSDs), will be studied. The advantage of G-SSDs over standard FETs, also showing a nonlinearity in the drain current vs. drain-to-source voltage curves (I_D - V_{DS}) originated from the gate electrode, is that the responsivity of G-SSDs has an additional contribution coming from the lateral field effect (associated with the SSD shape), superimposed to the effect of the top gate.

The characterized G-SSDs are based in an AlGaIn/GaN heterojunction on a Si substrate grown by EpiGaIn consisting of a 25 nm thick AlGaIn barrier (with 35% Al content) on top of a 1.5 μm thick GaN buffer. The fabrication process is similar to that of the recess technology presented in Ref. 8, in which, after the dry etching of the trenches, a final step associated with the top gate fabrication is added. This step is done as following: e beam writing of the PMMA and Argon

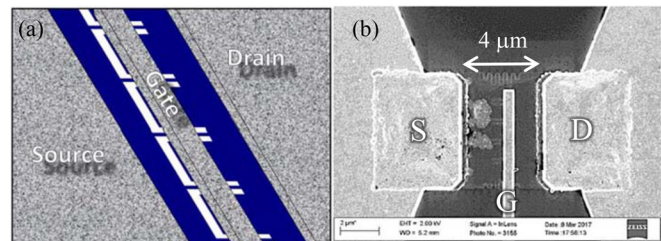


FIG. 1. (a) Sketch of a G-SSD and (b) SEM view of an array of 4 GaN SSDs with a top gate. The position of the source (S, at the left), drain (D, at the right), and gate (G, on the center of the channels) electrodes is also indicated.

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etching, followed by a Ni/Au evaporation (40 nm/300 nm, respectively). The device under test has 4 channels in parallel, approximately 70–100 nm wide and 1.0 μm long. The 500 nm gate electrode is located at the center of the channel, as shown in Fig. 1(b).

First, using a semiconductor analyzer (Keithley 4200-SCS), G-SSDs have been characterized in the DC regime at room temperature. Figure 2 shows the output curves of the devices, demonstrating good transistor operation, in spite of the appearance of a non-negligible gate leakage current, most probably associated with electrons injected from the gate through the lateral walls of the trenches. On the transfer characteristics (I_D vs. gate-to-source voltage, V_{GS}), not shown here, it is observed that the threshold voltage, V_{TH} , is more negative as V_{DS} increases, a well-known short channel effect (drain induced barrier lowering). Since G-SSDs will be used not as transistors but as zero-bias detectors, their usual operation point is not in saturation, but no V_{DS} is applied. Therefore, as a reference for calculating the gate voltage overdrive, we will use the threshold voltage determined for the lowest values of V_{DS} , $V_{TH} = -1.6$ V. In the inset, the current measured in a G-SSD with a floating gate (gate in the open circuit) and that of a usual SSD without a gate electrode, with a similar channel geometry (width of 74 nm), are compared to that of the G-SSD with $V_{GS} = 0.0$ V. According to this result, it is clear that the inclusion of a SC gate has a significant impact reducing the depletion region imposed by the surface charges at the lateral trench walls, thus opening the channel and increasing the current. Figure 2 also shows that, as expected, the gate electrode of the G-SSD screens the drain voltage and imposes the saturation of the drain current, not found in the SSD without gate (neither on the G-SSD with an open circuit gate).

From these DC measurements, it is possible to predict the responsivity and NEP based on the first and second derivatives of the I_D - V_{DS} curves, following the method described in Ref. 20. This quasi-static model has been satisfactorily used to analyze the performance of RF detectors based on SSDs made on InAs⁵ and GaN.²¹ By means of a polynomial

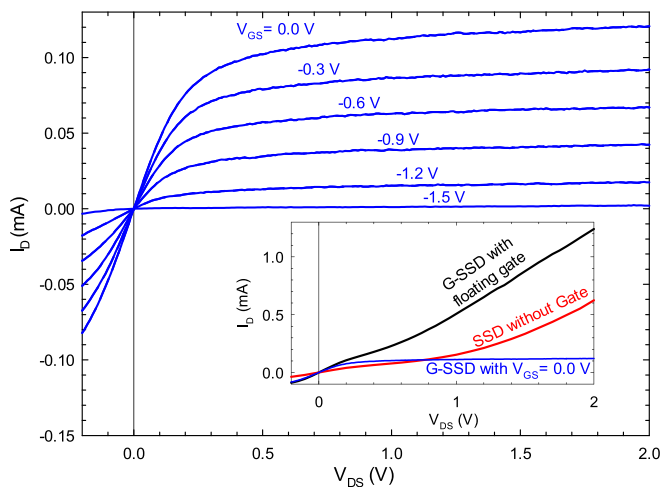


FIG. 2. Output characteristics of the G-SSD under test. The inset shows the I-V curve of the G-SSD with the gate contact in the open circuit (floating gate) and the SSD without gate with a similar geometry (74 nm width and 1.0 μm length).

fitting of order three (using 20 points within the $[-0.1$ V, $+0.1$ V] range), the values of (i) the resistance, R , and (ii) the bowing coefficient, defined as $\gamma = \left(\frac{d^2I}{dV^2}\right) / \left(\frac{dI}{dV}\right) = \left(\frac{d^2I}{dV^2}\right)R$, can be calculated. The figure of merit called matched or optimum responsivity is given by $\beta_{\text{opt}} = R\gamma/2$. γ is a normalized parameter (given in units of V^{-1}) allowing to compare different types of device architectures and whose value does not depend on the device size, i.e., the area of Schottky barrier diodes (SBDs), the gate width of FETs, or the number of parallel channels of SSDs or G-SSDs.

As expected, R and γ , shown in Fig. 3 as a function of $\Delta V = V_{GS} - V_{TH}$, increase monotonically when decreasing V_{GS} , taking values in the range of 2.0–200 k Ω and 0.2–10 V^{-1} , respectively. However, we can identify two regions depending on the gate bias. For ΔV above 0.5–0.6 V, the G-SSD behaves as a standard field effect transistor (FET), and R increases when decreasing V_{GS} , following the ideal $R \sim \Delta V^{-1}$ dependence. But when the G-SSDs approach pinch-off conditions ($\Delta V < 0.5$ V), R increases faster than expected, as ΔV^{-2} . This indicates that the current control mechanism in the G-SSDs is modified from the pure field effect gating appearing at higher V_{GS} to a more complex behavior when V_{GS} comes close to V_{TH} . Under those conditions, the depletion imposed by the surface charges at the drain side of the channel may become more important due to a stronger electron heating (due to the strong electric field caused by the large gate-drain voltage difference, V_{DG}) and thus further increasing R .

Those two regions of gate bias can also be observed in the values of γ . In open channel conditions, $\Delta V > 0.5$ V, when R is below 10 k Ω , γ goes as $R^{3/2}$, as shown in the inset of Fig. 3, so that $\gamma \sim \Delta V^{-3/2}$. However, this dependence cannot be extracted from the ideal FET theory, since it predicts a null value (as expected from a linear dependence of I_D on V_{DS}), and it is the asymmetry of the channel (the SSD geometry) which produces this nonlinearity. In the low V_{GS} region, in spite of the steeper increase in R , γ increases more slowly with decreasing gate bias as a result of a weaker dependence on R ($\gamma \sim R^{1/2}$, inset of Fig. 3) so that γ goes as

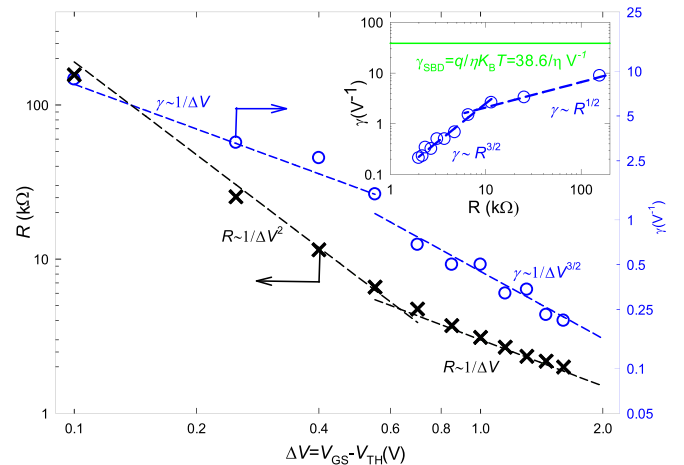


FIG. 3. Resistance, R , and bowing coefficient, γ , extracted from the DC measurements of the I_D - V_{DS} curves (shown in Fig. 2) as a function of $\Delta V = V_{GS} - V_{TH}$ at $V_{DS} = 0.0$ V. Dashed lines show different dependencies on ΔV for eye guiding. The inset shows the values of γ vs. R , with the eye guiding lines showing the $\gamma \sim R^{3/2}$ and $\gamma \sim R^{1/2}$ dependencies, appearing at high and low V_{GS} , respectively.

ΔV^{-1} . As it can be extrapolated from these γ vs. R dependencies, the value of $\left(\frac{d^2I}{dV^2}\right)$ increases with R for low R (when $\gamma \sim R^{3/2}$) and then decreases (when $\gamma \sim R^{1/2}$), peaking at about ($\Delta V \approx 0.5$ V).

Even if the change of the slope in the V_{GS} dependencies of R and γ is not extremely obvious (for this sake, eye-guiding dashed lines have been included in Fig. 3), the separation between the open-channel and near-pinch-off regions is quite evident in the γ vs. R representation in the inset of Fig. 3: a clear switch from a rapid increase in γ as $R^{3/2}$ for low V_{GS} to a slower increase as $R^{1/2}$ for the higher V_{GS} values appears at $R \sim 10$ k Ω (i.e., $\Delta V = 0.5$ – 0.6 V). The inset also shows the value of γ for devices with the exponential I-V curve (like SBDs, typically used as RF detectors), $\gamma = q/\eta k_B T$, with η being the non-ideality factor, which for $T = 300$ K and $\eta = 1$ leads to $\gamma = 38.6$ V $^{-1}$ (an invariant value regardless of the resistance of the SBD). This value of γ , which could be considered as the target for our G-SSDs (their non-linearity would be comparable to that of an exponential I-V), is approached when lowering V_{GS} , providing values not far from 10 V $^{-1}$.

In order to demonstrate their potentiality as sub-THz detectors, the devices were integrated with broadband bow-tie antennas, as shown in the inset of Fig. 4. A solid-state harmonic generator with an output power of ~ 6 mW at 300 GHz was used to excite the G-SSD. The induced V_{DS} was measured at room temperature using a lock-in technique with a mechanical chopper. More details about the set-up can be found in Ref. 17. In this kind of configuration, optical losses (focusing, wave propagation, normalization due to beam spot and device size) are very difficult to estimate, so that in Fig. 4, we just present the output voltage, V_o , measured at the drain. This figure shows that the photoresponse increases sharply when V_{GS} approaches the threshold voltage and then saturates within the subthreshold region. This behavior is similar to that obtained in other FETs as shown in Ref. 18.

With the aim of having a better quantitative estimation of the responsivity of the devices, we have also characterized the G-SSD as a power detector under probes, also at room temperature. In this case, the average V_{DS} output voltage, V_o , was measured while simultaneously biasing the device with $I_D = 0$ (through a bias tee) and the corresponding V_{GS} . The input signal is provided by means of a vector network

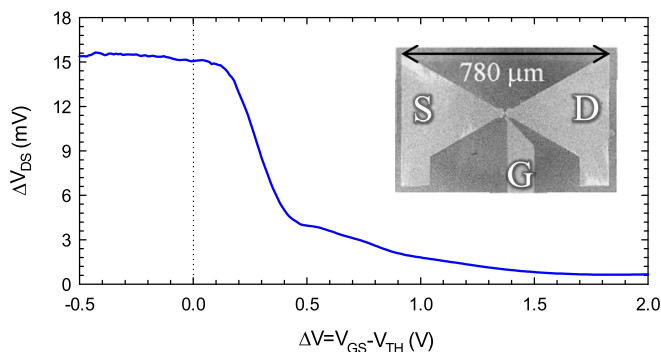


FIG. 4. Output voltage when illuminating the sample with a 300 GHz beam as a function of $\Delta V = V_{GS} - V_{TH}$ at $I_D = 0$. The inset shows the geometry of the bow-tie integrated antenna.

analyzer (Keysight PNA X N5244) with a power range of $P_{VNA} = [-20$ dBm, $+10$ dBm]. Since coplanar waveguide accesses were not available for the G-SSD, the RF measurements were performed using DC needles at relatively low frequency, 900 MHz. In order to calibrate the electrical losses associated with this setup, a power compensation is required. For that purpose, a previous measurement with both RF probes and DC needles was done on SSDs without gate (with integrated RF accesses), providing a value of 10 dB losses. Thus, the voltage responsivity of the G-SSD is calculated as $\beta = V_o / (P_{VNA} - 10$ dB), which is constant in the whole range of input power used in these RF measurements, meaning that the device behaves as a square-law detector. On the other hand, the noise equivalent power, NEP, is obtained as $NEP = (4k_B T R)^{1/2} / \beta$, using the ideal value of the noise power of the G-SSD given by the Nyquist theorem. In the case of the free space measurements, β and NEP are calculated in the same way but the coupling and mismatch losses have been estimated by fitting the free-space results to the RF measurements at $\Delta V = 0.1$ V, thus giving a value of 27 dB losses, approximately.

Figure 5 compares the values of β and NEP as a function of ΔV measured in free-space (@300 GHz) and under probes (@900 MHz), with the calculations using the previously presented quasi-static model. In fact, β can also be extracted from the DC measurements of γ and R by taking into account the impedance mismatch factor $M_0 = 4Z_0 R / (R + Z_0)^2$, so that $\beta = \beta_{opt} \times M_0 = R\gamma/2 \times M_0$, where the characteristic impedance is $Z_0 = 50$ Ω . DC, RF, and free space results show a reasonable agreement, the slight disagreement probably due not only to the power losses but also to the difficult

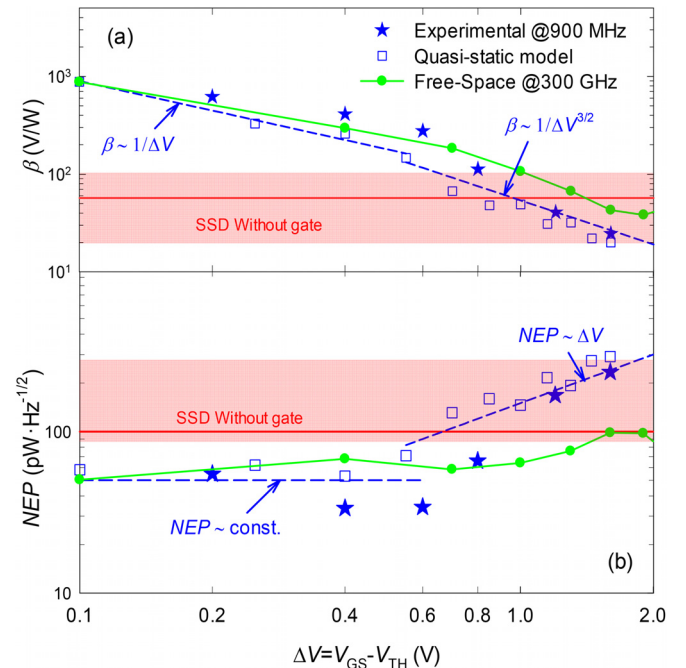


FIG. 5. Comparison of the values of (a) β and (b) NEP vs. ΔV (at $V_{DS} = 0.0$ V) calculated from the DC measurements (quasi-static model) with those obtained in the experimental free-space setup at 300 GHz and the RF measurements at 900 MHz. The values for the SSD without gate and the same geometry are shown by the horizontal solid line,²⁰ while the results of GaN based SSDs with other geometries (fabricated in the same run and published in the literature^{7,8}) are covered by the shaded regions.

extraction of the values of γ from very small values of current in the case of the quasi-static model and the frequency dependence of the impedance of the devices that could affect the value of the mismatch factor for the different frequency ranges.

The increase in β when lowering the gate bias shows the same trends as those of γ [Figs. 3 and 5(a)], $\beta \sim \Delta V^{-3/2}$, and $\beta \sim \Delta V^{-1/2}$ in the ΔV regions above and below 0.5–0.6 V, respectively. This happens because when R is very high, as occurs in our G-SSD, the value of the responsivity approaches $\beta \approx 2\gamma Z_0 = 100\gamma$.¹⁹ Therefore, β is just proportional to γ , i.e., depends only on the non-linearity of the I_D – V_{DS} curves. Figure 5(a) also shows the values of β obtained in ungated SSDs.^{7,8,20,21} Interestingly, the value of the responsivity of the G-SSD overcomes that of ungated SSDs when entering the near pinch-off gate bias region ($\Delta V < 0.5$ V). This is also an evidence that under those conditions, an additional current control mechanism is in action. Remarkably, this leads to values of responsivity as high as 600 V/W never obtained previously in ungated SSDs, even with the optimum geometry (the highest responsivity, 100 V/W, was obtained with an extremely narrow channel defined by ion implantation⁷). Regarding the NEP, in open channel conditions, it decreases when lowering V_{GS} as ΔV^{-1} (as follows from the $\Delta V^{-3/2}$ and ΔV^{-1} dependencies of β and R , respectively), reaching a nearly constant value for $\Delta V < 0.5$ V (where the ΔV^{-1} and ΔV^{-2} trends of β and R cancel each other). As a consequence, the value of NEP decreases below 50 pW·Hz^{-1/2}.

These results show that the performance of the G-SSD architecture can approach the state-of-the-art of mm- and sub-mm-wave detectors, since the impedance-tunability provided by the voltage control of the characteristics of the device can be combined with additional design efforts aiming to mitigate the strong mismatch presented by these devices, such as the increase in the number of parallel channels and the use of high impedance access lines.

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