



HAL
open science

BIST-Assisted Analog Fault Diagnosis

Antonios Pavlidis, Eric Faehn, Marie-Minerve Louërat, Haralampos-G.
Stratigopoulos

► **To cite this version:**

Antonios Pavlidis, Eric Faehn, Marie-Minerve Louërat, Haralampos-G. Stratigopoulos. BIST-Assisted Analog Fault Diagnosis. 26th IEEE European Test Symposium, May 2021, Bruges (virtual), Belgium. pp.1-6, 10.1109/ETS50041.2021.9465386 . hal-03181937

HAL Id: hal-03181937

<https://hal.science/hal-03181937v1>

Submitted on 26 Mar 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

BIST-Assisted Analog Fault Diagnosis

Antonios Pavlidis*, Eric Faehn[†], Marie-Minerve Louërat*, Haralampos-G. Stratigopoulos*

*Sorbonne Université, CNRS, LIP6, Paris, France

[†]ST Microelectronics, Crolles, France

Abstract—Fault diagnosis methodologies for analog circuits lag far behind those for their digital counterparts. In this paper, we show how the generic Symmetry-based Built-In Self-Test (BIST) (or *SymBIST*), originally proposed for defect-oriented post-manufacturing test and on-line test, can be seamlessly reused for the purpose of diagnosis. BIST can offer better insights into the circuit and, thereby, can assist diagnosis towards resolving ambiguity groups. Using *SymBIST* we demonstrate high diagnosis resolution and fast diagnosis cycle for an industrial Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC).

I. INTRODUCTION

Fault diagnosis refers to the analysis performed to identify the root cause of failure that occurred in an Integrated Circuit (IC) either during manufacturing or in the field during normal operation following a customer return. The output is the isolation of the defect responsible for the failure and its localization at transistor-level.

Diagnosis is a crucial step in a product life-cycle. It can reveal important statistics, such as defect distribution and yield detractors. In this way, it provides valuable feedback for improving the design to prevent failure re-occurrence and expand the safety features, and also for evaluating and improving the quality of post-manufacturing tests.

In a first step, diagnosis generates a set of candidate defects based on diagnostic measurements or observed syndromes. In a second step, the IC is physically examined, for example using a thermal camera, to highlight anomalies in the operation and narrow down further the set of candidate defects. In the third and last step, the IC is submitted to Physical Failure Analysis (PFA) where de-layering and cross-sectioning of the die is performed to confirm the defect using imaging. Since PFA is destructive and irreversible, ideally the first step should pinpoint the actual defect. However, very often the first step results in an ambiguity group of candidate defects. According to industrial experience, its size should be less than 5-10 candidate defects to increase the PFA success rate.

Diagnosis metrics include: (a) resolution, i.e., the size of the ambiguity group; (b) accuracy, i.e., whether a reported candidate corresponds to the actual defect; and (c) diagnosis cycle time, i.e., the time required to complete the diagnosis since the number of diagnoses performed per week per design can be in the order of thousands [1].

While for digital ICs there exist several in-house frameworks and commercial Electronic Design Automation (EDA) tools for diagnosis [1], [2], for analog ICs there exists neither a commercial tool nor a standardized diagnosis approach. Analog fault diagnosis is still an ad-hoc, manual, tedious, and time-consuming process very often resulting in large ambiguity groups and no actionable diagnosis information.

The traditional approach is a rule-based system which takes the form “IF symptom(s) THEN defect(s)” [3]; however it is difficult to acquire the knowledge to build such a system.

Model-based diagnosis approaches have also been studied extensively. The idea is to first build a model linking diagnostic measurements to circuit parameters. Then, given the diagnostic measurements from the real failing device, the model is used to identify the faulty circuit parameter, as well as its deviation from the nominal value. The model can be constructed using nonlinear circuit equations [4], sensitivity analysis [5], regression [6], or behavioral modeling [7]. This approach can be used for diagnosis of soft faults, i.e., deviations of circuit parameters; however, it is recognized that hard faults, i.e., defects such as short- and open-circuits, are the main root cause of IC failures [8]. Besides, it is challenging to build a model that faithfully reproduces the analog IC behavior.

Perhaps the most common diagnosis approach is based on the use of a fault dictionary. Given a list of defects generated by Inductive Fault Analysis (IFA) [8], one defect is injected at a time in the netlist, and the IC is simulated to obtain the diagnostic measurement pattern. The fault dictionary contains the pairs of defects and diagnostic measurement patterns. Then, the diagnostic measurement pattern from the failed IC is mapped to one of the logged diagnostic measurement patterns of simulated defects based on some similarity metric. The mapping can be established after training a multi-class classifier using the fault dictionary dataset [9], [10]. The challenge with this approach is the long defect simulation time. However, the recently proposed analog defect simulators [11]–[13] can help speed up the fault dictionary generation as demonstrated in [14].

In this paper, we investigate the use of Built-In Self-Test (BIST) in the context of analog fault diagnosis. Traditionally, BIST aims at adding on-chip test structures so to facilitate and reduce the cost of post-manufacturing test. BIST can offer better insights into the circuit and, thereby, can assist diagnosis towards resolving ambiguity groups [15]. We assume that the BIST infrastructure is already in place for post-manufacturing test and is reused for diagnosis “as is”. We opt for using generic BIST virtually applicable to any analog IC class, such that the BIST-assisted diagnosis paradigm is also generic. Our starting point is the recently proposed generic Symmetry-based BIST (*SymBIST*) [16], [17], which has been demonstrated for defect-oriented post-manufacturing test and on-line test. Herein, we demonstrate how *SymBIST* can be utilized for fault diagnosis too. Our case study is a 65nm 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) IP by ST Microelectronics (STM) that comprises several hundreds of

transistors.

The rest of the paper is structured as follows. In Section II, we provide a concise overview of the *SymBIST* operation. In Section III, we present the use of *SymBIST* for diagnosis. In Section IV, we present the case study. In Section V, we discuss defect modelling and simulation. In Section VI, we present the diagnosis results. Section VII concludes the paper.

II. *SymBIST* OVERVIEW

The central idea in *SymBIST* [16], [17] is to build invariant signals (or *invariances*) by monitoring internal nodes. An invariance is defined as a signal with a constant value irrespective of the input. It takes the form $f_k(\mathbf{V}) = 0$, where \mathbf{V} is a vector containing the voltages of the monitored nodes and k denotes the invariance number. Then, one checker is used per invariance. The checker constructs and monitors the invariance and provides a pass or fail output, corresponding to invariance compliance or violation, respectively. Invariance violation flags an anomaly in operation pointing to defect detection. The convention used is that 0/1 corresponds to pass/fail.

In practice, a true invariance cannot exist due to noise and process, voltage, and temperature (PVT) variations. The invariance is a small peak-to-peak signal and the checker examines whether it stays within a tolerance window, e.g. $|f_k(\mathbf{V})| < \delta$, $\delta > 0$. The tolerance window $[-\delta, \delta]$ is set by simulating the complete nominal design, including the *SymBIST* infrastructure, while considering noise, Monte Carlo (MC) analysis, and power supply and temperature fluctuations. The tolerance window defines a trade-off between yield loss and test escapes. By enlarging it we reduce yield loss (or false positives) possibly at the expense of test escapes (or false negatives).

The invariances can be built by exploiting existing symmetries into the design, i.e. fully-differential paths, complementary signals, replicated sub-blocks, etc. Invariance building is a circuit-specific problem, but such symmetries exist virtually in every Analog and Mixed-Signal (A/M-S) IC rendering *SymBIST* a generic BIST paradigm.

Since the invariances hold true for any input, we can craft a test stimulus, possibly relying on some internal re-configuration, such that the entire design is excited in very short time, thus concluding quickly on the presence or not of a defect. This property results in a small simulation time, enabling defect coverage evaluation of large A/M-S designs.

In practice, a small number of invariances can be used to cover the entire design thanks to feedback loops and block chains. Thus, the *SymBIST* area overhead, which is dominated by the checkers' area, can be very small.

Finally, since the invariances hold true for a running input, *SymBIST* can be reused for on-line concurrent error detection during normal operation [17].

III. DIAGNOSIS USING *SymBIST*

Let $C_k(t)$ denote the time-varying checker output for the k -th invariance, $k = 1, \dots, K$, where K is the number of invariances. For a checker clocked at a frequency f_{clk} , $C_k(t)$ is a bitstring with period $1/f_{clk}$. We consider the vector $C_k[t_i]$ of $n = T \cdot f_{clk}$ bits, where T is the duration of the

test stimulus and t_i are sampling times at half-period, i.e. $t_i = i \cdot (1/2f_{clk})$, $i = 1, \dots, n$. If the invariance is permanently satisfied (violated), then $C_k[t_i]$ will be a vector of zeros (ones). It is likely, however, that a defect will cause the invariance to slide outside the tolerance window at specific clock cycles, in which case $C_k[t_i]$ will be a vector containing both zeros and ones. We use the vector $C_k[t_i]$ as an n -bit digital diagnostic measurement pattern.

This diagnostic measurement pattern is a function of the parameters of the *SymBIST* setup. In general, this set of parameters includes the primary test stimulus to the IC denoted by I_{pri} , internally generated test stimuli denoted by I_{int} , and the tolerance window defined by δ . We can consider unequal tolerance window limits δ_- and δ_+ , i.e. the tolerance window becomes $[\delta_-, \delta_+]$. A setup may involve also some internal re-configuration denoted by R . Let

$$S^\ell = \{I_{pri}^\ell, I_{int}^\ell, R^\ell, \delta_-^\ell, \delta_+^\ell\} \quad (1)$$

denote the set of parameters of the ℓ -th *SymBIST* setup, $\ell = 1, \dots, L$, where L is the number of *SymBIST* setups.

In post-manufacturing test, the tolerance window sets a desired trade-off between test escapes and yield loss. In contrast, in diagnosis, the placement of the tolerance window can target uniquely exposing defects. For example, consider a defect that results in a time-varying invariant signal that is permanently above the upper limit of the tolerance window. By placing a higher upper limit at the average value of the invariant signal, we can obtain a vector $C_k[t_i]$ that toggles between 1 and 0, potentially offering a good diagnostic measurement pattern for this defect.

We follow a fault dictionary approach assuming a list of N_f defects denoted by F_j , $j = 1, \dots, N_f$. The diagnostic measurement pattern for defect F_j obtained by the k -th checker using the ℓ -th *SymBIST* setup is denoted by $C_k^{F_j, \ell}[t_i]$.

Combining the diagnostic measurement patterns of K checkers monitoring the K invariances and considering L *SymBIST* setups, we obtain a diagnostic measurement pattern for defect F_j in the form of a $K \times L \times n$ bitstring

$$DM(F_j) = [C_1^{F_j, 1}, \dots, C_K^{F_j, 1}, \dots, C_1^{F_j, L}, \dots, C_K^{F_j, L}]. \quad (2)$$

The diagnosis objective is that the Hamming Distance (HD) of the diagnostic measurement patterns of any two defects differs at least by 1, which can be expressed as

$$HD(DM(F_a), DM(F_b)) > 1, a \neq b. \quad (3)$$

An ambiguity group is a set of defects for which the HD of the diagnostic measurements of any pair of defects is 0.

In the diagnosis phase of faulty device X , the diagnostic measurement pattern DM_X is first obtained and then matched with a row in the fault dictionary matrix

$$\begin{bmatrix} DM(F_1) \\ \vdots \\ DM(F_{N_f}) \end{bmatrix}, \quad (4)$$

which has the diagnostic measurement pattern of defect j in row j . The row number points to the diagnosed defect.

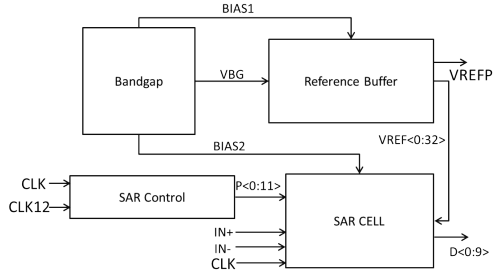


Fig. 1: Top-level architecture of 10-bit SAR ADC IP by STM.

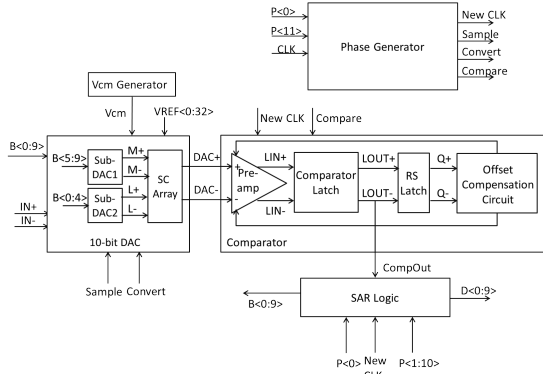


Fig. 2: Top-level architecture of SARCELL block.

SymBIST setups are sequentially added by searching in the space of test stimuli, tolerance window limits, and re-configurations, so as to enrich the digital diagnostic measurement pattern towards resolving the ambiguity groups.

IV. CASE STUDY

We use the same case study, i.e., a 10-bit SAR ADC IP by STM, employed in [16], [17]. Herein, we reintroduce the case study in Sections IV-A-IV-F for the purpose of completeness. The *SymBIST* setups for diagnosis are discussed in Section IV-G.

Previous BIST approaches for SAR ADCs are functional aiming at measuring Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) [18], [19]. They require long simulation times and, thus, large-scale defect simulation to generate the fault dictionary becomes cumbersome. In contrast, *SymBIST* offers a negligible simulation time and can be used in this context.

A. SAR ADC IP architecture

Fig. 1 shows the top-level architecture. The circuit accepts a fully-differential input $\Delta IN = IN+ - IN-$. CLK is the master clock with frequency $f_{clk} = 156$ MHz. The 10-bit digital code during the conversion is denoted by $B<0:9>$, and at the end of the conversion it is latched at the output $D<0:9>$. The SARCELL, whose top-level architecture is shown Fig. 2, is the main block which implements the SAR algorithm.

B. Invariances

The following invariances are identified covering the entire A/M-S part of the SAR ADC IP:

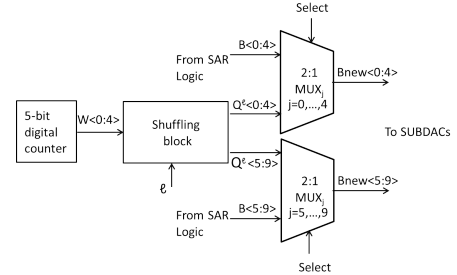


Fig. 3: On-chip generation of dynamic test stimulus.

$$M+ + M- = VREF[32] \quad (5)$$

$$L+ + L- = VREF[32] \quad (6)$$

$$DAC+ + DAC- = 2V_{cm} \quad (7)$$

$$LIN+ + LIN- = 2V_{cm2} \quad (8)$$

$$Q+ + Q- = VDD \quad (9)$$

$$\text{sgn}(Q+ - Q-) - \text{sgn}(LIN+ - LIN-) = 0 \quad (10)$$

where $VREF[32]$ is the largest reference voltage created by the Reference Buffer, $M+$ and $M-$ are complimentary comparison levels created by SUBDAC1 using the reference voltages $VREF<0:32>$ while converting the 5 Most Significant Bits (MSBs) $B<5:9>$, $L+$ and $L-$ are complimentary comparison levels created by SUBDAC2 using the reference voltages $VREF<0:32>$ while converting the 5 Least Significant Bits (LSBs) $B<0:4>$, $DAC+$ and $DAC-$ are the fully-differential outputs of the DAC, $LIN+$ and $LIN-$ are the fully-differential outputs of the pre-amplifier, $Q+$ and $Q-$ are the complimentary digital outputs of the RS Latch, V_{cm} is the common mode used inside the DAC, and V_{cm2} is the common mode at the outputs of the pre-amplifier. The signals composing the invariances are annotated in Figs. 1 and 2.

C. Test stimulus

The test stimulus has two parts, namely a static and a dynamic, and both parts can be robustly generated on-chip. The static part is simply a DC input to the ADC, denoted by ΔIN_{DC} . The dynamic part is a set of digital test patterns that are applied sequentially to the inputs of the two SUBDACs. More specifically, we cycle through all 2^5 bit combinations at the inputs of each SUBDAC. The SUBDAC input sequence generator is shown in Fig. 3. A 5-bit digital counter is used to generate the incremental counting $W<0:4>$ and a shuffling block is used to shuffle its outputs so as to generate the digital test stimuli $Q<0:4>$ and $Q<5:9>$ that cycle non-incrementally through all 2^5 bit combinations at the inputs of each SUBDAC. The shuffling block can be programmed to implement different cycles. Then, 10 2:1 multiplexers are used to switch during test mode the inputs of the SUBDACs, denoted now by $Bnew<0:4>$ and $Bnew<5:9>$, from the SAR Logic outputs $B<0:4>$ and $B<5:9>$ to $Q<0:4>$ and $Q<5:9>$, respectively.

D. Checker design

Invariances in Eqs. (5)-(9) are of type $V_1 + V_2 = c$ and are constructed and monitored using the checker in Fig. 4. It can be shown that $V_o = A + G \cdot (V_1 + V_2)$, where A is a function of

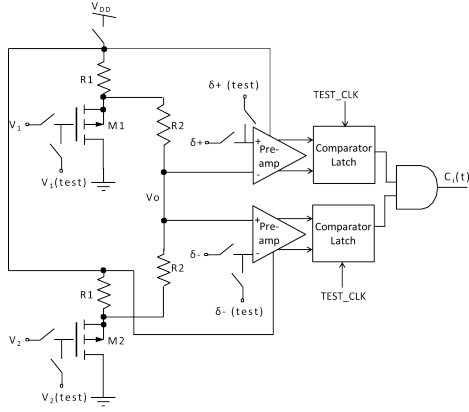


Fig. 4: Checker design for the invariances in Eqs. (5)-(9).

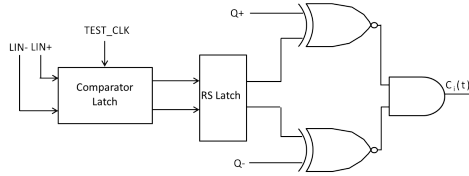


Fig. 5: Checker design for the invariance in Eq. (10).

the DC components of V_1 and V_2 and G is a gain quantity. In error-free operation, V_o is a DC signal with value $A + G \cdot c$. A defect will shift the DC component of V_o and/or will add an AC component, causing V_o to slide outside the tolerance window $[\delta_-, \delta_+]$, and raising the output from 0 to 1. The switches are used to disconnect the checker when *SymBIST* is disabled or to set the checker into self-test mode so as to verify its operation before it is used for diagnosis [17].

Fig. 5 shows the checker design for the invariance in Eq. (10). Note that this checker does not implement a tolerance window since the comparison is built from digital signals.

E. *SymBIST* test time

In total, 6 checkers are used, and the same test stimulus is used to check all invariances in parallel. The duration of the test stimulus is 2^5 clock cycles, which corresponds to a test time $T = 2^5 \cdot (1/f_{clk}) = 0.205\mu s$ per *SymBIST* setup.

F. Overheads

The test stimulus is composed of a DC static part and a digital dynamic part, while the checkers' output is an 1-bit response. Thus, *SymBIST* can be interfaced with a standard digital test access and control mechanism based on two external pins which is the minimum [20].

The *SymBIST* infrastructure is totally non-intrusive to the SAR ADC operation. The checkers in Figs. 4 and 5 have buffers as their first stage and the test stimulus generator in Fig. 3 is in a non-critical signal path. The zero performance penalty is confirmed by transistor-level DNL and INL simulations using a ramp histogram test [17].

The *SymBIST* infrastructure area overhead is roughly 5%.

G. *SymBIST* for diagnosis

A *SymBIST* setup is composed of the triplet:

$$S^\ell = \{\Delta IN_{DC}^\ell, Q^\ell < 0 : 9 >, \delta^\ell\}, \quad (11)$$

where ℓ denotes the setup index and δ^ℓ is a 2×5 vector containing the lower and upper limits of the tolerance window of the checkers monitoring the invariances in Eqs. (5)-(9).

Each checker provides a 32-bit diagnostic measurement pattern. Their concatenation results in a diagnostic measurement pattern of length $6 \times 32 = 192$ bits per *SymBIST* setup.

The first *SymBIST* setup is the same one used for post-manufacturing defect-oriented test [16], [17]. This setup uses $\Delta IN_{DC} = 0.1V$, the tolerance windows for the invariances in Eqs. (5)-(9) are placed at $\pm 5 \cdot \sigma$ so as to have negligible yield loss, and the implemented shuffling in Fig. 3 is $Q[j+5]=W[4-j]$ for SUBDAC1 and $Q[j]=W[4-j]$ for SUBDAC2, $j = 0, \dots, 4$. For example, for SUBDAC1, the input sequence is $\{2^4, 2^3, 2^4 + 2^3, 2^2, 2^2 + 2^4, \dots\}$. Then, additional *SymBIST* setups are used to resolve ambiguity groups. These *SymBIST* setups have a different combination of DC fully-differential input, DAC input sequence, and tolerance window widths for each checker. Generating the fault dictionary matrix in Eq. (4) for one *SymBIST* setup takes roughly one day. Thus, using an optimization algorithm to search in the space of *SymBIST* setups is computationally expensive, even if this is an off-line analysis. To this end, the next *SymBIST* setup is crafted based on the unresolved ambiguity groups so far with the aim to split them into smaller size groups, preferably uniquely detecting the defects composing them. For example, we can try a different input DAC sequence to split an ambiguity group with defects into the SUBDACs, we can increase (decrease) the upper (lower) tolerance window limit for an ambiguity group where the defects cause the invariance to exceed the nominal upper (lower) tolerance window limit, etc. We stop adding *SymBIST* setups when diagnosis resolution stops improving.

V. DEFECT MODELLING AND SIMULATION

We consider only the analog blocks and analog sections of the mixed-signal blocks of the SAR ADC IP. Digital blocks and digital sections of mixed-signal blocks can be tackled by digital diagnosis tools. Referring to Figs. 1 and 2, purely digital blocks excluded from the analysis are the SAR Control, Phase Generator, SAR Logic, and RS Latch. Moreover, the digital sections of the two SUBDACs are excluded.

To automate defect simulation we rely on the mixed-signal defect simulator tool Tessent®DefectSim by Mentor®, A Siemens Business [11].

We make a single defect assumption and we adopt the default defect model in the tool [11]. In particular, for MOS transistors we use only gate open and drain-to-source short defects. We use a default drain-to-source short resistance of 10Ω [11]. Regarding gate opens, we use the modeling approach proposed in [21]. In particular, V_{GS} is controlled by V_{DS} with a gain coefficient that is set to a default value of 0.5 [11]. For resistors and capacitors, we consider $\pm 50\%$ variations. The total defect count is $N_f = 648$.

VI. RESULTS

Fig. 6 shows a transistor-level transient simulation for two short defects within the SUBDAC1. The middle subplot shows the invariant signal in Eq. (6) for the defect-free and the two

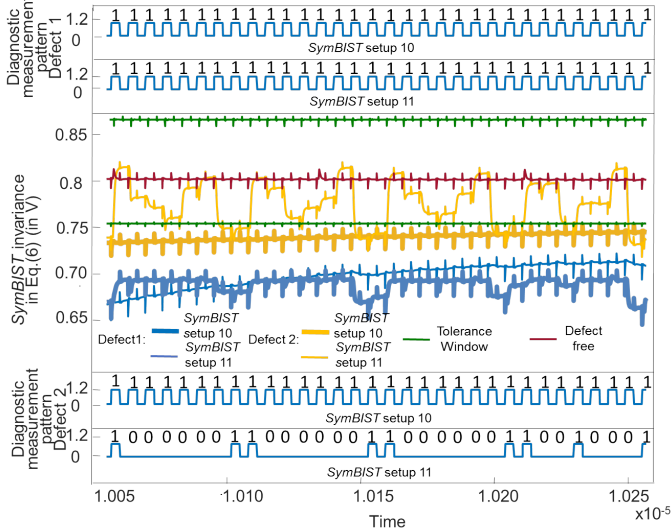


Fig. 6: Transient simulation of *SymBIST* invariance in Eq. (6) for two defects considering two different *SymBIST* setups.

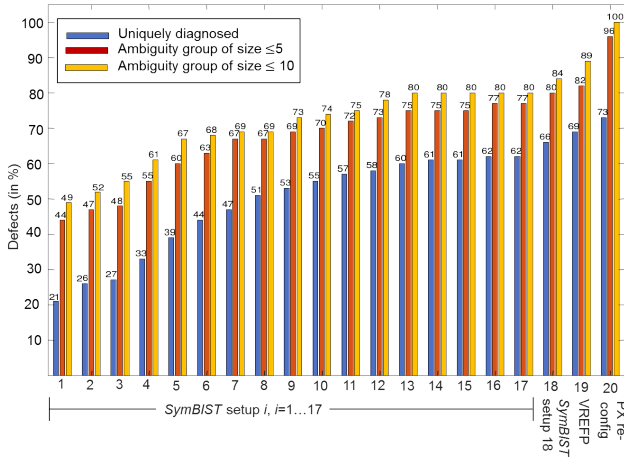


Fig. 7: Percentage of defects uniquely diagnosed and in ambiguity groups of sizes ≤ 5 and ≤ 10 .

defective cases. For each defect we show the invariance for two different *SymBIST* setups 10 and 11, which differ only in the dynamic part of the test stimulus, i.e., the input DAC sequence. The top and bottom subplots show the diagnostic measurement pattern of each defect for these two setups. In *SymBIST* setup 10, for both defects the invariance violates the lower limit of the tolerance window, thus their diagnostic measurement pattern is the same, i.e., a vector of ones, and the two defects are inseparable. With *SymBIST* setup 11, the invariant signal for defect 2 now toggles across the lower limit, whereas the invariant signal for defect 1 is still permanently violated. Thus, the two diagnostic measurement patterns are now different and the defects are successfully distinguished.

Fig. 7 shows the diagnosis results achieved with *SymBIST* following the strategy described in Section IV-G. For a given *SymBIST* setup, we show 3 bars corresponding to the percentage of uniquely diagnosed defects, i.e., ambiguity groups of size 1, the percentage of defects in ambiguity groups of size ≤ 5 , and the percentage of defects in ambiguity groups of size

≤ 10 . The inclusion of additional *SymBIST* setups stops when these three metrics saturate. As it can be seen, saturation occurs after using 17 different *SymBIST* setups. Using only the first *SymBIST* setup, 21% of the defects are uniquely diagnosed, 44% are in an ambiguity group of size ≤ 5 , and 49% are in an ambiguity group of size ≤ 10 . After using 17 different *SymBIST* setups, these metrics increase to 62%, 77%, and 80%, respectively. Fig. 8(a) sheds more light into the resultant ambiguity groups and their sizes. For example, 263 defects are uniquely diagnosed, there are $38/2 = 19$ ambiguity groups of size 2, 1 ambiguity group of size 3, etc.

It should be noted that the percentages in Fig. 7 are given in terms of detectable defects using nominal tolerance windows placed at $5 \cdot \sigma$. The first *SymBIST* setup provides the best absolute defect coverage of 57%, while the cumulative defect coverage increases to 65% considering all 17 *SymBIST* setups. Note that in practice we are interested in the likelihood-weighted (L-W) defect coverage that considers the likelihood of defect occurrence [11], which is shown to be over 86% for the complete A/M-S part of the SAR ADC IP using the first *SymBIST* setup [16], [17]. Thus, we are diagnosing over 86% of occurring defective cases considering defect likelihoods.

Next, we aimed at further improving the diagnosis result in Fig. 7 achieved with 17 *SymBIST* setups. Our first idea was to extract two diagnostic measurement patterns per defect per invariance by considering separately the two tolerance window limits. If an invariance violates permanently either the upper or the lower limit, the diagnostic measurement pattern is in both cases a vector of ones. If we consider separately the two tolerance window limits, then we can distinguish two defects where one violates the upper and the other the lower limit. This effectively doubles the size of the diagnostic measurement pattern per checker. This new *SymBIST* setup uses the same test stimulus and comparison window as *SymBIST* setup 1 and is numbered 18 in Figs. 7 and 8(b). As it can be seen, it improves the diagnosis resolution. For example, the number of uniquely diagnosed defects increases to 277 and the largest ambiguity group has now size 21.

Our second idea was to use the existing VREFP test pin, shown in the top-level architecture of Fig. 1. This pin outputs the VREF[32] reference voltage of the Reference Buffer used by the DAC during the conversion. We use the DC VREFP measurement as an analog diagnostic measurement. The nominal VREFP is 0.5V and we consider a nominal tolerance window set at $\pm 5 \cdot \sigma$. Let $VREFP(F_j)$ denote the diagnostic measurement value for defect F_j . Considering a range of 20mV centered at each $VREFP(F_j)$, a defect is detectable if its corresponding range does not overlap with the nominal tolerance window, and two defects are distinguishable if their corresponding ranges do not overlap. This test is numbered 19 in Figs. 7 and 8(c). It improves further the diagnosis resolution since the number of uniquely diagnosed defects increases to 291 and the largest ambiguity group has now size 17.

Our third idea was to use internal re-configuration. We used the topology modification approach proposed in [22]. The underlying idea is to connect Pull-Up (PU) PMOS and Pull-

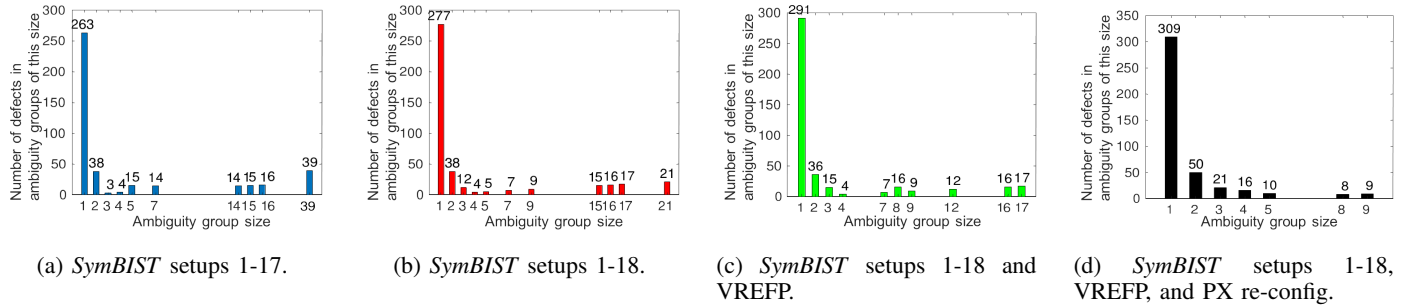


Fig. 8: Gradual diagnosis resolution improvement.

Down (PD) NMOS transistors that bring an internal node to VDD or ground, respectively. This changes the topology of the circuit and potentially can expose defects differently. First, we observed that the two largest ambiguity groups of sizes 16 and 17 in Fig. 8(c) concern defects inside the Bandgap. Thus, we apply topology modifications only in the Bandgap. More specifically, we inserted 13 PU and PD transistors enabling 13 re-configurations, where in each re-configuration only one PU or PD transistor is activated. For each re-configuration, we read out the diagnostic measurements using *SymbiST* setup 1. Since the Bandgap provides biases for all blocks inside the SAR ADC, the effect of a defect in the Bandgap can propagate to the outputs of the checkers in a complex way. This test is named “PX re-config” and is numbered 20 in Figs. 7 and 8(d). By adding this *SymbiST* variant, we were able to uniquely diagnose 73% of the defects, while the largest ambiguity group has size 9 and all but $8 + 9 = 17$ defects, i.e., 97.4% of the defects, are in ambiguity groups of size ≤ 5 , which overall is an excellent diagnosis resolution.

Finally, in total we used $L = 18 + 13 = 31$ *SymbiST* setups, thus maximum diagnosis time is $0.205 \cdot 31 = 6.35 \mu s$, plus the time of a DC measurement from the VREFP pin.

VII. CONCLUSIONS

We presented the use of *SymbiST* for analog fault diagnosis. Different *SymbiST* setups were employed to extract rich digital diagnostic measurement patterns capable of resolving defect ambiguities. *SymbiST* applied for diagnosis of an industrial SAR ADC IP resulted in high diagnosis resolution, i.e. 73% correct diagnosis of defects and over 97% defects in ambiguity groups of maximum size 5, while the largest ambiguity group has size 9. *SymbiST* offers a fast diagnosis cycle in the order of a few μs .

ACKNOWLEDGMENTS

The authors would like to acknowledge the financial support in the framework of the ANR EDITSoc project with N° ANR-17-CE24-0014-02.

REFERENCES

- [1] Q. Huang et al., “Towards smarter diagnosis: A learning-based diagnostic outcome previewer,” *ACM Transactions on Design Automation of Electronic Systems*, vol. 25, no. 5, 2020.
- [2] P. Maxwell et al., “Cell-aware diagnosis: Defective inmates exposed in their cells,” in *IEEE European Test Symposium*, 2016.
- [3] E. S. Erdogan et al., “Diagnosis of assembly failures for system-in-package RF tuners,” in *IEEE International Symposium on Circuits and Systems*, 2008, pp. 2286–2289.
- [4] N. Sen and R. Saeks, “Fault diagnosis for linear systems via multifrequency measurements,” *IEEE Transactions on Circuits and Systems*, vol. 26, no. 7, pp. 457–465, 1979.
- [5] M. Slamani and B. Kaminska, “Analog circuit fault diagnosis based on sensitivity computation and functional testing,” *IEEE Design & Test of Computers*, vol. 9, no. 1, pp. 30–39, 1992.
- [6] K. Huang et al., “Fault diagnosis of analog circuits based on machine learning,” in *Design, Automation & Test in Europe Conference*, 2010, pp. 1761–1766.
- [7] E. F. Cota et al., “A new adaptive analog test and diagnosis system,” *IEEE Transactions on Instrumentation and Measurement*, vol. 49, no. 2, pp. 223–227, 2000.
- [8] F. J. Ferguson and J. P. Shen, “A CMOS fault extractor for inductive fault analysis,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 7, no. 11, pp. 1181–1194, 1988.
- [9] S. S. Somayajula et al., “Analog fault diagnosis based on ramping power supply current signature clusters,” *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 43, no. 10, pp. 703–712, 1996.
- [10] K. Huang et al., “Diagnosis of local spot defects in analog circuits,” *IEEE Transactions on Instrumentation and Measurement*, vol. 61, no. 10, pp. 2701–2712, 2012.
- [11] S. Sunter et al., “Using mixed-signal defect simulation to close the loop between design and test,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 12, pp. 2313–2322, 2016.
- [12] V. Zivkovic and A. Schaldenbrand, “Requirements for industrial analog fault-simulator,” in *International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, 2019, pp. 61–64.
- [13] V. Gutiérrez Gil et al., “Assessing AMS-RF test quality by defect simulation,” *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 1, pp. 55–63, 2019.
- [14] T. Melis et al., “Automatic fault simulators for diagnosis of analog systems,” in *International Symposium on On-Line Testing and Robust System Design*, 2020.
- [15] S. Mir et al., “Fault-based testing and diagnosis of balanced filters,” *Analog Integrated Circuits and Signal Processing*, vol. 11, no. 1, pp. 5–19, 1996.
- [16] A. Pavlidis et al., “Symmetry-based A/M-S BIST (SymBIST): Demonstration on a SAR ADC IP,” in *Design, Automation & Test in Europe Conference*, 2020, pp. 282–285.
- [17] A. Pavlidis et al., “SymBIST: Symmetry-based analog and mixed-signal built-in self-test for functional safety,” *IEEE Transactions on Circuits and Systems - I: Regular Papers*, 2021.
- [18] F. Azais et al., “Optimizing sinusoidal histogram test for low cost ADC BIST,” *Journal of Electronic Testing: Theory and Applications*, vol. 17, no. 3-4, pp. 255–266, 2001.
- [19] R. S. Feitoza et al., “Static linearity BIST for V_{cm} -based switching SAR ADCs using a reduced-code measurement technique,” in *IEEE International New Circuits and Systems Conference*, 2020, pp. 295–298.
- [20] S. Sunter et al., “Streaming access to ADCs and DACs for mixed-signal ATPG,” *IEEE Design & Test*, vol. 33, no. 6, pp. 38–45, 2016.
- [21] B. Esen et al., “Effective DC fault models and testing approach for open defects in analog circuits,” in *IEEE International Test Conference*, 2016, Paper 3.2.
- [22] A. Coyette et al., “Automatic generation of test infrastructures for analog integrated circuits by controllability and observability co-optimization,” *Integration, the VLSI Journal*, vol. 55, pp. 393–400, 2016.