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# Analysis Of Drain Current Transient Stability Of AlGaN/GaN HEMT stressed under HTOL & HTRB, By Random Telegraph Noise And Low Frequency Noise Characterizations

J.G. Tartarin, O. Lazar, A. Rumeau, B. Franc, L. Bary, B. Lambert

*Abstract – The charges in wide bandgap Gallium Nitride (GaN) High Electron Mobility Transistors (HEMT) can be identified by means of various methods such as electrical transient and pulsed measurements, or noise spectroscopy methods, usually performed at different temperatures to extract activation energies. These traps can be passivated or activated according to electrical or thermal conditions over the lifetime. Therefore, the distinction between harmful traps (with consequences on performances) and harmless traps (without impact on electrical behaviour) must be performed. In this paper, devices stressed by HTOL (High Temperature Operating Life) are characterized by time domain electrical techniques (transient and pulsed), and with low frequency noise (LFN) experimental tools. By performing characterizations on the gate and on the drain, it is also possible to identify the drain current sensitivity to charges located in specific regions of the transistor (command or channel zones). The proposed case study discriminates the traps in the GaN buffer and at the vicinity of the AlGaN/GaN interface. The HTOL stress impacts the traps at the interface border zone in the AlGaN layer. This causes a drift in the threshold voltage  $V_{th}$ , also with a hysteresis depending on direction of increasing or decreasing sweep of the gate voltage during the characterization. Also the Schottky diode leakage current profile at the transition voltage between forward and reverse biasing mode has been analysed versus temperature. The thermal sensitivity of the drift of the threshold voltage and of the transition voltage is attributed to the kinetics of ionization and neutralization of the donor traps with the applied gate voltage. This drift of  $V_{th}$  and the action of many other traps or charges, cause the drain current to vary over time. These results are finally compared to those obtained by HTRB stress (High Temperature Reverse Bias), presenting similar degradation signatures over a longer stress period.*

## 1. GaN HEMT technologies; impact of trapping effects

Thanks to large efforts dedicated to technology development and reliability campaigns, nitride technologies have now penetrated the market; however, to the power-frequency regression limit must be added the temperature and other electrical related frontiers that define the SOA. Moreover, the High Electron Mobility Transistors (HEMT) developed with GaN technologies are sensitive to trapping effects, which consequence is a limited confidence in the stability of the quiescent point or RF dynamic signal for power amplifiers or also pulse to pulse stability in radar applications. Therefore, it is necessary to detect these traps, to locate them and to find their activation parameter as illustrated in previous studies [1]. A lack of stability of the  $I_{DS}$  current has long been attributed to traps in the channel or in the buffer layer. But an analysis of the electrical low frequency noise spectra in the 2DEG (drain current spectral density  $S_{ID}$ ) generally features almost constant noise sources in the channel before and after the application of stresses, while the gate current spectral density ( $S_{IG}$ ) evolve by several orders of magnitude (revealing an evolution of traps related to the gate region). It means that the 2DEG channel is insensitive to the stress, and that the drain current degradation mainly comes from the gated zone (vertical or lateral zones). On the other hand, despite their insensitivity with stress, LF noise contributors to the drain noise current spectra  $S_{ID}$  can reveal traps on which the drain current  $I_{DS}(time)$  depend. We analyze transient measurements on  $I_{DS}$  with LFN on the gate and drain accesses before and after HTOL stress. A focus is given on the thermal drift of the threshold voltage  $V_{th}$  and on the thermal behavior of the leakage current, as markers of the degradation kinetic. Then HTRB stress is mentioned relatively to HTOL.

## 2. AlGaN/GaN HEMT performances before and after stress.

The batch of devices under test relate to a process under development from a European company, and not to the qualified one (now commercially available) although the main technological features have remained unchanged (Figure 1). The devices feature 8 gate fingers of  $125 \mu m$  width (gate length  $0.25 \mu m$ ) grown on SiC substrate, and with 25% of Al content.

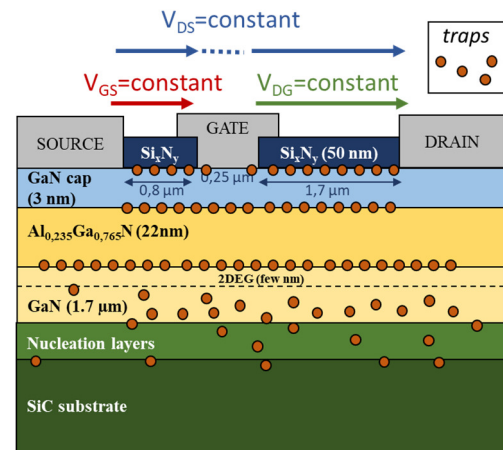


Fig. 1. Schematic of the HEMT structure under test, with DC biasing conditions to keep  $I_{DS}$  current constant vs variable electrical field ( $V_{GS}=\text{constant}$  with  $V_{DG}$  variable), or to maintain the drain-source electrical field constant vs variable electron density in the 2DEG ( $V_{DG}=\text{constant}$  with  $V_{GS}$  variable) or with a mixed biasing at constant  $V_{DS}$  (i.e. variable  $V_{DG}$  and  $V_{GS}$  – thus  $I_{DS}$ ). These biasing conditions are used for transient and Low Frequency Noise characterizations.

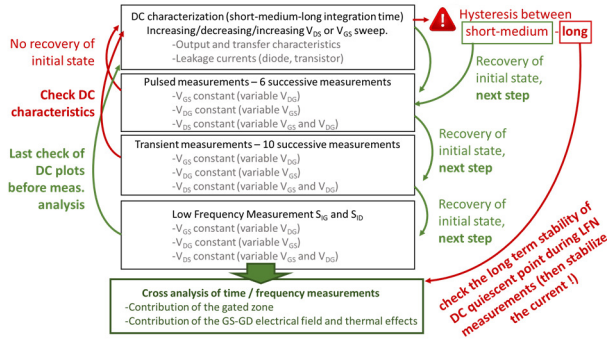


Fig. 2. Synoptic of the characterization flow for the electrical time domain measurements and for the LFN noise spectral measurements. Virgin and stressed AlGaN/GaN HEMT devices are sharing the same experimental procedure.

- A set of ten HEMT (2 virgin devices, 8 stressed devices) is considered for the HTOL (High Temperature Operating Life) stress during 105 hours, performed at 175 °C ambient temperature (320°C junction temperature) and under  $V_{DS}=30V$ ,  $I_{DS}=180mA/mm$ .

- A set of six HEMT (3 virgin devices, 3 stressed devices) is considered for the study case of HTRB (High Temperature Reverse Bias) stress during 1000 hours at a junction temperature of 200 °C (quiescent biasing point:  $V_{DS}=30 V$ ,  $V_{GS}=V_{pinchoff}$ ).

These two HTOL and HTRB stresses are key industrial items prone to reveal the epitaxial quality of materials, and so the device reliability of GaN based HEMT:

-After 105 hours of HTOL stress, measurements reveal a drop of 45% on  $I_{DSS}$  (measurement taken at  $V_{GS}=1 V$  and  $V_{DS}=8 V$ ), 130% increase on  $R_{ON}$ , 5% to 15% increase on  $V_{th}$  and one decade degradation on  $I_{GS}$ .

- After 1000 hours of HTRB stress, aged devices feature a mean degradation of 15% on  $I_{DSS}$  (measurement still taken at  $V_{GS}=1 V$  and  $V_{DS}=8 V$ ), 40% increase on  $R_{ON}$ , 7% increase on  $V_{th}$  and no degradation on  $I_{GS}$  is evidenced for half of the stressed devices (degradation by one decade for the second half).

In the next characterization section, as the HTRB stress provokes less degradation on  $I_{DSS}$  and  $R_{ON}$  after 1000 hours of stress than those observed after HTOL over a shorter stress period, case study is focused on this later stress with DC and transient electrical characterization, and with low frequency noise measurements. However, comparable variations are observed on the threshold voltage  $V_{th}$  and on the leakage current during the two stress campaigns. An analysis is carried out at the end of the *Discussion* section, regarding behavior of devices subjected to HTOL stress and those having undergone HTRB stress. The synoptic of the characterization plan, as described in Figure 2, concerns:

- DC characteristics performed with increasing/decreasing  $V_{DS}$  and  $V_{GS}$  sweeps. These are realized for different integration time conditions to evidence some trapping effects, even at this stage of characterization. Measurements are performed at various temperatures ranging from 80 K to 400 K by step of 25 K.

- Pulsed  $V_{GS}$  characterizations are performed for various  $V_{DS}$ , to evaluate the lag effects, and to sense the impact of traps in the gate-source and gate-drain region (interface or bulk).

- Transient measurements are performed for various biasing conditions from pinched channel (off) to partially or totally open channel (on), to track the evolution of  $I_{DS}$  versus time.

- Low Frequency Noise (LFN) spectroscopy on gate and drain current has been performed at ambient temperature, for various biasing conditions as explained below. Traps ranging from 1  $\mu s$  to 1 s can be revealed on both the drain and gate currents, in accordance with the spectral range of the experimental bench.

### 3. Electrical and Noise characterization.

Multiple measurements are carried out for a given quiescent point to highlight a possible impact of the characterization setup conditions on the measured data (impact of the increasing or decreasing sweep of the control voltage, of the memory effects and thermal effects, of the recoverable or permanent degradation even during the characterization). For pulsed electrical and for low frequency noise measurements, biasing conditions have been selected in the saturated zone (as depicted in Fig. 1) to:

-maintain the current density constant ( $V_{GS}$  constant) while varying the electrical field between drain and gate  $V_{DG}$ , to reveal the influence of this later zone.

-control the current density at variable  $V_{GS}$ , while keeping constant the electrical field in the channel through drain-gate voltage  $V_{DG}$ , to evidence gate related defects on the 2DEG density of electrons.

-perform a mixed characterization mode on the quiescent biasing conditions to corroborate the hypothesis rising from the two previous experiments.

The presence of deep-levels in various locations of the HEMT, as depicted in Figure 1, degrades the RF dynamic performances and the reliability of a device. The previous biasing conditions are used to refine the location of the traps.

#### 3.1. Pulsed I-V characterizations

All virgin and stressed devices have been extensively characterized. The difference on pulsed output characteristics in

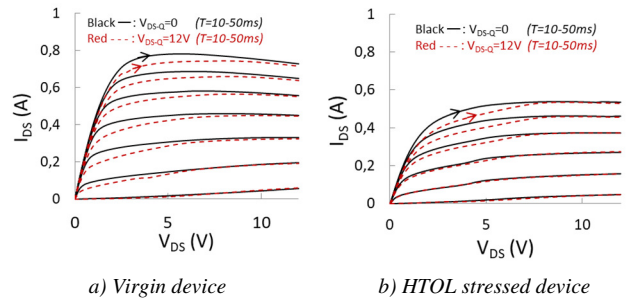


Fig. 3. Pulsed output characteristics for virgin device a) and HTOL stressed device b). Pulse width is 500  $\mu s$ , for duty cycle varying from 1 % to 5 % (i.e. period T of 10 to 50 ms). Arrows indicate the sweep direction of  $V_{DS}$ , for two quiescent  $V_{DS-Q}=0 V$  (black plot) and  $V_{DS-Q}=12 V$  (red dotted plot), while  $V_{GS-Q}=0 V$ .

Figure 3 is revealed for various quiescent conditions of  $V_{DS-Q}$ . Similar plots have largely been reported in the literature related to GaN HEMT structures, as in [2], where (co)doping of the buffer is investigated as the cause for such signature. To resume this variation in  $I_{DS}$  near the knee region (saturated / ohmic region), neither the period nor the width of the pulse impact significantly the output characteristic of the devices. Also, measurement performed with increasing or decreasing  $V_{DS}$  or  $V_{GS}$  sweeps feature almost identical plots at ambient temperature. Only the initial quiescent condition of  $V_{DS-Q}$  (0 V or 12 V) causes this variation in the  $I_{DS}$ - $V_{DS}$  plots, which results in a lower  $I_{DS}$  current when quiescent biasing  $V_{DS-Q} = 12$  V. As the isothermal conditions are respected ( $I_{DS}$  at higher dissipated power, i.e.  $V_{GS} = 0$  V and  $V_{DS} = 12$  V, are almost the same for the two  $V_{DS-Q}$  conditions), this difference cannot be attributed to thermal effects, but more likely to the quiescent state of the electrical field between drain and source (i.e.  $V_{DS-Q}$ ). The difference between a virgin device and a representative HTOL stressed device is depicted in Figure 3. Gate lag measurements have been performed on the virgin devices with figure of merit as low as  $GL_{\%}=3\%$  as defined by (1), using the output characteristic in class A biasing at maximum voltage and current swing. The measurement of the pulsed output characteristics are performed at quiescent points of ( $V_{GS-Q}=0V$ ;  $V_{DS-Q}=0V$ ) and under pinched conditions ( $V_{GS-Q}<-7V$ ;  $V_{DS-Q}=0V$ ).

$$GL_{\%} = 100 \times \frac{\Delta I_{DS}(V_{GS-Q} < V_{th} \& V_{DS-Q} = 0V) - \Delta I_{DS}(V_{GS-Q} = 0V \& V_{DS-Q} = 0V)}{\Delta I_{DS}(V_{GS-Q} = 0V \& V_{DS-Q} = 0V)} \quad (1)$$

$$DL_{\%} = 100 \times \frac{\Delta I_{DS}(V_{GS-Q} < V_{th} \& V_{DS-Q} \neq 0V) - \Delta I_{DS}(V_{GS-Q} = 0V \& V_{DS-Q} = 0V)}{\Delta I_{DS}(V_{GS-Q} = 0V \& V_{DS-Q} = 0V)} \quad (2)$$

However, the gate lag degrades by only  $\Delta(GL_{\%})=3\%$  after the HTOL stress. The gate lag remains constant during HTRB stress for half of the devices, and degrades by  $\Delta(GL_{\%})=2\%$  for the other half of samples under test. Drain lag is a combined response of the quiescent gate and drain voltage conditions, but with a higher drain voltage impact on the 2DEG density of electrons (2). It is measured at  $DL_{\%} = 7\%$  for virgin devices, and  $DL_{\%} = 12\%$  for HTOL stressed devices.

When considering  $I_{DS}$  plots by changing  $V_{GS}$  quiescent point turned on from 0 V to a lower value as illustrated in Figure 4, the effect of traps is clearly highlighted even on a virgin device for various  $V_{DS}$  voltages on slow drain current transients. This capture and emission process features time constant decreasing when  $V_{DS}$  (temperature) increases.  $V_{GS}$  is also related to the thermal time constant dependence of the traps through  $I_{DS}$  (by  $V_{DG} \times I_{DS}$ ), which are not easy to discriminate from pure self-heating effects. However, the trapping effect dependence to the temperature is not considered in this paper. Last, measurements performed at various final quiescent points  $V_{GS}$  (same profiles as for Figure 4) reveal that the variations of  $I_{DS}$  are related to  $V_{GS}$  for the transient variation in the magnitude of  $I_{DS}$ , and then to  $V_{DG}$  ( $V_{DG}=V_{DS}-V_{GS}$ ) for the steady state of  $I_{DS}$  as expected. Such behavior has been simulated by TCAD models; it is attributed to traps in the buffer and possibly in the AlGaN barrier [3][4]. This

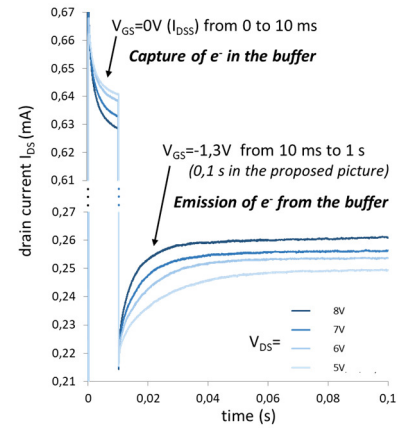


Fig. 4. Transient profile of pulsed plots of  $I_{DS}$  versus time for a virgin device. AlGaN/GaN HEMT is turned on from pinched 2DEG to  $V_{GS} = 0$  V ( $I_{DSS}$ ) at  $t = 0$  till  $t = 10$  ms, then the device is biased at  $V_{GS} = -1.3$  V, for various  $V_{DS} = 5, 6, 7, 8$  V.

is consistent with the activation of more ionized or neutralized acceptor traps with the electrical field.

### 3.2. Time domain characterization

A set of measurements is performed at different initial conditions over the batch of virgin and aged devices.  $V_{GS}$  is triggered from pinched to open channel conditions (-7 V to 0 V), or  $V_{DS}$  is triggered from 0 V to [4 V, 8 V, 12 V] (or using more complex profiles) [5]. It is evidenced that:

- not surprisingly, virgin devices are more sensitive to thermal effects at the early establishment of  $V_{DS}$ , according to the more elevated DC power than that of stressed devices.
- during successive measurements, traps are activated and the  $I_{DS}$  characteristic is lowered (up to 1 second of pulse width). Then the  $I_{DS}$  plot is stabilized after 3 successive measurements (10<sup>th</sup> measurement is compared with the 1<sup>st</sup> one on Figure 5). The initial plot is recovered when applying positive  $V_{GS}$  voltage or after 1 minute with no biasing. Again the role of the gate biasing on the recovery of  $I_{DS}$  is evidenced.
- HTOL stress makes  $I_{DSS}$  (at  $V_{GS} = 0$  V) decrease as a possible consequence of the threshold voltage  $V_{th}$  increase. Therefore we have focused on the threshold voltage variations for different

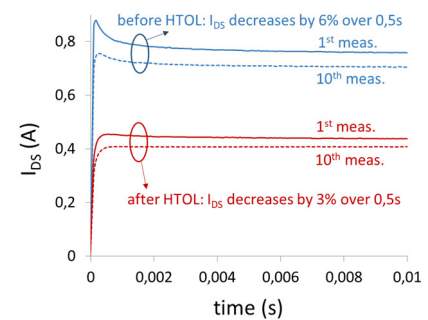


Fig. 5. Transient evolution of  $I_{DS}$  over 10 successive measurements before (blue plots) and after (red plots) the application of HTOL stress.  $V_{GS}=0V$  (open channel condition) while  $V_{DS}$  is triggered from 0V to 12V at time  $t=0$ .

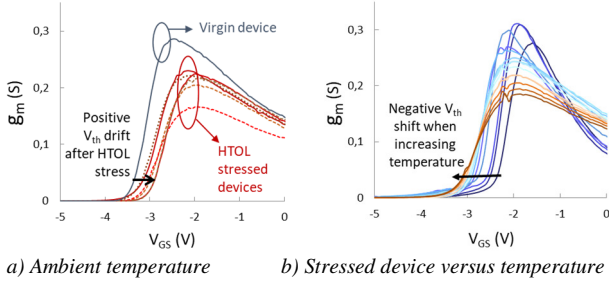


Fig. 6. Pulsed transconductance gain  $g_m$  versus  $V_{GS}$ . Quiescent conditions are ( $V_{GS-Q}=0V$ ;  $V_{DS-Q}=0V$ ) and measurement is plotted for  $V_{DS-meas.}=8V$ . a) Virgin and HTOL stressed devices at ambient temperature featuring positive  $V_{th}$  drift. b) HTOL stressed device for temperature ranging from 80 K (dark blue plot) to 400 K (orange plot) by step of 25 K, from which the negative bias temperature instability (NBTI) of  $V_{th}$  is extracted.

temperatures. The analytical expression of  $V_{th}$  is given in (3):

$$V_{th} = \frac{\phi_B}{e} - \frac{d\sigma}{e} - \frac{\Delta E_C}{e} + \frac{E_{f0}}{e} - \frac{edN_{St}}{\varepsilon} - \frac{eN_b}{C_b} \quad (3)$$

where  $\phi_B$ ,  $d$ ,  $\sigma$ ,  $\Delta E_C$ ,  $E_{f0}$  are the height of the Schottky barrier, the thickness of the AlGaIn barrier, the total polarization charge at the barrier-AlGaIn/GaN interface, the discontinuity of the conduction band at the AlGaIn/GaN heterojunction, the difference between the intrinsic Fermi level and the conduction band edge of the GaN channel. The last two terms in (3) describe the effects of the interface or surface traps ( $N_{St}$  is the net-charged interface or surface traps per unit area) and bulk traps in the buffer ( $N_b$  is the effective net-charged buffer traps per unit area) [6]. Finally,  $\varepsilon$  and  $C_b$  are respectively the permittivity of the AlGaIn layer and the effective buffer-to-channel capacitance per unit area respectively. As most of the parameters from equation (3) should be kept unchanged ( $\Phi_B$ ,  $\Delta E_C$ ,  $E_{f0}$  are not stress dependent parameters), only the modification of interface polarization charges  $\sigma$  (spontaneous and piezoelectric) or even buffer charges or surface/interface traps are likely to modify  $V_{th}$ .

Transconductance gain  $g_m$  is extracted from pulsed transfer characteristics  $I_{DS}-V_{GS}$ . Figure 6.a compares a virgin device with an HTOL stressed HEMT. A shift in the threshold voltage is

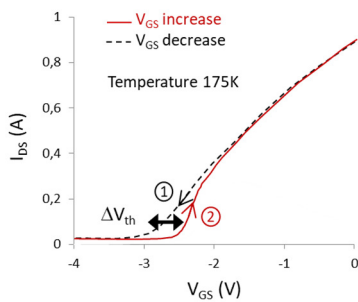


Fig. 7. Pulsed  $I_{DS}-V_{GS}$  transfer characteristic for an HTOL aged device measured at 175 K by decreasing ①, or by increasing ②  $V_{GS}$  sweep. Biasing conditions are ( $V_{GS-Q}=0V$ ;  $V_{DS-Q}=0V$ ) and measurement is plotted at  $V_{DS-meas.}=8V$ .

evidenced as the signature of the stress endurance period. The fixed defects in the GaN, AlGaIn or GaN cap layers can act like traps. According to the density of defects, this could lead to a drift of the intrinsic potential and an energy band bowing, thus a  $V_{th}$  drift. Therefore, characterization at various temperatures has been performed from 80 K to 350 K. The negative bias temperature instability (NBTI) is noticeable through the thermal drift in the threshold voltage as evidenced in Figure 6.b. This NBTI has been previously reported, and it was associated with nitrogen vacancies near the AlGaIn/GaN [7] interface or at the AlGaIn surface [8]. However, an hysteresis is experienced on the  $I_{GS}-V_{GS}$  plots (and thus in the drift magnitude of  $V_{th}$ ), according to the increasing or decreasing sweep of  $V_{GS}$ , as depicted in Figure 7. The higher drift on  $V_{th}$  is measured for increasing  $V_{GS}$  sweep ②, with a changing slope in  $I_{DS}$  near the pinch-off zone (and so visible on the enhancement in  $g_m$  near  $V_{th}$  in figure 6b), and for the lowest temperatures. This is the consequence of a fast increase of  $I_{DS}$  when the channel starts to be filled with electrons. This low temperature change in the slope is no longer activated from a specific  $V_{DS}$  voltage (around 10V), or when decreasing the  $V_{GS}$  sweep ①. The dynamic activation of traps in this particular zone stand as a probable hypothesis, as discussed in the last section, and according to equation (3).

These  $V_{th}$  drifts with temperature are plotted for the virgin transistor and for a representative HTOL stressed transistor in Figure 8. When we perform a decreasing  $V_{GS}$  sweep from 3 V to -6 V (the  $V_{GS}$  range is reduced to [-5 V; 0 V] in Figure 6), this accentuation of  $g_m$  no longer occurs, and the  $V_{th}$  drift with temperature is lowered. The variation of  $V_{th}$  is more pronounced for the stressed device when  $V_{GS}$  increases than when  $V_{GS}$  decreases, whereas no noticeable change is experienced on the virgin device. It seems that traps are activated/passivated near the pinching region by increasing  $V_{GS}$ , whereas these traps do not change of state by decreasing  $V_{GS}$ .

To assess such trap evolution according to the direction of sweep on  $V_{GS}$ , DC measurements of the gate leakage current have been performed at various temperatures as depicted in Figure 9 (diode mode, open drain). First, the inversion point, i.e. the gate voltage  $V_{inv}$  when the sign of the current  $I_{GS}$  changes (i.e. at the forward-reverse transition voltage), varies according

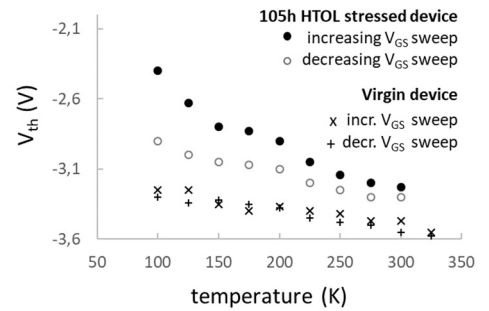


Fig. 8. Negative drift of the threshold voltage  $V_{th}$  with temperature (NBTI).  $V_{th}$  is extracted from transconductance gain  $g_m$ , i.e. the derivative slope of  $I_{DS}$  versus  $V_{GS}$  in Figure 6, and for  $V_{GS}$  increasing/decreasing voltage sweeping (HP4156C signal analyzer).

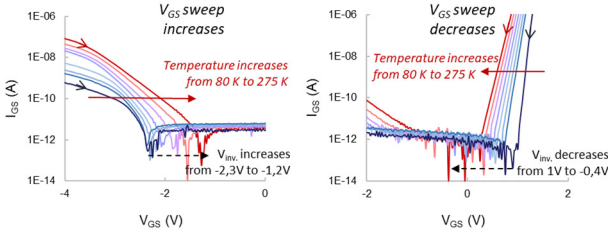


Fig. 9. Thermal dependence of the leakage current in diode mode (DC measurements). Arrows on the plots indicate the increasing (left) or the decreasing (right) sweeping direction for  $V_{GS}$ . The drift of the inversion voltage  $V_{inv}$  (i.e. when the leakage current is null if not using a logarithmic scale) is identified for each sweep direction.

to the increase or the decrease in the  $V_{GS}$  sweep.  $V_{inv}$  increases by 1.2 V (Figure 9 left) or decreases by 1.4 V (Figure 9 right) for the specific temperature range. This behavior is revealed in diode configuration (open/shorted drain) and in transistor mode.

The inversion voltage  $V_{inv}$  can be an original marker revealing the change in the charges density under the gate. The latter is possibly correlated to the weaker drift of  $V_{th}$  ( $\Delta V_{th} = 0.8$  V for the increase of  $V_{GS}$  sweep).

### 3.3. Low Frequency Noise spectral measurements

Gate and Drain current low frequency noise (LFN) characterization (resp. through current spectral densities  $S_{IG}$  and  $S_{ID}$ ) have been performed according to biasing conditions exposed in Figure 1. From the LFN spectra on the drain access, numerous generation-recombination (GR) centers are identified as already published in numerous articles (see for instance [5][9][10]), but no major difference in these spectra allows any distinction between aged or virgin devices. Figure 10 represents the drain current spectral density for a virgin device and for a stressed device; the spectra are almost identical for these devices within the explored  $V_{GS}$  and  $V_{DS}$  biasing conditions (the saturated current  $I_{DSS}$  cannot be reached due to setup limitation). For comparison between devices, these spectra are usually normalized as  $S_{ID}/I_D$  (under saturated biasing condition) to get rid of the drain current level, and when considering the  $1/f$  flicker noise source. Many generation-recombination centers can be noticed in the spectra from Figure 10, but this representation is still valid at a frequency of 1 kHz as proposed in Figure 11. The spectral density  $S_{ID}/I_D$  on the drain access

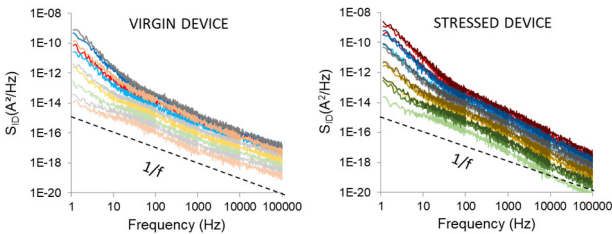


Fig. 10. LFN drain current spectral density  $S_{ID}$  in the saturated biasing region for various  $V_{GS}$  and  $V_{DS}$  voltage biasing ( $V_{DS}$  ranges from 5 to 8V,  $V_{GS}$  ranges from -0.7 to -2V with  $I_{DS} < 100$  mA due to setup limitation).

measured at 1 kHz is plotted versus the three different voltage configurations as depicted in Figure 1.  $\Delta S_{ID}/I_D$  versus  $\Delta$ voltage data in Figure 11 are relative to a reference value  $(S_{ID}/I_D)_{ref}$  measured at a reference quiescent point of  $V_{GS} = -2$  V and  $V_{DS} = 7$  V (thus  $V_{DG} = 9$  V). The three biasing conditions are plotted versus  $\Delta$ voltage respectively expressed by  $\Delta$ voltage =  $\Delta V_{DG} + \Delta V_{SG}$  for constant  $V_{DS} = 7$  V (blue symbols), or  $\Delta$ voltage =  $\Delta V_{DG}$  for constant  $V_{GS} = -2$  V (red symbols), and  $\Delta$ voltage =  $\Delta V_{SG}$  for constant  $V_{DG} = 9$  V (green symbols). These three sets of measurements at constant  $V_{DS}$ ,  $V_{GS}$  or  $V_{DG}$  reveal a linear trend of the normalized drain current spectral density. Since the normalization  $S_{ID}/I_D$  gets rid of the value of  $I_{DS}$  at these different DC biasing conditions, this linear trend reveals the relation between the defects density that increases with the extension of the electrical field (between Gate and Source or Gate and Drain accesses). This also explains the smaller variation under constant  $V_{DG}$ , since only  $V_{GS}$  can vary over a small range of values. As virgin and stressed devices share the same LFN characteristics on the normalized drain spectral density versus these various biasing voltages in Figure 11, this reveals that the channel is not altered by the stress condition.

LFN characterizations on the gate access has been performed in diode mode (open and shorted drain), and in transistor saturated mode. Measurements are performed with custom LFN setup which allows very low current spectral densities down to  $10^{-24}$  A<sup>2</sup>/Hz for the lower range of leakage current. Figure 12 represents the gate current spectral density  $S_{IG}$ , and a normalized representation  $S_{IG}/I_G$  versus frequency. The normalized  $S_{IG}/I_G$  spectra for the virgin device remains almost constant for all forward and reverse biasing conditions, with less than an order of magnitude of variation for  $V_{GS}$  in the range of [-9 V; 1.2 V] in spite of different conduction modes for the reverse and forward leakage current. This variation of the normalized gate current spectral density is in the range of three orders of magnitude for HTOL stressed devices as depicted in Figure 13. It can also be noticed the presence of low frequency (below 10 Hz) and medium frequencies (above 1 kHz) GR centers as evidenced for aged devices in diode configuration in Figure 13. The normalized  $S_{IG}/I_G$  LFN spectra is higher in transistor biasing condition than in diode mode since the activation of the electrical field  $V_{DG}$  in transistor mode also

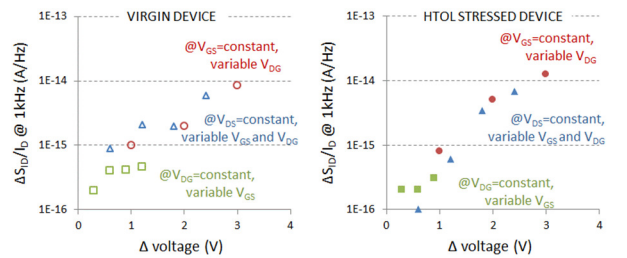


Fig. 11.  $\Delta S_{ID}/I_D$  relative normalized LFN drain current spectral density at 1 kHz versus relative  $\Delta$ voltage. The initial  $S_{ID}/I_D$  measurements from Figure 10 are performed in the saturated biasing region, under different  $V_{GS}$ ,  $V_{DG}$  or  $V_{DS}$  biasing voltage. Empty symbols are for a Virgin device (left). Filled symbols are for a representative device after HTOL stress (right).

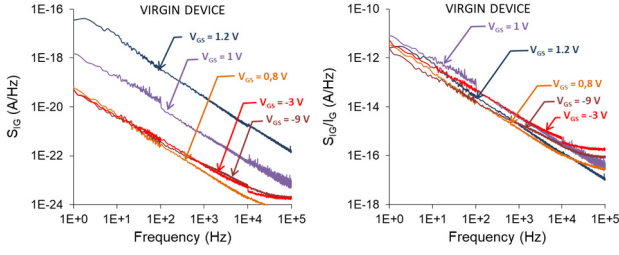


Fig. 12. LFN gate current spectral density in diode mode for a virgin device (open drain). The diode is measured in forward and reverse biasing conditions (-9V, -3V, 0.8V, 1V, 1.2V). The left caption represents  $S_{IG}$ , and the right caption represents the normalized  $S_{IG}/I_G^\alpha$  (power factor for  $I_G$  is taken at  $\alpha=1$ , but it can be found at different values, see for instance [11]).

changes the leakage path; these spectra are constituted by a higher number of GR centers (continuum) as the space charge region extension increases with  $V_{DS}$  in this transistor configuration (cf. Figure 11). Moreover, transient measurements with an oscilloscope have been performed on  $I_{GS}$  (with a current probe) to discriminate Random Telegraph Noise (RTN) centers from the numerous GR centers in transistor saturated mode (RTN and GR centers share the same Lorentzian signature in their spectral representation). RTN centers are identified on virgin and stressed devices (Figure 14). First, it can be stated that the GR centers measured in transistor saturated mode on aged device from Figure 13, between 1 Hz and 10 Hz, are not associated with RTN centers. Surprisingly, a delimitation zone can be easily drawn between the virgin device and the HTOL stressed device. For this study, we only focus on the determination of distinct signatures before and after HTOL stress, with higher corner frequencies (so shorter trapping constants) for aged devices. This means that trapping centers have been modified or created during the HTOL stress. These traps, as revealed by  $S_{IG}$ , are located in the vertically stacked layers below the gate. The action of traps under the gate have already been identified [12], with correlated effects on  $I_{GS}$  and  $I_{DS}$  currents, and also in connection with the inversion voltage on the  $I_{GS}$ - $V_{GS}$  plots [13].

#### 4. Discussion.

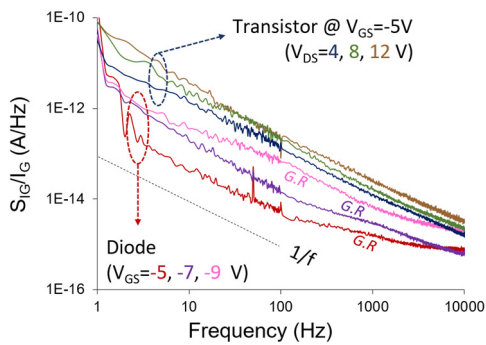


Fig. 13. Normalized LFN spectral density  $S_{IG}/I_G$  for a HTOL stressed device (diode and transistor mode at different  $V_{GS}$  and  $V_{DS}$  quiescent voltages).

From the cross-analysis between electrical and LF noise experiments, we now propose an interpretation of the variations of  $V_{th}$ , and thus of the subsequent current drift.

Firstly, as evidenced by  $S_{ID}$  and  $S_{IG}$  LFN measurements, various types of traps are revealed through GR or RTN centers. Some of them are not bind to the HTOL stress as they remain almost constant regardless the aged or virgin devices under test (traps extracted from  $S_{ID}$  in the 2DEG channel activated with the space charged region extension). From TCAD simulations, donor buffer traps can explain the linear dependence of  $S_{ID}$  with the space charged region extension.

Secondly, trap density involved in the characterization of the drain current spectral density  $S_{ID}$  (related to  $I_{DS}$ ) is largely higher than that involved in  $I_{GS}$  LFN spectra. Donor buffer traps evoked previously for  $S_{ID}$  could probably also explain some of the thermal drift on  $V_{th}$  for decreasing  $V_{GS}$  sweep. However, these bulk (donor) charges cannot explain the impact of the  $V_{GS}$  increasing/decreasing sweep direction at low temperature as discussed in section 3.1 and 3.2, and as depicted in Figure 7. RTN plots depicted in Figure 14 clearly evidence a difference between stressed and virgin devices, and traps positioned on the leakage path are proposed to explain the  $V_{th}$  shift from this hysteresis in  $I_{DS}$ - $V_{GS}$  plot according to the sweeping direction of  $V_{GS}$ .

Figure 15 presents a drawing of the energy band diagram where only traps at the vicinity of the AlGaIn/GaN interface are depicted. Donor traps with energy levels  $E_{T-donor}$  close to the conduction band  $E_C$  are considered to be ionized for strongly negative  $V_{GS}$  values (i.e. situation when  $V_{GS}$  sweep increases from -6 to +3V). These donor traps are considered to be neutral if filled with an electron, for  $V_{GS}$  values when the fermi level  $E_{Fi}$  is above the energy level of the trap  $E_{T-donor}$  (i.e. situation when  $V_{GS}$  sweep decreases from +3V to -6V). In Figure 15, donors are located at the AlGaIn/GaN interface or in a near border zone in the AlGaIn layer to illustrate this hysteresis mechanism.

① Case when decreasing  $V_{GS}$  from +3V to -6V (reduced to [-4V; 0V] in Figure 7): donors remain passivated till the 2DEG is fully depleted. Then  $E_{Fi}$  shifts below  $E_{T-donor}$  level, and donors start to get ionized. This ionization of the donors has no impact on the control of the depleted 2DEG when  $V_{GS}$  still decreases. So  $V_{th-decr.}$  is not modified during  $V_{GS}$  sweep.

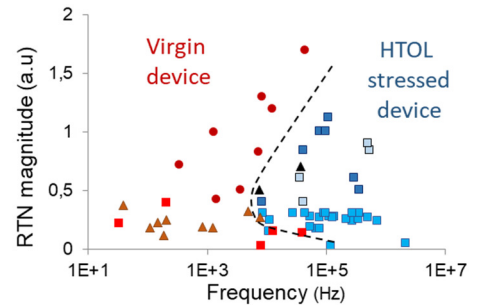


Fig. 14. Random Telegraph Noise (RTN) centers extracted from  $I_{GS}$  for various reverse and forward diode biasing in the range of (-11V, +2V) on virgin devices (red plots, lower frequency centers) and on HTOL stressed device (blue plots, higher frequency centers).

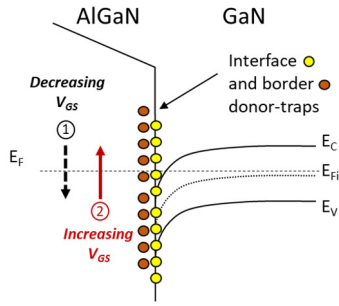


Fig. 15. Energy band diagram near the AlGaIn/GaN interface.  $E_F$  relative level to  $E_C$ ,  $E_V$  and  $E_{Fi}$  moves with decreasing / increasing  $V_{GS}$  voltage. Border donor-traps are passivated when  $V_{GS}$  decreases ① (leading to a stable  $V_{th-decr}$ ). Border donor-traps are evolving near the  $V_{th-incr}$  pinch-off voltage when  $V_{GS}$  increases ② as depicted in Figure 7.

② Case when increasing  $V_{GS}$  from -6V to +3V: border donors near the interface are ionized ( $N_D^+$ ) under strongly negative  $V_{GS}$ . These positive charges act as an internal generator which field is opposite to the applied voltage  $V_{GS}$ , and then  $V_{th-incr.} > V_{th-decr.}$  (thus  $n_{i-incr.} < n_{i-decr.}$ ). This situation lasts till  $V_{GS}$  increases to  $V_{th-incr.}$ , and when the energy level of the donors equals the fermi level ( $E_{T-donor}=E_{Fi}$ ). Then, the 2DEG starts to be filled with electrons, and ionized donor-traps recombine with few of these electrons from the 2DEG (this negligible quantity of derived electrons do not reduce  $n_i$ ). The donor traps are then neutral, and the internal generator disappears;  $V_{th}$  goes to a lower value (as for the decreasing sweep,  $V_{th-decr.}$ ) and the electron density increases to its value such as with neutral donor case.

Of course, the explanation for the BTI as illustrated in Figure 8 involves other traps, but the negative drift magnitude with temperature is almost the same for virgin and HTOL stressed devices (in exception of increasing  $V_{GS}$  sweep for aged devices as previously discussed). Buffer traps are then probably also under concern, as Figure 14 suggests through the large number of defects revealed by RTN characterization.

Last, all the discussed characteristics for HTOL stressed devices have also been evidenced for HTRB stressed devices, in a lesser proportion in spite of a longer stress period. It is assumed that the same degradation process rises from these two stresses, but it is accelerated under HTOL conditions.

## 5. Conclusions.

The impact of the dynamic or static charges in the gated zone of AlGaIn/GaN HEMT is evidenced both on the drain current and on the gate leakage current, based on a wide set of experimental setups concerning electrical pulsed and transient measurements, as well as RTN and LFN noise characterizations.

It has been evidenced the threshold voltage dependence with temperature changes after HTOL stress, and that an hysteresis is revealed according to the increasing or decreasing  $V_{GS}$  sweep. This hysteresis degrades when temperature decreases (with variation of  $\Delta V_{th}=0.1$  V at 200 K, and up to  $\Delta V_{th}=0.5$  V at 100 K), and it can be integrated in a compact

model to account for its effect in a power amplifier where the dynamic swing of  $V_{GS}$  could affect the circuit performance.

From diode characterization versus temperature, the transition zone between forward and reverse biasing is also  $V_{GS}$  sweep dependent, and is sensed through the shift in the inversion voltage  $V_{inv}$ .

Charges responsible for such  $V_{th}$  and  $V_{inv}$  dependency with  $V_{GS}$  sweep are investigated by noise spectral characterizations. Low Frequency Noise measurements have revealed that the defects in the 2DEG (through drain current spectral density measurements  $S_{ID}$ ) do not evolve during stress, even if traps are evidenced, which feature a dependence upon the lateral electrical field between gate-drain or gate-source in a lesser way. From low frequency gate current spectral densities  $S_{IG}$ , the normalization versus the leakage current reveals the impact of the stress on the charges beneath the gate. Also random telegraph noise on the gate leakage current (RTN from time domain characterization) evidences specific signatures before and after the application of the stress: aged devices feature traps with shorter time constants, and could possibly be involved in the  $V_{th}$  and  $V_{inv}$  hysteresis signatures. An explanation invoking donors under the gate near the AlGaIn/GaN interface, allows a coherent explanation of the measurements.

Finally, similar electro-thermal and low frequency noise signatures for HTOL and HTRB stresses suggest the same origin of the defects, but with accelerated degradation for HTOL stress during a shorter period than for HTRB.

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