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A Temperature-Aware Framework on g_m/I_D -Based Methodology Using 180 nm SOI From $-40\text{ }^\circ\text{C}$ to $200\text{ }^\circ\text{C}$

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ABSTRACT The advent of the Internet-of-Things brings new challenges in circuit design. The presence of circuits and sensors in harsh environments brought the need for methodologies that account for them. Since the beginning of the transistors, the temperature is known for having a significant impact on performance, and even though very low temperature sensitivity circuits have been proposed, no general methodology for designing them exists. This paper proposes a g_m over I_D technique for designing temperature-aware circuits that can be used either on measurement data, analytically, or based on simulation models. This model is validated using measurements up to 200°C of X-FAB XT018 transistors and later with a circuit design example.

INDEX TERMS Temperature-aware, g_m/I_D , SOI, harsh-environments, smart-vehicles.

I. INTRODUCTION

WITH the challenge of connecting people and circuits, Internet-of-Things (IoT) introduces new power decisions in autonomous electronics in consumer products. The challenge of connecting people with different objects has been extremely rapid in recent years. Today, electric vehicles represent new investments in sensors and integrated circuits that, between 2017 and 2019, accounted for a 1.3 billion dollars worldwide investment with projections of growth in the next coming years. [1]. Vehicles' IoT circuits must efficiently sense and communicate with other nearby devices, considering the working environment [2]. For obvious reasons, the design and the specification of vehicles' IoT circuits are regulated by many strict security and safety standards. The temperature range is arguably the most demanding environmental challenge for electronics in the automotive industry [3].

Circuit design for harsh environments places new constraints on system design, representing a challenge for low-cost, reliable devices [4]. Even though in a late 90s

report, the U.S. National Research Council pointed out the possibility of Si materials to operate up to $300\text{ }^\circ\text{C}$ [5], the usual approach for designing small temperature sensitivity circuits relies on the use of wide bandgap semiconductor materials such as GaN [6] or SiC [7]. Even though those materials present intrinsically smaller parameters degradation over temperature [6], [7], they come with a higher production cost, not enabling the integration of digital circuits on-chip, an essential feature of smart sensing.

Being a standard in high-end automotive applications, the SOI 180 nm process technology from the X-FAB Silicon Foundries is ideal for electronics to operate near-combustion engine compartments or electric engine housings with a temperature range from $-40\text{ }^\circ\text{C}$ up to $175\text{ }^\circ\text{C}$ [8], low-power digital applications in communications, consumers, and industrial markets [9]. Silicon-based SOI technologies, as X-FAB, are indispensable for high temperature operations due to the reduced current leakage and have dominated the consumer market, having affordable production costs.

Literature has presented design solutions to address temperature-aware circuits in Si technologies. In [10], a current reference is proposed by combining a beta-multiplier current source with an altered version of a Nagata current mirror and a high-temperature coefficient resistor to design a circuit with a 200 ppm/°C temperature coefficient. Toledo *et al.* [11] have proposed a zero temperature coefficient bias point (ZTC) for the gate transconductance based on the UICM model and explored this point to design a 34 ppm/°C single-ended Gm closed-loop resistor. Another approach showed in [12], where a closed-loop digital controller is proposed to control the non-linearity error of a temperature sensor.

Even though recent papers presented very low temperature sensitivity, the presented methods are mostly dependent on the ZTC operation point of a unique transistor or additional control circuitry. This design choice intrinsically increases consumption and production cost which could be prohibitive in new low-power IoT devices. With the increasing need for temperature-aware designs, it is indispensable to have a common framework for developing temperature-aware circuits.

This work proposes a temperature analysis using the g_m/I_D methodology. By introducing the concept of temperature normalized g_m/I_D parameters. The presented ZTC bias points have no significant influence on mobility temperature dependency and are still compatible with the g_m/I_D methodology. The analytical development is done using the UICM model and validated by simulations on BSIM v4.6, factory-validated from -40 °C to 175 °C, and measurement data for higher temperatures up to 200 °C. Moreover, a global framework in temperature-aware methodology and a design example are presented.

The paper is organized as follows: Section II explores the state-of-the-art ZTC points and discusses their trade-offs. In Section III, the temperature normalized g_m/I_D method is presented and validated with simulations and measurement data. An example circuit is presented in Section IV. Finally, Section V concludes and summarizes this brief.

II. ZERO TEMPERATURE COEFFICIENTS (ZTC) POINT

A. TEMPERATURE EFFECTS ON MOS TRANSISTORS

Most temperature-aware circuit designs rely on ZTC bias conditions, i.e., points where the value of a given parameter remains almost independent of temperature. The known ZTC bias conditions are based on the threshold voltage and mobility temperature dependency [11], [13]. For this reason, they are dependent on the temperature modeling of those quantities, which are not necessarily accurate in the circuit working conditions [14].

1) THRESHOLD VOLTAGE TEMPERATURE EFFECTS

Even though the threshold voltage (V_{th}) has a rather blurry definition at the latest MOSFET models [15], [16], it is a key parameter for circuit design. In this paper, the V_{th} definition will be taken as the gate voltage that equalizes

drift and diffusion current components [17]. The threshold voltage has a well-defined temperature dependency based on the materials and transistor properties given by [18]:

$$V_{th}(T) = V_{th0} - \alpha_{th} \cdot T, \quad (1)$$

$$\alpha_{th} = \frac{(2 \cdot n_0 - 1) \cdot k_b}{q} \left[\frac{3}{2} + \ln \left(\frac{\sqrt{N_c \cdot N_v}}{N_a} \right) \right] \quad (2)$$

$$- \frac{(n_0 - 1) dE_g}{2 \cdot q \cdot dT}, \quad (3)$$

where k_b is the Boltzmann's constant; q the elementary charge; N_c, N_v are respectively the effective density of states on the conduction band and valence band; N_a the acceptors doping density; $n_0 = 1 + \gamma/(2\sqrt{2}\phi_F)$; γ the body factor; ϕ_F the bulk quasi-Fermi level of the major carriers. Though α_{th} is not constant over temperature, their variation in extensive temperature ranges still negligible [16].

2) MOBILITY TEMPERATURE DEPENDENCY

Usual mobility temperature dependency modeling considers an exponential temperature dependency. This model is valid under the assumption that one of Si's significant scattering events is predominant. The primary approach to combine different scattering effects is Matthiessen's rule:

$$\frac{1}{\mu_{eff}} = \sum_i \frac{1}{\mu_i}, \quad (4)$$

where μ_{eff} is the total effective mobility and μ_i the contribution of each scattering event. However, as pointed out in [19], Matthiessen's rule is only valid using the Time Relaxation Approximation, assuming Boltzmann statistics, and, more importantly, if the characteristic scattering exponents are the same for the different scattering mechanisms. These assumptions are hardly valid for Si-based transistors in their working environment. Typical process design kit, transistor models combine surface phonon scattering and surface roughness using Matthiessen's rule expressed as:

$$\mu_{eff} = \frac{\mu_0}{1 + \left[(\theta_{ph} \cdot E_{eff})^{\nu/3} + (\theta_{sr} \cdot E_{eff})^{k \cdot \nu} \right]^{1/\nu}} \cdot \left(\frac{T}{T_0} \right)^{-\beta_\mu}, \quad (5)$$

where E_{eff} is the effective electric field; θ_{ph}, θ_{sr} are empirical parameters related to phonon scattering and surface roughness; μ_0 is the carrier mobility limited by ionized impurity scattering and acoustic phonon scattering; ν is an empirical parameter that accounts for a statistical averaging of the relaxation times [20]; β_μ is the strong inversion temperature coefficient [16]. This claim can hold either in a short temperature range or at a specific inversion level where a scattering mechanism is dominant.

Sub-micron MOS technologies require a deeper understanding of semi-classical and quantum transport. As pointed out by [21], ballistic transport begins to overcome the classic drift-diffusion regime. Therefore, it represents a new challenge for the already difficult task of modeling mobility.

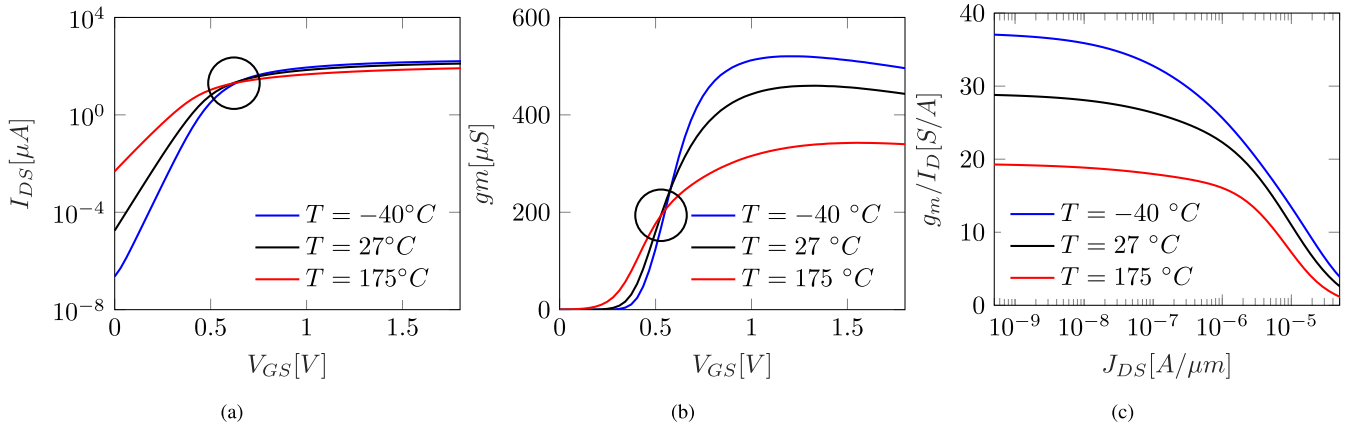


FIGURE 1. Electric Simulation of (a) $I_D \times V_{GS}$, $V_{DS} = 1.8$ V, (b) $g_m \times V_{GS}$, $V_{DS} = 1.8$ V and (c) g_m/I_D , $V_{DS} = 1.8$ V for a $10 \times 0.22 \mu\text{m}^2$ low V_{th} NMOS transistors of XT018. Sub-figures (a) and (b) present a ZTC bias point around 0.6 V and 0.5 V, respectively, and (c) does not present such a ZTC bias point. All three figures are taken at -40°C (blue), 27°C (black), and 175°C (red), which lies on the temperature range in which the process design kit is validated.

Since mobility temperature modeling is a complex task for semiconductor physics, it is even more challenging for the designer to consider it. For this reason, most of the model modifications to better account for temperature changes are empirical or semi-empirical expressions for mobility temperature dependency [22], [23].

3) ZTC BIAS

MOSFET ZTC bias are well known since the beginning of MOS technology, notably the drain to source current ZTC (I_{DSZTC}) [24] and, more recently, the gate transconductance ZTC [11] (g_{mZTC}). The I_{DSZTC} is illustrated in Fig. 1(a) for an NMOS transistor from XT018 technology; the ZTC condition is given in [24] as:

$$V_{GS} - V_{th} = \frac{V_{th} + \phi_B}{2} \left[\frac{1}{T} - \frac{\partial n_i}{\partial T} \frac{1}{n_i \cdot \ln(N_D/n_i)} \right] - \frac{\partial \bar{\mu}}{\partial T} \frac{1}{2 \cdot \bar{\mu}}, \quad (6)$$

V_{th} is the extrapolated strong inversion threshold voltage; ϕ_B the bulk potential; n_i the intrinsic carrier concentration and $\bar{\mu}$ the average channel mobility. One may conclude that the I_{DSZTC} is found for a V_{GS} between 0.6V to 0.8V.

More recently, the gate transconductance ZTC (g_{mZTC}) was proposed by [11], using the UICM model described as:

$$\frac{\partial \ln(\mu)}{\partial T} \left(\sqrt{1 + i_{fgz}} - 1 \right) - 2 + \frac{\sqrt{1 + i_{fgz}} + 1}{\sqrt{1 + i_{fgz}}} \times \left(\frac{\partial V_{th}}{\partial T} \frac{q}{\eta \cdot k_b} + 2 - \ln(\sqrt{1 + i_{fgz}} - 1) \right), \quad (7)$$

η is the threshold slope and i_{fgz} the inversion coefficient at the I_{DSZTC} point.

Even though those ZTC points exist, their bias condition relies on mobility temperature dependency, which depends on several scattering effects including ballistic ones in new technologies [25]. For this reason, modeling the temperature dependency is a challenging task. Besides, Fig. 1(a) and 1(b) highlight a required V_{GS} close to V_{th} from this

technology and, therefore, in the moderate inversion region. In opposition to the strong and weak inversion, the moderate inversion does not present a straightforward current model [13]. Furthermore, some critical parameters for analog and digital design, i.e., g_{DS} , are already proven to do not have a ZTC point, as pointed out in [9].

To propose a common framework for temperature-aware design, one may approach it using a design methodology such as g_m/I_D . Proposed by Silveira *et al.* [26] is a powerful transconductance to drain current method to help designers size up transistors quickly. The so-called “ g_m/I_D design” was initially developed to calculate parameters such as small-signal gain and bandwidth, later extended to distortion analysis [27], age-dependent degradation effects [28], and short channel effects [29].

III. TEMPERATURE ANALYSIS OF G_M/I_D PARAMETERS

The g_m/I_D methodology introduces width-independent parameters allowing the designer to choose the transistor W to accommodate other circuit prerequisites such as power consumption, occupied active surface, and operation region. The main parameters analyzed in this paper are the gate transconductance ratio (g_m/I_D) and the transistor self-gain (g_m/g_{ds}). The mathematical model to analyze those parameters will be based on the UICM model, introduced by Galup and Schneider [30], a charge-based model that accounts for accurate, but straightforward g_m/I_D parameters expressions, even quasi-ballistic nanometer-sized transistors [31]. The validation is done using the factory temperature validated BSIM model from -40°C to 175°C and measurement data from 27°C to 200°C .

A. GATE TRANSCONDUCTANCE RATIO

The g_m/I_D parameter for a long-channel transistor, neglecting specific current gate voltage dependency, is defined in the UICM model as:

$$\frac{g_m}{I_D} = \frac{2}{\eta(V_G) \cdot \phi_T (q_{is}(V_G, V_S) + q_{id}(V_G, V_D) + 2)}, \quad (8)$$

where ϕ_T is the usual thermal voltage and q_{is} , q_{id} are the inversion charge on the source side and the drain side normalized by the inversion charge at pinch-off.

Fig. 1(c) illustrates the g_m/I_D parameter obtained from electrical simulation using XT018 process design kit for a $10 \times 0.22\mu\text{m}^2$ low V_{th} NMOS transistor for three different temperatures, one may notice the absence of ZTC bias. From a design point of view, it is helpful to analyze the bias dependency of the given parameter, analyzing (8), the only term that is not bias dependent is ϕ_T . In order to evaluate the bias effect on g_m/I_D one may define the temperature normalized gate transconductance ratio (G_g) as:

$$G_g = \phi_T \cdot \frac{g_m}{I_D}. \quad (9)$$

The sensitivity is defined in [32] as the normalized variation $S_x^{y(x)} = \frac{\Delta y}{y} \approx \frac{x}{y(x)} \cdot \frac{dy(x)}{dx}$. The temperature normalized gate transconductance G_g is a function of η , q_{is} and q_{id} , and can be expressed as:

$$S_T^{G_g} = - \left[S_T^\eta + (q_{is} \cdot S^{q_{is}} + q_{id} \cdot S^{q_{id}}) \cdot \frac{G_g \cdot \eta}{2} \right]. \quad (10)$$

As reported in [31], the weak inversion slope factor η is sufficient to represent the g_m/I_D characteristics even in quasi-ballistic transistors; therefore, one may define η by ignoring the inversion charge as:

$$\eta = \left(\frac{\partial \psi_{sa}}{\partial V_{GB}} \right)^{-1} = 1 + \frac{\gamma}{2 \cdot \sqrt{\psi_{sa}}}, \quad (11)$$

$$\psi_{sa} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}(T)} \right)^2, \quad (12)$$

by definition, the η sensitivity can be calculated as:

$$S_T^\eta = \frac{T}{2} \frac{\partial V_{FB}/\partial T}{\psi_{sa}^2 (2 \cdot \sqrt{\psi_{sa}} + \gamma)}, \quad (13)$$

the flat-band voltage temperature behavior depends on the materials used for the transistor gate contact and bulk. In the node sizes addressed in this paper, the gate contacts are highly doped poly-Silicon with bulk-Si. The poly-Silicon is considered doped enough, so its Fermi level is pinned to the conduction band. By considering a low enough doping on the bulk and that Boltzmann statistics apply, one may write:

$$\frac{\partial V_{FB}}{\partial T} = \frac{1}{T} \left(\frac{E_G(T=0)}{2 \cdot q} - \phi_F \right). \quad (14)$$

For Silicon, the extrapolated bandgap at 0 K ($E_G(T=0)/q$) is 1.12 eV; for normal doping levels, the Fermi level is not very apart from the middle gap ($E_G(T=0)/2 \cdot q$) making the flat-band voltage (V_{FB}) temperature derivative very low and, by consequence S_T^η negligible.

Some approximations were made for the development of the η sensitivity. Fig. 2 evaluates the relative error of those approximations when calculating the Fermi Level. The gray area's top represents the limit where Boltzmann statistics and

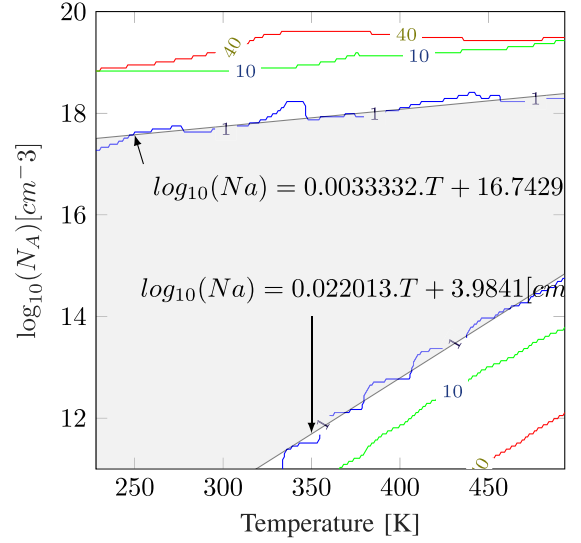


FIGURE 2. Relative error of approximation of Boltzmann statistics, neglecting minority carriers, and complete dopant ionization on the calculation of the Fermi level.

incomplete dopant ionization give a relative error smaller than 1%. The bottom border of the gray area is caused by neglecting minority carriers on the Fermi level calculation. Since the usual doping of Silicon starts to rise with scaling, some factors to account for Fermi-Dirac statistics and incomplete ionization may be added for smaller technologies.

The normalized inversion charges (q_{is} , q_{id}) sensitivity can be obtained from the so-called universal MOSFET characteristics of the UICM model:

$$\frac{V_p - V_{S(D)}}{\phi_T} = q_{is(d)} - 1 + \ln(q_{is(d)}). \quad (15)$$

by taking the temperature sensitivity of both sides of (15) one may find

$$S_T^{q_{is(d)}} = - \frac{V_p \cdot (S_T^{V_p} - 1) + V_{S(D)} \cdot (S_T^{V_{S(D)}} - 1)}{\phi_T \cdot (q_{is(d)} + 1)}. \quad (16)$$

It is essential to point out that unlike the ZTC bias pointed out on Section II-A3 the bias voltages are considered temperature-dependent. The importance of considering the temperature dependency of the bias voltages is that even though on the test benches often used for to extract the ZTC points, the bias point is constant, in a more complex circuitry, transistor nodes not connected at voltage sources can suffer from bias drift with temperature. For an extended temperature range, the use of Silicon on Insulator (SOI) is essential to minimize gate currents. Considering a MOSFET with source and bulk connected $V_S = 0$ and that in moderate inversion ($1 < q_{is(d)} < 100$) $q_{is} \approx q_{id} = \bar{q}$ one may find:

$$S_T^{G_g} = \frac{\bar{q} \cdot (V_p (S_T^{V_p} - 1))}{\phi_T (1 + \bar{q})^2}. \quad (17)$$

Since q_{id} , q_{is} , G_g , η , and ϕ_T are always greater than 0, one may find that the ZTC condition is $V_p (S_T^{V_p} - 1) = V_x$, by

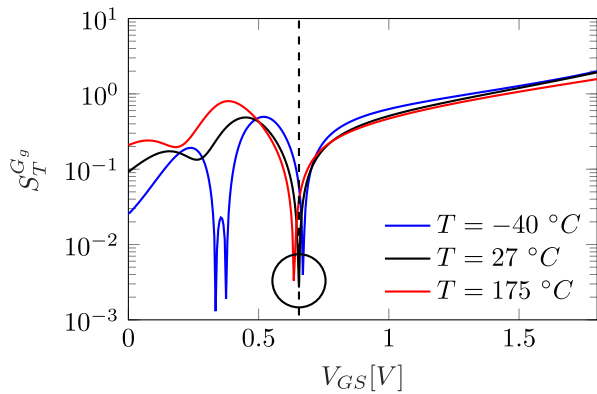


FIGURE 3. The G_g for a Low VT NMOS transistor $10 \mu\text{m} \times 10 \mu\text{m}$ on different temperatures on the valid simulation range.

taking the usual approximation of $V_p \approx (V_{GB} - V_{th})/\eta$ and the threshold temperature dependency from (1). One may find that the nil condition of (17) is

$$V_p|_{S_T^{G_g}=0} = \frac{\alpha_{th} \cdot T}{\eta} \quad (18)$$

At the vicinity of the ZTC point, $V_p \approx 0$; $q_{is} \approx q_{id} \approx 1$ [30] the sensitivity can be approximated as:

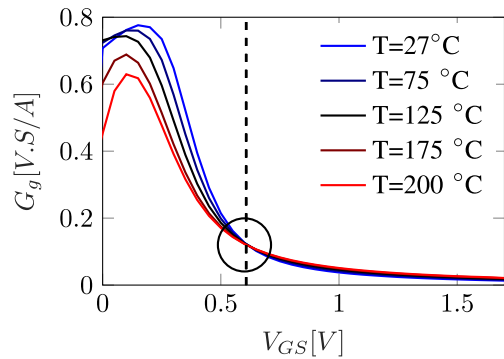
$$S_T^{G_g} \approx \left(\frac{T \cdot \alpha_{th}}{V_p \cdot \eta} - 1 \right) \frac{V_p}{4 \cdot \phi_T}, \quad (19)$$

by replacing (18) in (15) ones may find that \bar{q} it is independent of V_D and equal to a temperature invariant constant (ν):

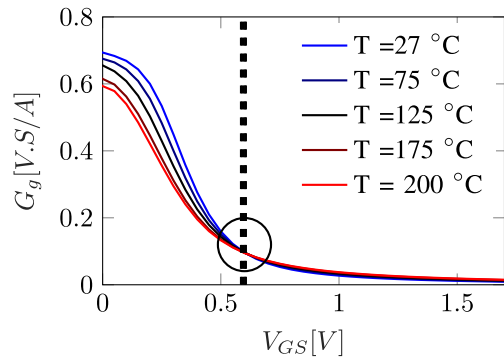
$$G_g|_{ZTC} = \frac{1}{2 \cdot \eta \cdot \nu} \quad (20)$$

Since for modern node sizes α_{th} tends to get smaller due to the channel doping increase [13], and η lies between 1 and 3, the right-hand side of (18), is very close to zero and a weak temperature function. Fig. 3 shows the sensitivity of the G_g parameter for a $10 \times 10 \mu\text{m}^2$ low V_{th} transistor obtained from BSIM simulations using the factory validated PDK from -40°C to 175°C . It is important to point out that in our simulations, the same ZTC point was found in small length transistors, which is expected since g_m/I_D is known to have little channel length dependency [31].

To extend the temperature range, factory measurements were made and are here presented on Fig. 4. The same ZTC bias point can be seen in measurement data obtained from the same transistor up to 200°C . Fig. 4 shows the G_g parameter extracted from measurement data at 27, 75, 125, 175, 200°C of a long and a short channel Low V_{th} NMOS transistor with the estimated V_{GSZTC} . The gate transconductance was obtained using Euler's method, and the threshold voltage was obtained at the different temperatures by the linear extrapolated method with the correction proposed in [33] following the threshold definition. The extracted V_{th} at different temperatures was later fitted using least squares to obtain α_{th} and V_{th0} estimation. The η parameter was obtained from the linear interpolation of the log current in weak inversion.



(a)



(b)

FIGURE 4. The G_g parameter extracted from measurement data from a Low VT NMOS transistor at 27, 75, 125, 175, 200°C (from blue to red) with dimensions (a) $10 \times 10 \mu\text{m}^2$ and (b) $10 \times 0.18 \mu\text{m}^2$ with $V_S = 0$ and $V_D = 0.1 \text{ V}$.

B. SELF GAIN

Another critical parameter on the g_m/I_D methodology is the self-gain (g_m/g_{DS}). This parameter's modeling needs to be handled with little more attention since the self-gain is very sensitive to short channel effects compared to the g_m/I_D parameter. According to [34], the significant short channel effects controlling the drain to source transconductance are velocity saturation, drain induced barrier lowering (DIBL), and channel length modulation (CLM). Those effects will be first evaluated, and then a g_m/g_{DS} expression will be presented for temperature behavior evaluation.

1) DIBL

The DIBL is a 2D effect that includes the variation of carriers barrier on the source to drain axis caused by the V_D variation. In a long channel MOSFET, the threshold voltage can be extrapolated from the classical MOS capacitor 1D analysis, since most of the channel has similar behavior. However, this approximation does not hold in short channels since the transverse field and drain/source junctions can no longer be neglected. In the short channel case, the V_D increase causes a reduction of the PN barrier between source and gate, usually modeled as a linear relationship between the

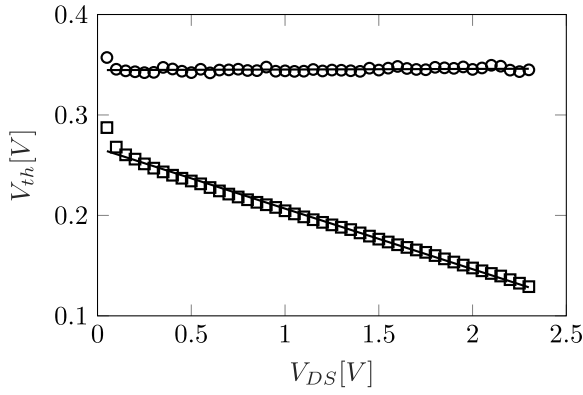


FIGURE 5. Estimated DIBL from measurement data for a Low VT NMOS transistor with $L = 0.18\mu\text{m}$ (squares), $L = 10\mu\text{m}$ (circles), and the fitted data (solid lines).

threshold voltage and V_D [13].

$$V_{th}(V_{DS}) = V_{th}(0) - \sigma \cdot V_D. \quad (21)$$

Since the definition of DIBL naturally depends on the transistor length, many works have proposed different $\sigma(L)$ relations. However, most experiments show a power relation with L [13]. One may express this relation in general as:

$$\sigma(L) = \frac{(\sigma_0 + \sigma_1 \cdot V_{SB})}{\pi t_{ox} L^m}. \quad (22)$$

Fig. 5 shows the DIBL effect from measurement data. V_{th} was extracted using the method explained in [17]. Even though the work [26] points out a linear increase of σ with temperature, as illustrated in Fig. 6, the 99.7% confidence bars of the extracted σ value exceeds the presented temperature variation, and therefore was considered negligible. Since the available measurement data only contains two different channel lengths, the σ parameter was extracted from Spectre simulations from the foundry PDK. Even though BSIM 4v6 (suitable for the node size) models $\sigma(L)$ having an exponential relation, [13] points out that the model shown in (22) fits better with experimental results. For this reason the latest BSIM version uses (22) model [16]. Fig. 7 shows the comparison of both models presenting overall similar behavior.

2) VELOCITY SATURATION

With the decrease of channel length, the electric fields hugely increase, giving carriers more energy and increasing the probability of scattering events [19]. This increase of scattering events, limits the maximum electric field on the channel to a value E_{sat} . This saturation makes the transition between the linear and saturated regimes occurs earlier than the classical limit $V_{D_{sat}} = V_{GS} - V_{th}$. In [34], the $V_{D_{sat}}$ is considered constant ($\approx L \cdot E_{sat}$) because the channel length is smaller than 200 nm , which is not the case for all transistors on the working technology. Jepers *et al.* [35] define $V_{D_{sat}}$ as $2/g_m$ that, in contrast to [34] is highly dependent of

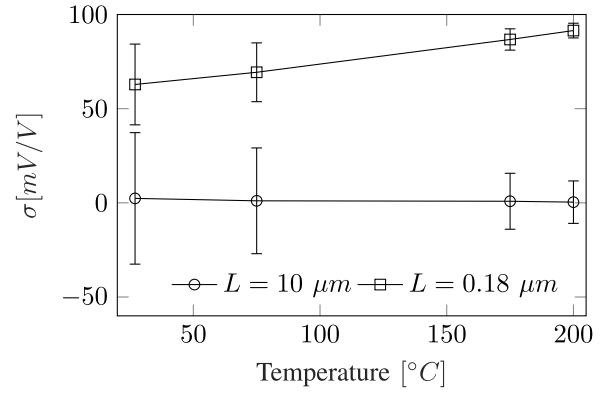


FIGURE 6. Estimated DIBL from measurement data for a Low VT NMOS transistor with $L = 0.18\mu\text{m}$ (squares), $L = 10\mu\text{m}$ (circles) and the fitted data (solid lines).

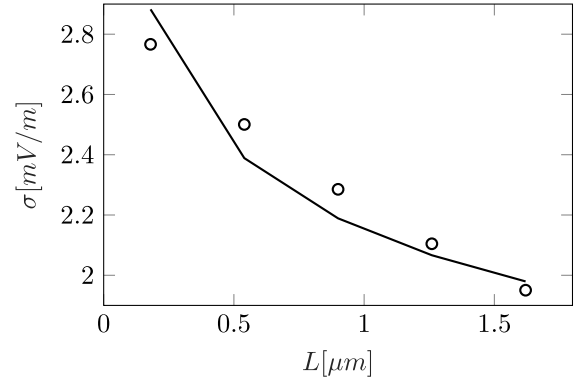


FIGURE 7. Estimated σ parameter for different channel lengths estimated from BSIM 4v6 (circles), and fitted data.

V_{GS} , a proposition considering both effects in $V_{D_{sat}}$ is given in [36] as:

$$V_{D_{sat}} = 2/g_m \| L \cdot E_{sat}. \quad (23)$$

To validate (23), $V_{D_{sat}}$ was extracted using [37], the E_{sat} value was calculated from the measured g_m/I_D for $L = 10\mu\text{m}$ and then reused for $L = 0.18\mu\text{m}$. The obtained $V_{D_{sat}}$ can be shown in Fig. 8. The obtained $E_{sat} = 1.396 \cdot 10^4\text{ V/cm}$ value is in accordance with literature values.

3) CHANNEL LENGTH MODULATION

When the drain to source voltage exceeds $V_{D_{sat}}$, the pinch-off region starts to grow towards the source, making the effective channel length smaller with the increase of V_{DS} . In [34] the CLM effect is modeled as:

$$F_{CLM}(V_{DS}) = \left(1 + \frac{V_{DS} - V_{D_{sat}}}{V_0}\right)^{\frac{1}{\alpha}}, \quad (24)$$

the α coefficient is a length-dependent coefficient responsible for the CLM strength and V_0 a constant model parameter. It is important to point out that, even though no temperature studies were made concerning the α and V_0 parameters, they showed no temperature dependency on our experiments. Fig. 9 shows the results from the extraction of CLM

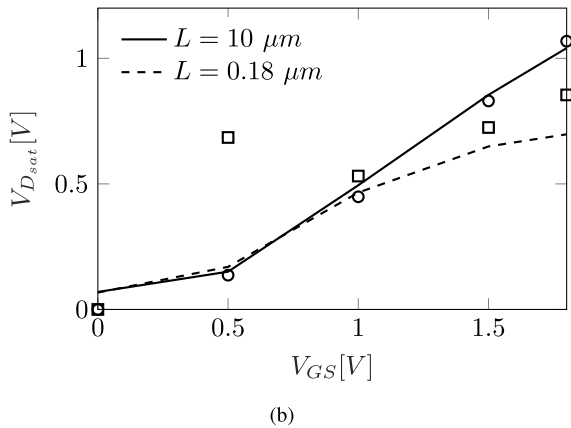
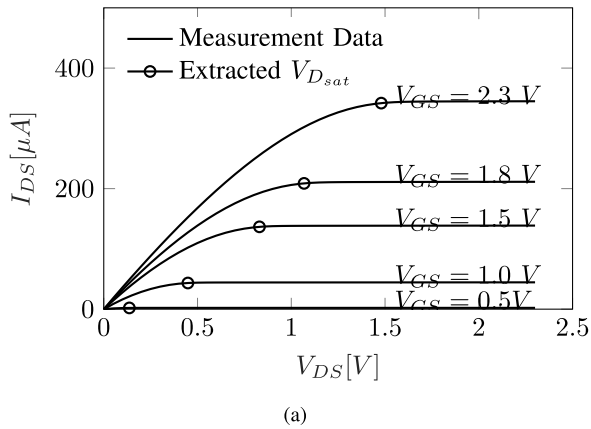


FIGURE 8. V_{Dsat} Extraction, in (a) the extracted V_{Dsat} is highlighted with circles at different V_{GS} , (b) shows the extracted model based on (23) for $L = 10\mu m$ (circles) and $L = 0.18\mu m$.

parameters using [34] for different channel lengths and temperatures, α and V_0 were kept constant through different temperatures while E_{sat} modeled with a surface roughness scattering predominant model [13]. The obtained values where $V_0 = 0.433$ V and the α parameter modeled in [38] as:

$$\alpha = \alpha_0 + \alpha_1 \cdot L + \alpha_2 \cdot L^2. \quad (25)$$

It is important to point out that the temperature variation observed in Fig. 9(a) is due to E_{sat} variation following the dependency of the limiting scattering effect. Contrary to mobility temperature dependency, the scattering mechanism is known and unique (surface roughness scattering on Silicon). Since only one scattering mechanism is responsible for the field saturation, the exponential temperature behavior can be taken with no approximation. Fig. 9(b) validates (25) by showing the extracted value of α and the polynomial relation with the channel length.

4) G_M/G_{DS} MODEL

The latest subsections explained the principal effects that affect the self-gain, with those effects modeled and extracted based on [35] definition, one may write g_m/g_{ds} as a function of the temperature normalized gate transconductance

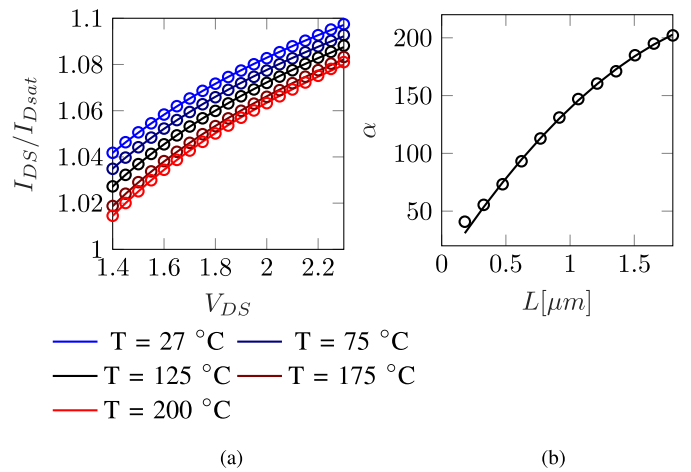


FIGURE 9. CLM parameters extraction, (a) for $L = 0.18\mu m$ for temperatures 27, 75, 125, 175, 200 °C (from blue to red) and α obtained from L_{min} to $10 \cdot L_{min}$. Circles represent extracted data from simulations, and lines the proposed models.

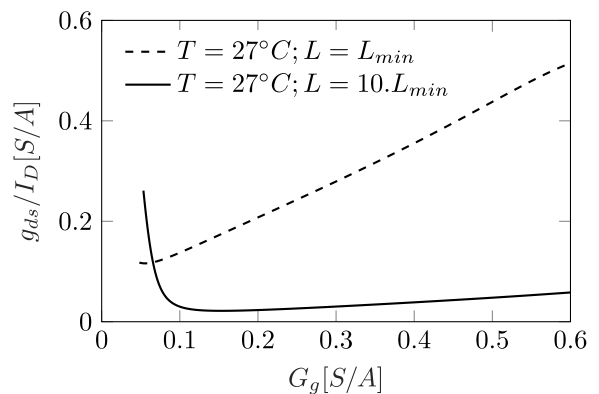


FIGURE 10. $g_{ds}/I_D \times G_g$ plot obtained from BSIM model for different L and $V_{DS} = 0.6V$.

ration G_g :

$$\frac{g_m}{g_{ds}} = \frac{g_m}{I_D} \cdot \left(\frac{g_{ds}}{I_D} \right)^{-1} \quad (26)$$

$$\frac{g_{ds}}{I_D} = \sigma \cdot \frac{G_g}{\phi T} + \frac{1}{\alpha \cdot \left(V_0 + V_{DS} - \left(\frac{2\phi T}{G_g} \parallel L \cdot E_{sat} \right) \right)}. \quad (27)$$

Fig. 10 shows the $g_{ds}/I_D \times g_m/I_D$ plot for one transistor with two different channel lengths. The decreasing part of the curve is dominated by CLM, represented by the second term in (27). The increasing portion is the DIBL dominated g_{ds}/I_D (G_g) relation. Fig. 11 shows the temperature variation of the g_{ds}/I_D parameter using $4 \cdot L_{min}$, a very common rule of thumb length for analog design, $V_{DS} = 0.6V$ at different temperatures -40 °C, 27 °C and 175 °C. Even though the different curves cross in an area close to $G_g = 0.1$ the difference on the bias of those crossing points are very different and therefore unusable for large temperature variations. For low-power devices, weak and moderate inversion bias is preferable, the transistor's bias point will rather lie

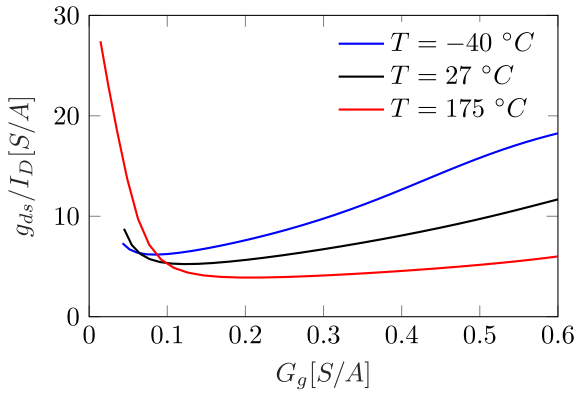


FIGURE 11. $g_{ds}/I_D \times G_g$ plot obtained from BSIM model for different L and $V_{DS} = 0.6\text{V}$.

on the DIBL dominated region. As in the g_m/I_D characteristics, a factor $1/\phi_T$ is present on this region. Thus, one may define a temperature normalized quantity (G_d) for the g_{ds}/I_D similarly to what was done for g_m/I_D as

$$G_d = \frac{g_{ds}}{I_D} \phi_T. \quad (28)$$

Since most of the analog expressions for circuits are written in terms of g_m/I_D and g_m/g_{ds} , it is essential to highlight the expression of the latter as a function of the temperature normalized g_m/I_D parameters. Fig. 12 shows the relation of both temperature normalized parameters for different channel lengths.

$$\frac{g_m}{g_{ds}} = \frac{\frac{g_m}{I_D}}{\frac{g_{ds}}{I_D}} = \frac{G_g}{G_d}. \quad (29)$$

Fig. 12 shows the two proposed temperature normalized g_m/I_D parameters (G_g , G_d) for two different channel lengths, extracted using (27) and the previous extracted values. At first glance, it is noticeable that a ZTC point occurs in the DIBL dominated portion of G_d in small channel sizes.

5) TEMPERATURE ANALYSIS

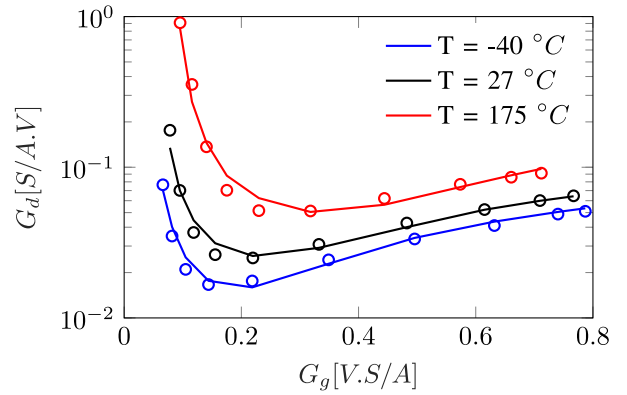
In order to evaluate the G_d temperature sensitivity, one may write (27) as a function of G_g , for this matter, G_d will be divided into two parts, responsible for DIBL and CLM effects:

$$\begin{cases} G_d^{DIBL} = \sigma \cdot G_g \\ G_d^{CLM} = \frac{\phi_T (G_g L E_{sat} + 2 \phi_T)}{\alpha (V_0 + V_{DS}) (G_g L E_{sat} + 2 \phi_T) - 2 \phi_T L E_{sat}} \end{cases} \quad (30)$$

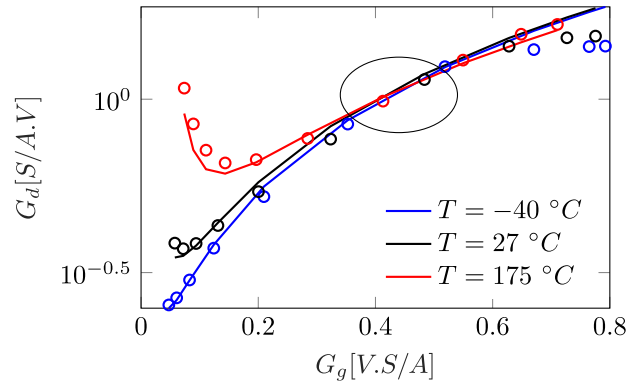
By separating G_d on those factors, the total sensitivity can be written as:

$$S_T^{G_d} = \frac{G_d^{DIBL} \cdot S_T^{G_d^{DIBL}} + G_d^{CLM} \cdot S_T^{G_d^{CLM}}}{G_d}, \quad (31)$$

Furthermore, ZTC bias occurs in the DIBL dominated part of G_d , i.e., G_d^{CLM} close to $\phi_T/\alpha(V_0 + V_{DS})$. The sensitivity of G_d^{DIBL} is approximately the same as G_g due to the weak



(a)



(b)

FIGURE 12. Proposed temperature normalized parameters extracted from for (a) $L = 10 \mu\text{m}$ and (b) $L = 0.18 \mu\text{m}$ for temperatures $-40, 27$ and 175°C (from blue to red) obtained from simulated data.

temperature dependency of the multiplicative factor. One may suppose that the ZTC points occur when:

$$\sigma \cdot G_g \cdot S_T^{G_g} = -\frac{\phi_T}{\alpha(V_0 + V_{DS})}, \quad (32)$$

using the approximations developed for the ZTC vicinity of G_g

$$\left(V_p \Big|_{S_T^{G_g}=0} - V_p \right) = -\frac{8\eta\phi_T^2}{\alpha \cdot (V_0 + V_{DS})\sigma}. \quad (33)$$

Fig. 12(b) shows the G_d sensitivity, as described by (33). The linear relation with G_g makes the overall shape pretty similar. However, minimum point position is now dependent on V_{DS} , L , and V_p in opposition to the $S_T^{G_g}$ that mainly depended on V_p . It is important to point out that (33) implies that there is a maximum channel length that the ZTC occurs, this relation depends on the dependency of σ and α to L better developed as:

$$\phi_T^2 \cdot C_1 \cdot L^m = -C_2 \cdot \Delta V_p \cdot \alpha(L)(V_0 + V_{DS}), \quad (34)$$

where $C_1 = 8 \cdot \eta \cdot \pi \cdot t_{ox}$, $C_2 = \sigma_0 + \sigma_1 \cdot V_{SB}$, and ΔV_p the left-hand side of (33). Since L^m is a monotonic function and α a quadratic polynomial, if (33) occurs then it must cross twice defining a region where the ZTC condition is fulfilled.

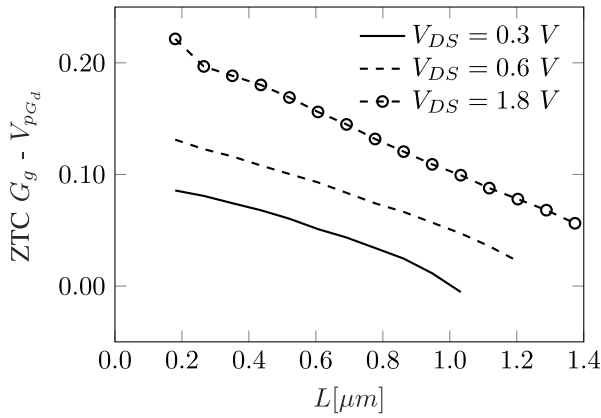


FIGURE 13. Extracted pinch-off voltage at G_d ZTC for different V_{DS} and channel lengths.

Fig. 13 shows the pinch-off voltage G_d ZTC obtained from BSIM 4v6 simulations. The lines lie inside the limit defined in (34). The short channel ZTC point comes in contrast with usual analog design practices that maximize L to increase linearity performance, with the trade-off of decreasing speed performance.

Another way of seeing this deduction is given that when L gets bigger, the DIBL effect gets smaller and CLM dominates on (30); $S_T^{G_d}$ approaches to $S_T^{G_d^{CLM}}$, which has no ZTC bias point. Both sensitivities for long and small channels are illustrated in Fig. 14.

IV. CIRCUIT DESIGN EXAMPLE

To better illustrate how the temperature normalized g_m/I_D parameters can be used in a temperature-aware design, one may take as an example a simple PMOS differential pair OTA with active load, as illustrated in Fig. 15. This example is often used in design methodology studies as a standard testing circuit [26], [39]. The voltage gain and its temperature sensitivity can be written in terms of the temperature normalized parameters as:

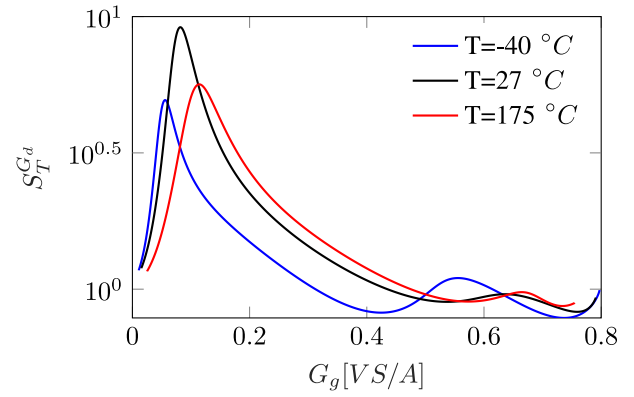
$$|A_v| = \frac{G_{g2}}{G_{d1} + G_{d2}}, \quad (35)$$

$$S_T^{A_v} = S_T^{G_{g2}} - \frac{S_T^{G_{d1}} \cdot G_{d1} + S_T^{G_{d2}} \cdot G_{d2}}{G_{d1} + G_{d2}}. \quad (36)$$

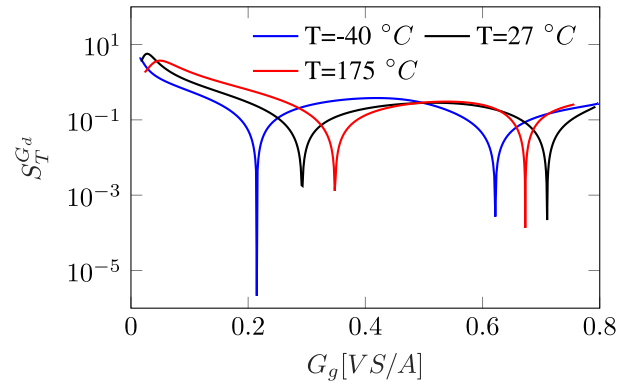
By imposing $M_{2A,B}$ and $M_{1A,B}$ to be at the vicinity of G_{gZTC} developed in (20), (36) simplifies to:

$$S_T^{A_v} = \frac{1}{4} \frac{(TV_{th2} \alpha_{th} - V_{p2}) \sigma_2 (-\sigma_1 \eta_2 + \eta_1)}{\phi_T (\sigma_2 \eta_1 + \sigma_1 \eta_2)}. \quad (37)$$

Therefore to have a ZTC, A_v we must have either $V_{p2} = V_{pZTC} (\eta_2 - 1) = 0.08$ V or make $\sigma_1 = \frac{\eta_1}{\eta_2} = 1.0123$. Since it is not possible in the technology XT018 to have such a big DIBL coefficient, $M_{2A,B}$ is biased at $V_p = 0.08$ V. In order to compensate the (18) temperature dependency, the current-source temperature coefficient was chosen such as the temperature coefficient of $V_{D_{M_{2,A}}}$ being $\frac{\alpha_{th}}{\eta}$. The biasing



(a)



(b)

FIGURE 14. Extracted sensitivities for long channel ($L = 10 \mu m$) (a) and short channel ($L = 0.18 \mu m$) (b) at $-40^\circ C$ (Blue); $27^\circ C$ (Black); $175^\circ C$ (Red).

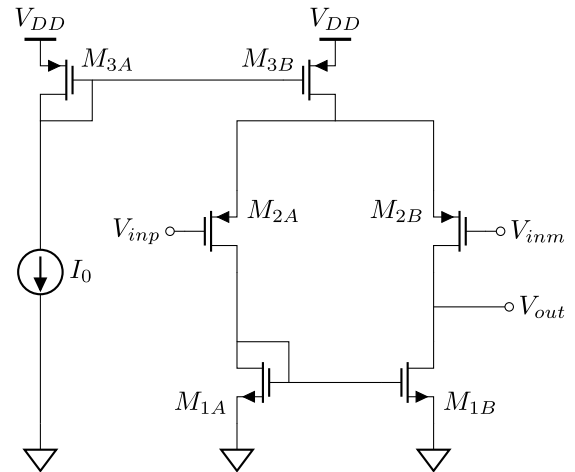


FIGURE 15. PMOS differential pair with active load.

transistors sizes were chosen so they are biased in I_{DSZTC} point.

The obtained voltage gain is illustrated in Fig. 16 at the typical corner and the worst corner boundary defined by FS and SF corners. It is essential to point out that the temperature coefficient of the bias current is negative, the

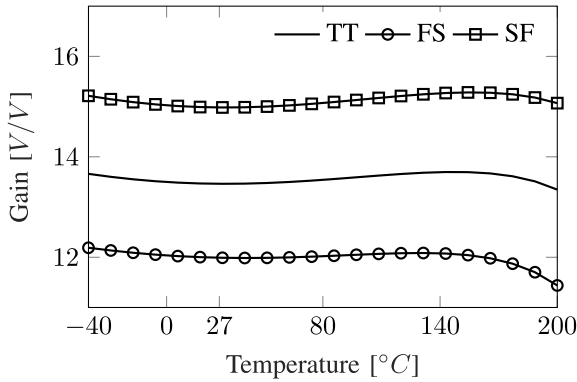


FIGURE 16. Gain variation over temperature in different corners of the amplifier design with the novel methodology.

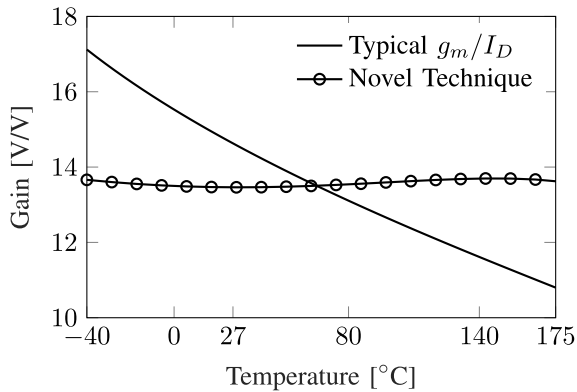


FIGURE 17. Comparison with gain over temperature using typical g_m/I_D methodology and the proposed in TT corner.

temperature-aware solution does not come with a power consumption ($9.2 \mu\text{W}$ at 27°C) increase. This is an essential feature for novel, temperature-aware, low-power IoT circuits.

To compare the novel technique with the conventional g_m/I_D methodology, one may take the methodology given in [35] for the same topology. All transistors' lengths were made $3 \cdot L_{min}$ for linearity improvement. The g_m/I_D of the active load, the differential pair, and the current mirrors were chosen to be 4 to decrease the gain loss compared to the common source amplifier and maintain the V_{Dsat} small enough for $M_{1,2,3}$ being saturated. The electrical simulations result from the classically designed circuit can be seen in Fig. 17.

In order to evaluate circuit temperature performance the temperature coefficient (TC) is usually used as a figure of merit. However the usual definition considers 27°C as a reference temperature. Since the goal of the method is to allow for a wide temperature working range, in contrast to a circuit that will work around ambient temperature, another approach is taken in this work. To this end, one may define a modified TC figure of merit as: $T_{C_{eqq}}(A_v) = (\max(A_v) - \min(A_v)) / (A_v(\text{mean}(T))(T_{max} - T_{min}))$.

Using the proposed definition, the obtained value of $T_{C_{eqq}}$ on typical corner for the proposed circuit is $107.33 \text{ ppm}/^\circ\text{C}$, compared with the traditional design that got roughly a 22 times bigger $T_{C_{eqq}}$ of $2364.46 \text{ ppm}/^\circ\text{C}$.

TABLE 1. Circuit dimensions and parameters.

	Novel Technique	Typical g_m/I_D
$W/L _{M1,A,B}$	10	2.8
$W/L _{M2,A,B}$	2.5	8.8
$W/L _{M3,A,B}$	2	8.8
Bias TC	$-19.5 \text{ nA}/^\circ\text{C}$	0
DC Power Consumption	$9.2 \mu\text{W}$	$240 \mu\text{W}$
Gain TC	$107.33 \text{ ppm}/^\circ\text{C}$	$2159 \text{ ppm}/^\circ\text{C}$

The different sizing and performance figures of the two designs are presented on Table 1. One may notice the more significant power consumption for the more traditional circuit since the transistors are classically biased in strong inversion.

The different corners on the optimized circuit still presented the same gain temperature regulation with different $T_{C_{eqq}}$, showing that the technique still works even with process variations.

Since the mean gain depends on g_{mPMOS}/g_{dsNMOS} parameter, it is expected, as seen in Fig. 16 that the SF and FS corners present a higher variation on the mean gain. However, this variation on the mean gain does not affect the small temperature sensitivity of A_v presenting $260 \text{ ppm}/^\circ\text{C}$ and $82.42 \text{ ppm}/^\circ\text{C}$ FS and SF corners, respectively.

V. CONCLUSION

An extension of the g_m/I_D method was proposed to allow for temperature-aware circuits' design by introducing temperature normalized g_m/I_D parameters. Those modified parameters allow the use of ZTC points in the early design stages. Those ZTC points were developed using the UICM model; however, they also allow a table-lookup design paradigm from g_m/I_D methodology. The limits of the temperature sensitivities of the weak inversion η parameter and the effective mobility (highly model dependent) were explored and ended up not being relevant for the ZTC analysis.

A circuit design was presented using the proposed methodology having an equivalent temperature coefficient of $107.3 \text{ ppm}/\text{K}$ for its gain performance having a 22 times improvement to the traditional g_m/I_D methodology. The novel temperature stabilization methodology is shown to hold even with process variability.

This is the first demonstration of a temperature-independent gain for an extended temperature range suitable for smart vehicles to the best of our knowledge. The use of a g_m/I_D methodology proves to be a very general design methodology that allows the designer to consider temperature effects using the novel technique proposed in this paper.

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