



HAL
open science

Experimental and simulation investigation of the out-of-equilibrium phenomena on the pseudo-MOSFET configuration under transient linear voltage ramps

Miltiadis Alepidis, Licinius Benea, Davide Bucci, Xavier Mescot, Maryline Bawedin, Irina Ionica

► To cite this version:

Miltiadis Alepidis, Licinius Benea, Davide Bucci, Xavier Mescot, Maryline Bawedin, et al.. Experimental and simulation investigation of the out-of-equilibrium phenomena on the pseudo-MOSFET configuration under transient linear voltage ramps. *Solid-State Electronics*, 2020, 168, pp.107721. 10.1016/j.sse.2019.107721 . hal-03171017

HAL Id: hal-03171017

<https://hal.science/hal-03171017v1>

Submitted on 20 May 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

Experimental and simulation investigation of the out-of-equilibrium phenomena on the Pseudo-MOSFET configuration under transient linear voltage ramps

Miltiadis Alepidis, Licinius Benea, Davide Bucci, Xavier Mescot, Maryline Bawedin, Irina Ionica

University Grenoble Alpes (UGA), CNRS, Grenoble INP, IMEP-LAHC 38016 Grenoble, France

Keywords

Pseudo-MOSFET configuration, transient measurements, simulation, out-of-equilibrium body potential, out-of-equilibrium phenomena

Abstract

The pseudo-MOSFET configuration is an electrical characterization technique developed for silicon-on-insulator (SOI) wafers. The wide variety of experiments that have been performed to date have also extended recently in the study of out-of-equilibrium phenomena for bio-sensing applications. However, the lack of a full understanding of the ohmic contact behaviour between the probes and the low doped silicon film results in simulation inconsistencies. This work proposes a simulated device structure that is capable of reproducing the behaviour of the device and further extends the experiments into large-signal linear ramps which are also reproduced through simulations.

1. Introduction

The pseudo-MOSFET configuration measurements are performed by the placement of two metal probes with controlled pressure on top of bare SOI wafers [1]. The metal probes mimic the source and drain contacts. The buried oxide (BOX) underneath the silicon film can be biased through the substrate and consequently acts like a gate dielectric. The combination of those elements creates a structure similar to an upside-down MOSFET. The main

utilization of this pseudo-transistor is the extraction of important parameters of the top silicon film, by exploiting different measurement methods: current-voltage characteristics for extraction of the mobility of electrons (e^-), holes (h^+) and threshold/flatband voltages [1,2], capacitance [3] and noise measurements [4,5] for estimation of interface state density. Carrier life times were also estimated by the pseudo-MOSFET configuration [6,7]. Recent advancements showed that out-of-equilibrium phenomena, such as the out-of-equilibrium body potential, manifest themselves in the pseudo-MOSFET configuration [8]. Similar to the fully depleted SOI MOSFETs, in which it was firstly reported [9], the out-of-equilibrium body potential variation arises when the transition between depletion and inversion/accumulation occurs and the carriers are not provided by the source and drain probes instantaneously. In this case, during the variation of the gate voltage, the lack of carriers needed to reach equilibrium drives the body potential into an out-of-equilibrium state which will simply follow the V_G variation. Obviously, one of the key elements to understand and exploit this phenomenon is related to the contacts that provide (or not) the free carriers for the channel formation. In the pseudo-MOSFET, this aspect is very complex to consider since, theoretically, metal probes on the low doped silicon film should behave as Schottky contacts. However, the metal probes used in the pseudo-MOSFET show ohmic behaviour and provide both types of carriers into the film [1,5,10–14]. The origin of this behaviour is not fully-understood and can be explained by defects under the metal contacts [11,14] or phase transformation in the silicon film [10]. Therefore, an implementation of ohmic contacts allowing both electron and hole transport with pressure controlled probes in the simulation software has not yet been developed.

The first aim of this work is to develop a simulation strategy for technology computer-aided design (TCAD) software that allows an accurate reproducibility of the measured “static” electrical behaviour of the pseudo-MOSFET with metal contacts. The

simulations will be used in the second part of the paper (section 3) to reproduce the electrical measurements of the configuration under fast transient conditions.

2. Pseudo-MOSFET contact emulation for the simulations

2.1. Pseudo MOSFET configuration characteristics

In order to understand the challenges for the pseudo-MOSFET simulation, we will describe the typical experimental aspects. The wafer used for this work has mesas of $5 \times 5 \text{mm}^2$ top silicon film defined by lithography and reactive ion etching from SOI. This produces a defined area of the silicon and restricts systematic current leakage that may appear if the BOX has defects on a side of the full wafer. The SOI has a silicon thickness $t_{\text{Si}}=88\text{nm}$ and a BOX thickness $t_{\text{ox}}=145\text{nm}$. The film is lightly P-type doped ($\sim 10^{15} \text{cm}^{-3}$). The substrate underneath the BOX has the same doping concentration as the film. The source and drain contacts are two tungsten pressure-controlled probes installed in a Jandel probe station. The wafer is placed on a metal chuck onto which the gate voltage (V_G) is applied (Fig.1a). Typical drain current (I_D) with respect to gate voltage (V_G) characteristics for low drain voltage (V_D), obtained with an Agilent B1500 semiconductor analyser, are presented in Fig.1b. In the characteristics, we observe the I_D associated to the electron channel in strong inversion ($V_G > 0$) and the hole current in accumulation ($V_G < 0$). The subthreshold slopes are comparable for the electrons and holes channels but the maximum current for holes is significantly lower due to different carrier mobilities and different series resistances [11]. As previously seen [12], low V_D guarantees ohmic regime and the metallic probes are able to provide both e^- and h^+ according to the V_G sign.

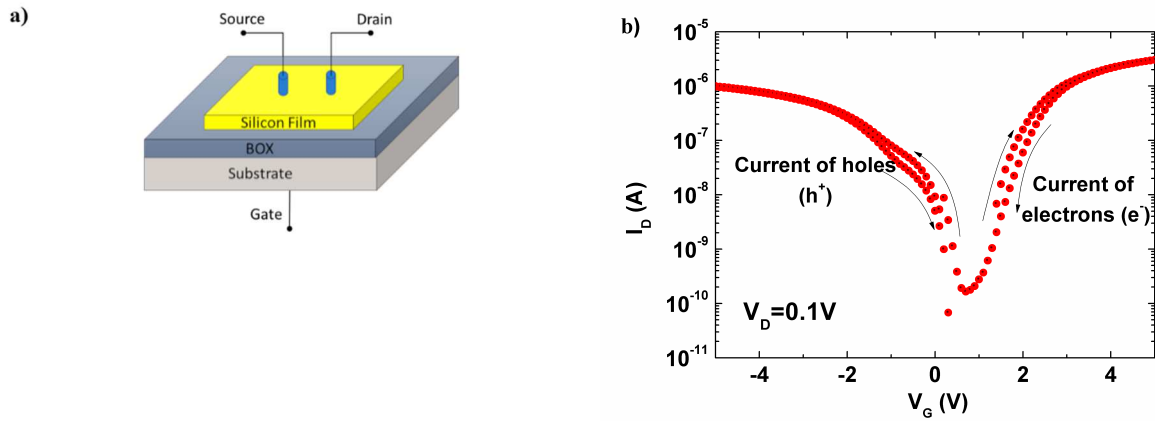


Figure 1: a) Schematic of the experimental configuration and b) Measured I_D - V_G characteristic curve for $V_D=0.1$ V.

2.2 Pseudo-MOSFET simulation strategy

The challenge in the simulation is that the contacts should be defined to match the experimental configuration and to allow the injection of both types of carriers into the channel. We start by defining a structure ($t_{si}=88$ nm and $t_{BOX}=145$ nm) in Sentaurus with the same layer thicknesses as the experimental one (Fig.1a). To consider substrate effects, a $t_{sub}=1.2\mu\text{m}$ bulk silicon region was included under the BOX in the simulation (the maximum space charge region was calculated at about 880nm for the doping of the substrate). The injection of both carrier types was demonstrated by defining metal regions as contacts with variable metal workfunctions [13]. However, this strategy was not very successful to reproduce the out-of-equilibrium phenomena. An alternative way to inject the two carrier types is to use highly doped P and N type regions as source and drain. If only one type of dopants is chosen, the electrical simulations will only show the channel of e^- or h^+ . Consequently, we would need to combine the results produced from two different structures, one for $V_G > 0$ and one for $V_G < 0$, to reproduce the complete I_D - V_G characteristics. For the study of the out-of-equilibrium phenomena this is not an option since they occur during the transition between the accumulation and the inversion regimes. In order to reproduce the full pseudo-MOSFET behaviour with a single structure, the contacts were defined as two regions

of silicon with different doping types and a concentration of 10^{20}cm^{-3} . The source and drain in simulations both have a P⁺-type and N⁺-type regions for the injection of electrons and holes, as shown in Fig.2. The total length of the device is made of the contacts length L_{con} , the distance between their inner edges L and 10% of L added on each side of the structure. This extension was included to the simulation structure for improved correlation to the experimental configuration. For all the simulations, we kept the L constant at $1\mu\text{m}$.

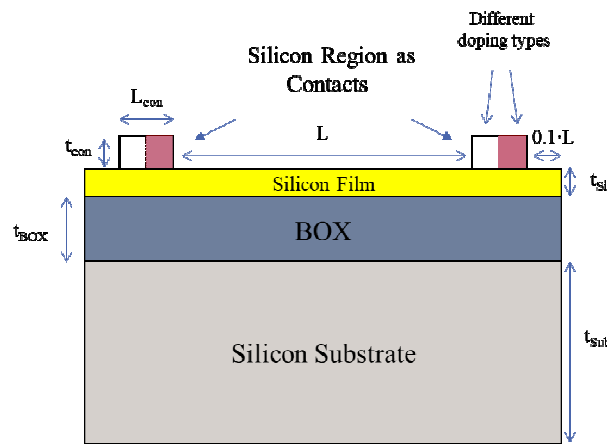


Figure 2: Pseudo-MOSFET simulation structure to emulate the source and drain contacts obtained experimentally with controlled pressure probes.

Different simulated combinations of doped areas were examined in order to emulate the contacts. The selection of the proper structure emerges from the benchmarking of the I_D - V_G simulated curves versus the real measurements. The drain voltage was set to 0.1V for all the simulations as in experiments and the source contact was grounded. Default models (ohmic boundary conditions between electrodes and highly doped regions) were applied for the electrode definition which was placed on top of highly doped regions. For the carrier mobility, the Lombardi model and doping dependence were used. In Fig.3a, the doping regions P⁺ or N⁺ on the contacts are mirrored with respect to the centre of the device. The simulated I_D - V_G characteristics shown in Fig.3b reveal that one carrier is favoured over the other. We evidence a really steep subthreshold slope with higher ON-current in PN-NP for electrons and in NP-PN structure for holes. Positioning a highly doped region on a lightly

doped silicon layer creates a barrier for the opposite carrier type. For instance, the space charge region under the N^+ region is a barrier for the hole flow through that side of the contact. To avoid this effect and to emulate the contacts properly, we studied the alternating doping regions (PN-PN and NP-NP, Fig.4a). In this case, we reproduce relatively similar subthreshold slopes in the I_D - V_G curves (Fig.4b) on both electrons and holes sides and a comparable ON-current for both configurations. The ON-current is slightly stronger in the electrons side compared to the holes side similarly to the experiments. While the difference in series resistance is mostly responsible for the higher electron ON current for the experiments, in the simulations, this deviation is mainly caused by the different mobility values for electrons and holes in the silicon. This can be evidenced by the ratios between the maximum values of currents and the mobility values in the simulator **which are** almost the same ($I_{ON-electrons}/I_{ON-holes} \approx 3.45$, $\mu_{electrons}/\mu_{holes} \approx 3.11$). The alternating doped contacts are more appropriate for the pseudo-MOSFET simulations and will be used for the next sections. A supplementary study based in the I_D - V_D curves is shown in the appendix A.

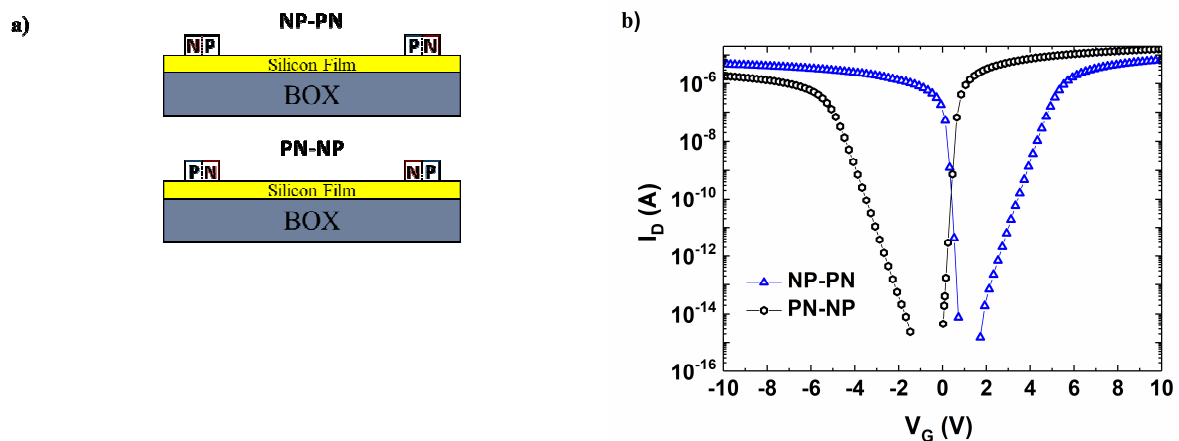


Figure 3: a) Schematic of the simulated structures with mirrored doping regions with respect to the centre of the device b) Simulated I_D - V_G for mirrored contacts, $V_D=0.1V$ and $L_{con}=0.5\mu m$.

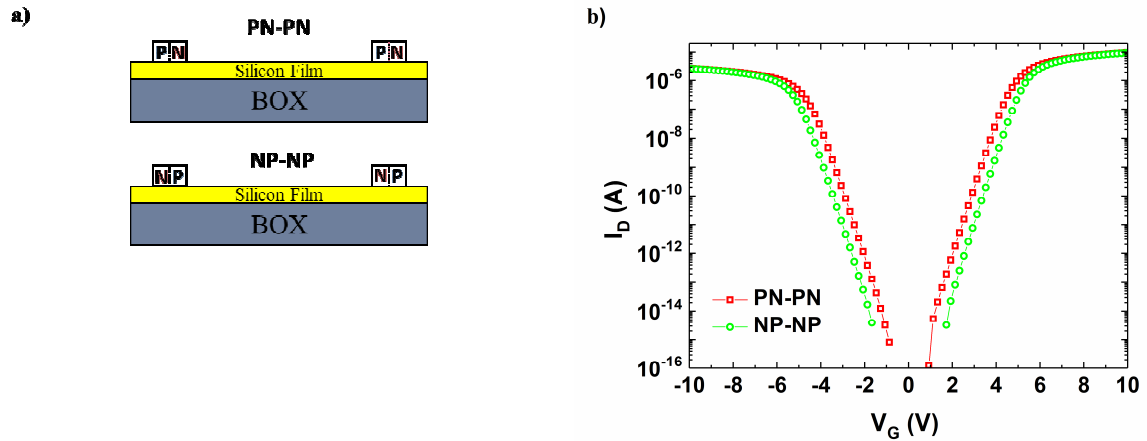


Figure 4: a) Schematic of the simulated structures with alternating doping for the contacts b) Simulated I_D - V_G for alternating doping contacts, $V_D=0.1V$ and $L_{con}=0.5\mu m$.

3. Transient Behaviour of the pseudo-MOSFET

3.1. Experimental set-up for transient current measurements

The dynamic character of any phenomenon originates from its dependence on time. To proceed with the time dependent experimental study, we apply a large triangular voltage ramp (AC), as illustrated in Fig.5, to the gate of the device in order to mimic the quasi-static (DC) V_G sweep in the forward and reverse scanning directions. The V_G scanning range of the measurement corresponds to the peak to peak of the triangular signal. We used a constant range from -5V to 5V (bias range allowing to cover the transient behaviour of interest) in all the transient experiments. The scanning speed of the back gate was varied by changing the triangular pattern frequency covering scanning speeds (SS) from 10V/s up to 400V/s. In all cases, the source contact was grounded and the drain was biased at $V_D=0.1V$. To perform with precision the above study, we used an Agilent B1500 analyser with a B1530A fast I-V module. Additionally, a slow transient measurement with a scanning speed of $SS \approx 1.667 V/s$ was included for a direct comparison between the large signals and “quasi-static” sweep measurements. The scanning speed was chosen to correspond to a DC sweep with a 100mV gate step, 20ms integration time and 40ms delay time.

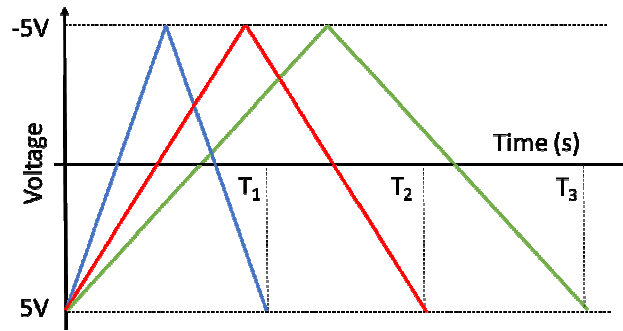


Figure 5: Schematic of the triangular large signal, applied to the gate of the device.

3.2. Large signal versus sweep voltage measurements

The I_D - V_G and I_G - V_G curves for the static sweep and transient measurements are illustrated in Fig.6. Although, the produced drain current curves have similar response for strong inversion or accumulation, a deviation on the subthreshold slope on the holes current can be observed. This behaviour can be attributed to the charging/discharging of slow traps which might be different in the two experiments because the evolution of the voltage is not done the same way, even if the total scan time is the same. For the sweep measurements, the voltage variation is done step by step while V_G is ramped with shorter voltage intervals for the transient ones. Also, the hysteresis effect on the electrons side between forward and reverse directions vanishes. On the other hand, gate current in I_G - V_G curves has significant higher values for the whole V_G scanning range in transient measurements and the peak of I_G shifts towards inversion/accumulation. The stronger signature on the transient I_G can be assigned to (i) the shorter voltage intervals that are applied to the gate in the transient measurements and (ii) the averaging of several measurement points in static (DC) experiments which reduce the dynamic response.

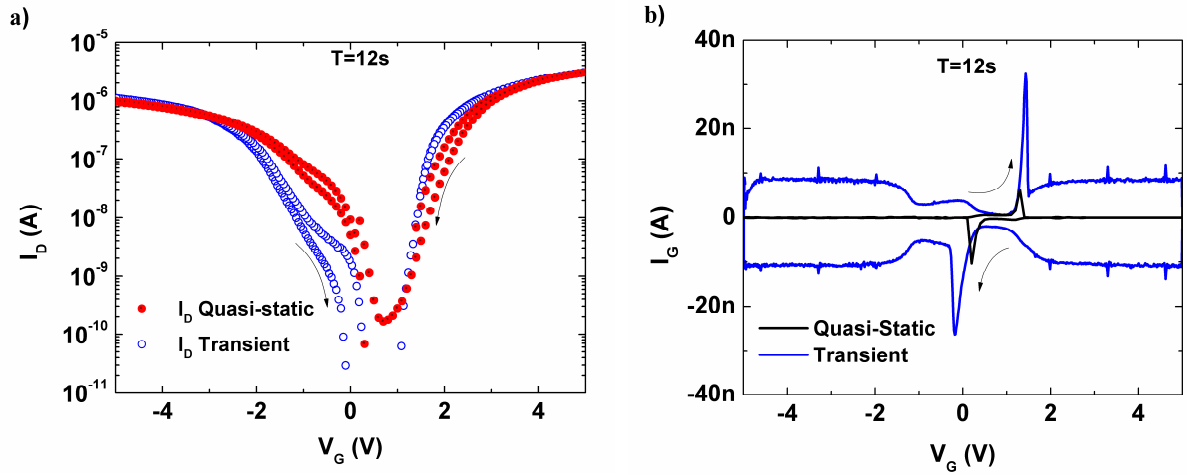


Figure 6: a) I_D - V_G (red full and blue empty symbols) and b) I_G - V_G (black and blue lines) for static and transient measurements. Scanning speed $SS \approx 1.667V/s$ and drain voltage $V_D = 0.1V$.

3.3 Transient effects on the drain current

To investigate the limit for which the transient phenomena do not affect drastically the drain current characteristics, we traced them for various scanning speeds. The respective curves are illustrated in Fig.7a for the forward scanning direction and in Fig.7b for the reverse. The effect of scanning speed in the I_D - V_G characteristics has a significant impact for scanning speeds greater than $SS=20V/s$. Additionally, hysteresis effects are noticed between the two scanning directions. A similar hysteresis has been reported for silicon [15] and SiC MOSFETs [16] and was associated with the threshold voltage variation due to the charging of traps during V_G scans. In order to check if this explanation applies here, we simulated the I_D - V_G curves in a NP-NP structure with surface traps at the Si/BOX interface (Fig.8). The traps density was $D_{it}=2 \cdot 10^{11} eV^{-1} cm^{-2}$ and they follow a Gaussian distributions located at 0.35eV from the valance/conduction band for donors/acceptors, as used [14] or recommended in the literature [17,18]. The simulated results show a shift in the subthreshold slope for increasing scanning speed. However, we cannot explain the experimental curve behaviour only with the

effect of D_{it} . The transient behaviour of the traps is, most likely, screened by other transient effects which originate from capacitive phenomena evidenced by the gate current transient response in the next section.

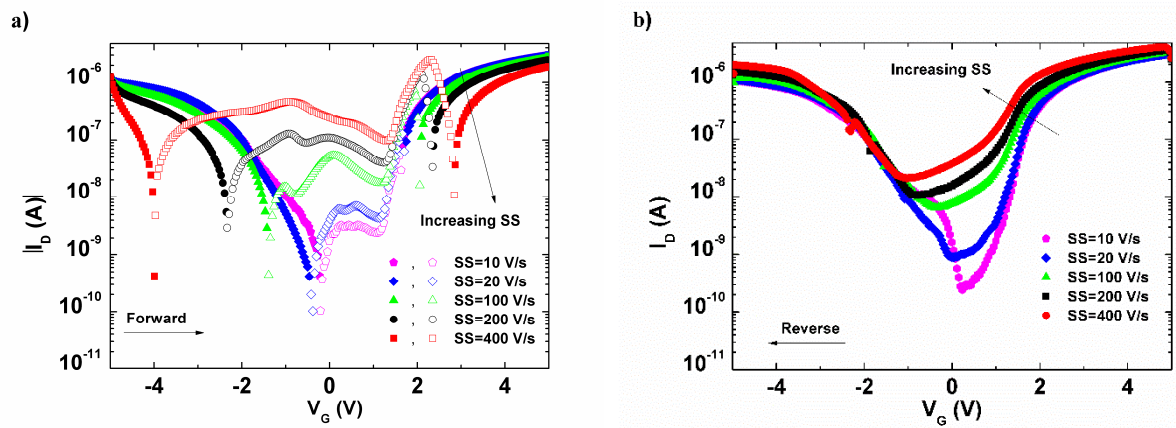


Figure 7: Measured absolute I_D (empty symbols correspond to negative values) with respect to V_G for various scanning speeds. a) scanning from accumulation to inversion and b) from inversion to accumulation.

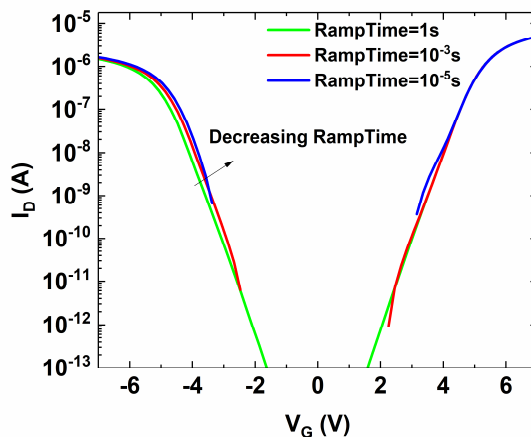


Figure 8: Simulated I_D - V_G curves for NP-NP structure with interface traps between the BOX and the film for various transient simulation times.

3.4 Transient effects on the gate current: experiments and simulations

Fig.9 presents two I_G - V_G curves for various scanning speeds. The shape of the gate current shows two different elements: a plateau current and a peak. The plateau current appears in strong inversion and accumulation and decreases in the depletion region. This is related to the total capacitance that drops significantly in the depletion region [19]. The peak

in Fig.9 is the result of a displacement current which is imposed by the lack of carriers in the transition from depletion to strong inversion/accumulation. Due to the opposite carrier types needed in the two different scanning directions, the peak is positive for a forward scan and negative for the reverse.

Comparing to “static-like” measurements, a significant increase in the maximum value of I_G peak value is noticed. Additionally, the peak shifts to higher V_G values for increasing scanning speed. Considering the dynamic character of this phenomenon, the increment in I_G peak value was foreseen. In the silicon film, during the transition from depletion to inversion (or accumulation), the total device capacitance increases and so does the need for carriers to charge/discharge the BOX capacitance. Since the total carrier density to reach equilibrium is constant [8], the increase in scanning speed induces a higher I_G . Indeed, as the scanning speed increases, we notice an increase in the gate current value. This evolution of the plateau current with the scanning speed can be explained by the displacement current which is equal to the product of a capacitance and the derivative of the voltage with respect to time. In strong inversion/accumulation the capacitance is constant and given by the BOX capacitance. As a result, I_G plateau current increases linearly with the scanning speed.

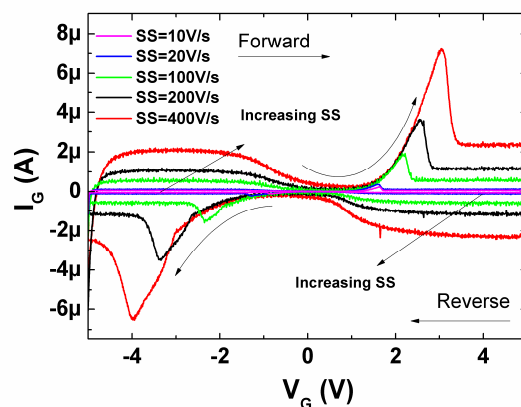


Figure 9: Experimental transient gate current versus gate voltage characteristics for various scanning speeds.

Simulations with the NP-NP structure have also been performed in similar conditions for the forward scan direction. In simulations, the scanning range was set from -10V to 10V, in order to confirm the area of interest. The scanning time was adjusted accordingly to maintain the same scanning speeds as in the experiments. The contact length for those simulations was set to $L_{con}=0.5\mu m$. It is worth noting that since no V_D is applied here and the effects are related to charging of the BOX capacitance, L_{con} was not kept at $0.1\mu m$ as in the static simulations but was chosen to give strong out-of-equilibrium signatures. The results are presented in Fig.10a. Although they follow the same trends as the experimental curves in Fig.9, the current values are significantly lower. Considering that all the above mentioned phenomena are related to the total BOX capacitance, they will be impacted by the area of the simulated structure which is different from the actual size of the configuration. To verify this assumption, we proceed to a normalization of the current with respect to the total area of the device in both experiments and simulations. The normalized I_G current (I_G density) is presented in Fig10b. The comparison between the measurements and simulations of I_G are almost perfectly matched, besides the position of the I_G maximum value.

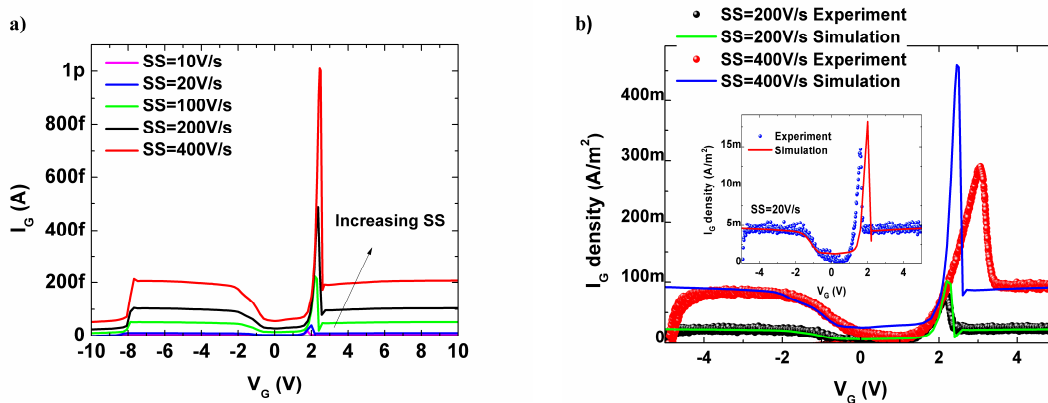


Figure 10: a) Simulated I_G - V_G curves for various scanning speeds using the NP-NP structure scanning from accumulation to inversion b) Comparison between experimental curves and simulated I_G density.

However, the total area of the device is not the only difference between the experiments and the simulations. The length of the contacts with respect to the channel length

is also different and might affect the simulated results. To further investigate its possible role on the maximum I_G value, simulations of various contact lengths and areas have been performed. The total area of the simulated device equals to the product of its total length by its width (set at $1\mu\text{m}$ in the simulator). The results are shown in Fig.11 and reveal that the increase of the I_G maximum value and position has a strong dependence on the contact size. Larger contacts result in higher I_G maximum values. This is an indication that the maximum value might depend on the ability of the carriers to be injected in the film. In the case of $L_{\text{con}}=0.1\mu\text{m}$, the highly doped silicon regions cannot provide the complete amount of carriers needed for the capacitance charge or create the necessary barrier, hence the I_G peak is not present. For larger contacts, the I_G peak occurs as in the experiments. When the contact size increases, the interface between the highly doped regions and the silicon film increases. If the area is sufficient, the simulated contacts are able to provide the carriers or create the barrier and the peak increases.

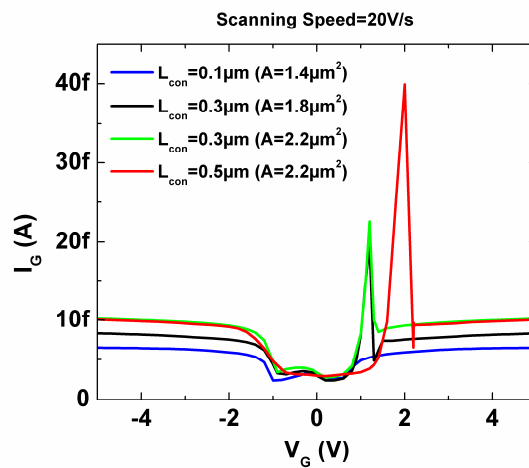


Figure 11: Simulated I_G - V_G curves for NP-NP structure for various contact sizes and areas.

The capacitive effects are connected to the geometry of the device. The large area of the SOI mesas used experimentally induces capacitive effects that affect significantly the device performance when the scanning speed is sufficiently high. This is evidenced in Fig.7 with the deformation of the I_D - V_G curves which, in strong inversion/accumulation, have comparable values as the capacitive induced current. Moreover, the dynamic character of the

I_G current indicates analogous behaviour to other out-of-equilibrium phenomena which are related to the body potential response, that are shown in the next section.

3.5 Transient out-of-equilibrium body potential measurements

The connection of the I_G displacement term with the out-of-equilibrium body potential (V_B) is well defined in FD MOSFETs [9]:

$$\frac{I_G}{C} = \frac{\Delta(V_G - V_B)}{\Delta t}$$

$$\frac{\Delta V_B}{\Delta t} = \frac{\Delta V_G}{\Delta t} - \frac{I_G}{C}$$

$$I_G \propto -\frac{\Delta V_B}{\Delta t} \quad (1)$$

where C is an adjusting capacitive coefficient. In the pseudo-MOSFET configuration, the V_B response under quasi-static measurements is documented [8] and was monitored through a third probe placed halfway between the source and drain probes. In accumulation and inversion regimes, the body voltage is simply halfway between the source and drain voltage, hence $V_B = V_D/2$ since source is grounded. In the depletion region, if V_G is scanned fast between accumulation and inversion, the carriers are lacking and V_B varies.

The measurement of the body potential in the depletion region is complex because the experimental configuration has a high impedance value of $Z \approx 10^9 \Omega$ at 40Hz [20]. Additionally, the RSU (Remote-sense and Switch Unit) of the B1530A cannot be used as a current source and impose a zero current to the body probe which would be necessary for an accurate V_B measurement. The modification of the experimental set-up was a necessary step to overcome the above drawbacks (see Fig.12). An arbitrary waveform pulse generator (Agilent 33250A) was used to impose the large triangular signal. As demonstrated in [8], the drain electrode is not mandatory for the observation of V_B , but in order to mimic the static measurements, an external power supply (Agilent E3642A) was biasing the drain at

$V_D=0.1V$. The V_B probe was connected to the input of a voltage follower, which is a unity-gain amplifying circuit with a high input impedance. The circuit was built using a TL081 operational amplifier with its inverting input connected to its output. The monitoring of the signals was performed with an oscilloscope (LeCroy Wafesurfer 424). The same scanning speed signals as in transient measurements were applied and a slow measurement was included to benchmark the new set-up with a quasi-static measurement.

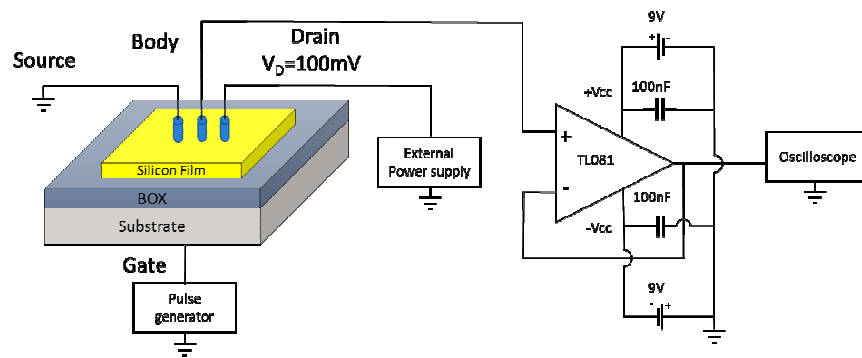


Figure 12: Experimental configuration for the measurement of the transient body potential.

Fig.13 shows the comparison of the V_B response between transient and sweep measurements along with the static (sweep) I_D current. The V_B signatures superpose well into the accumulation/inversion regimes, with a value of $V_D/2$. For the forward scan, there is a small shoulder appearing in the new configuration. Additionally, the reverse V_B peak increases slightly. The body potential drop also shifts towards inversion or accumulation. That was actually expected because as shown by eq.(1), the body potential drop is linked to the maximum value of I_G . In Fig.6b the measured I_G peak is shifted also towards accumulation/inversion, when moving from static to transient measurements. The shift in the V_B drop is consistent to the above mentioned result and is an additional argument for the validation of the experimental set-up.

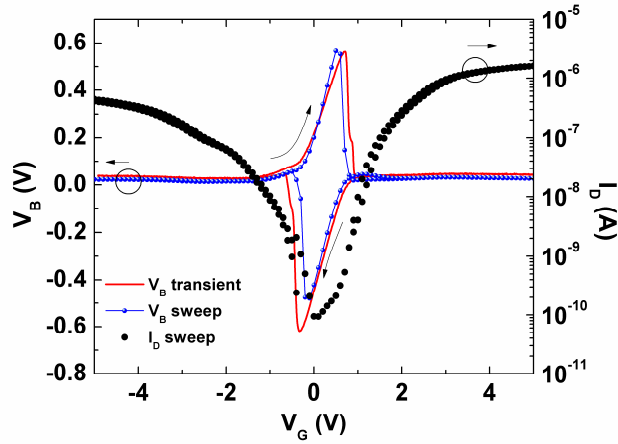


Figure 13: V_B versus V_G (red line for transient and blue line and symbols for static “static-like” measurements respectively) and I_D versus V_G (black symbols) characteristics. Transient $SS=0.416\text{V/s}$, equivalent sweep period $T=24\text{s}$.

The evolution of the transient measurements body potential for various scanning speeds can be seen in Fig.14. The response of V_B is stronger as the scanning speed increases. Similarly to the above analysis, we notice the V_B drop shift which is in agreement with the shift in I_G from Fig.6b. The small V_B oscillations on the linear part of the V_B curve (V_G between -1V and 1V) are caused by the data treatment used to filter a part of the measurement noise due to lack of electromagnetic isolation (see Appendix B for some examples of the detailed calculations). Note that the shoulder seen in Fig.14 is increasing for higher scanning speed, for both scanning directions.

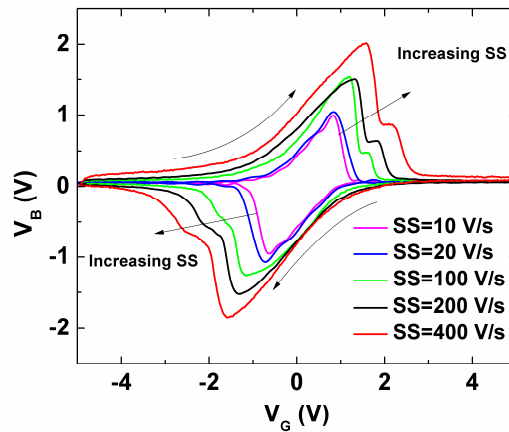


Figure 14: Measured transient V_B versus V_G curves for various scanning speeds. $V_D=0.1\text{V}$.

3.6. Out-of-equilibrium body potential simulations

V_B measurements can be done with a third probe between source and drain in a three probe configuration, but also in a two probe configuration with one probe grounded and the second one for the V_B measurement [8]. In the simulation environment, adding a third probe between source and drain induces an extra barrier for the carriers in 2D. Therefore, we used the drain contact to perform the body potential measurement. The electrode condition in the simulator was set to zero current. The evolution of $V_B(V_G)$ with the scanning speed in the simulation (Fig.15) reproduces well the behaviour of the experimental data. The derivative of the simulated body potential with respect to time step (Fig16.a) validates the connection between I_G and V_B in the transient simulation of the pseudo-MOSFET as stated by equation (1). Plotting the transient body potential in a log scale (Fig16.b) reveals that the injection of the carriers to return to equilibrium occurs in two steps. The first step drop of V_B (around $V_G=2V$) is connected to the injection of the appropriate type of carriers for C_{BOX} charging, as we discussed earlier. The second part of the drop shows an exponential decrease with V_G which is compatible with the exponential increase of the inversion charge versus the gate voltage.

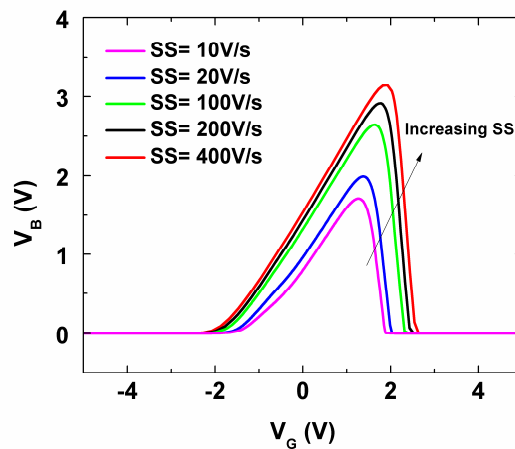


Figure 15: Simulated body potential with respect to gate voltage and for various scanning speeds.

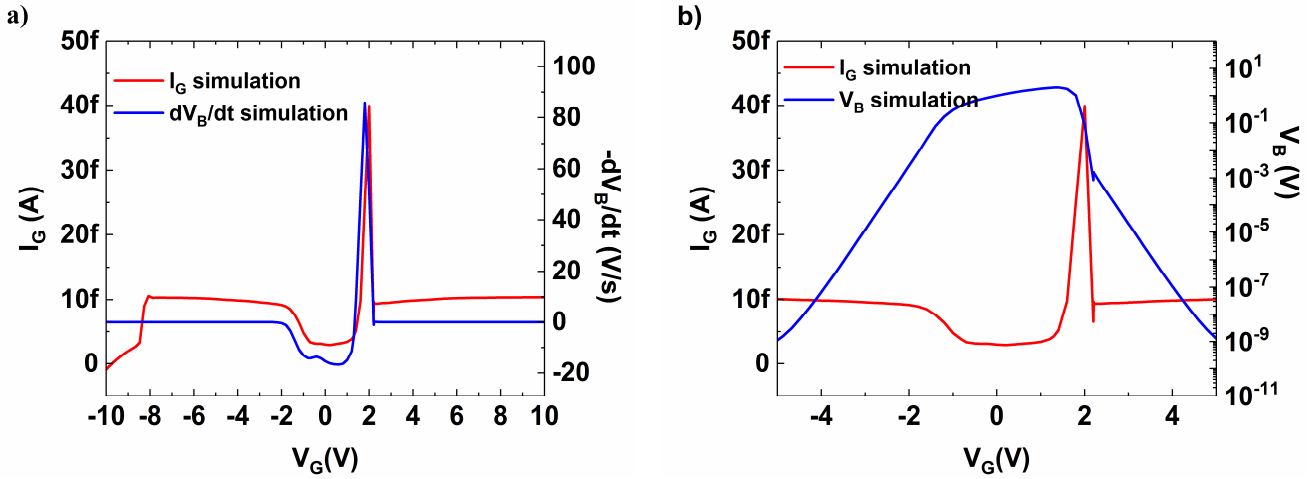
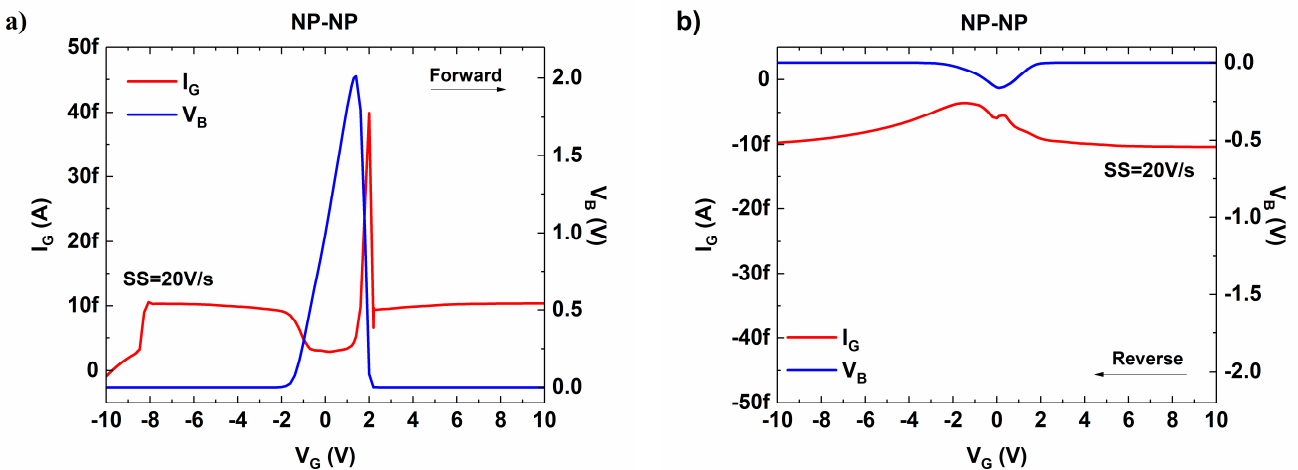


Figure 16: a) Simulated I_G and derivative of V_B b) Simulated I_G and V_B in log scale for $SS=20V/s$ produced by NP-NP structure scanning from accumulation to inversion

V_B and I_G peaks in the reverse scan can be reproduced by the simulations as well (Fig.17) but, it is the PN-PN structure that must be used in this case. Indeed, the forward behaviour is well reproduced by the NP-NP and the reverse needs the PN-PN structure (Fig.17). V_B is probed on the right electrode in both cases. This outcome is connected to the nature of the simulation. Different carrier types would be injected from different probes according to the device conditions. By setting the boundary condition of zero current to one of the probes in the simulation, the carrier injection is blocked through the probe (due to electrode conditions in the simulation). Thus, only one scanning direction can be reproduced per structure.



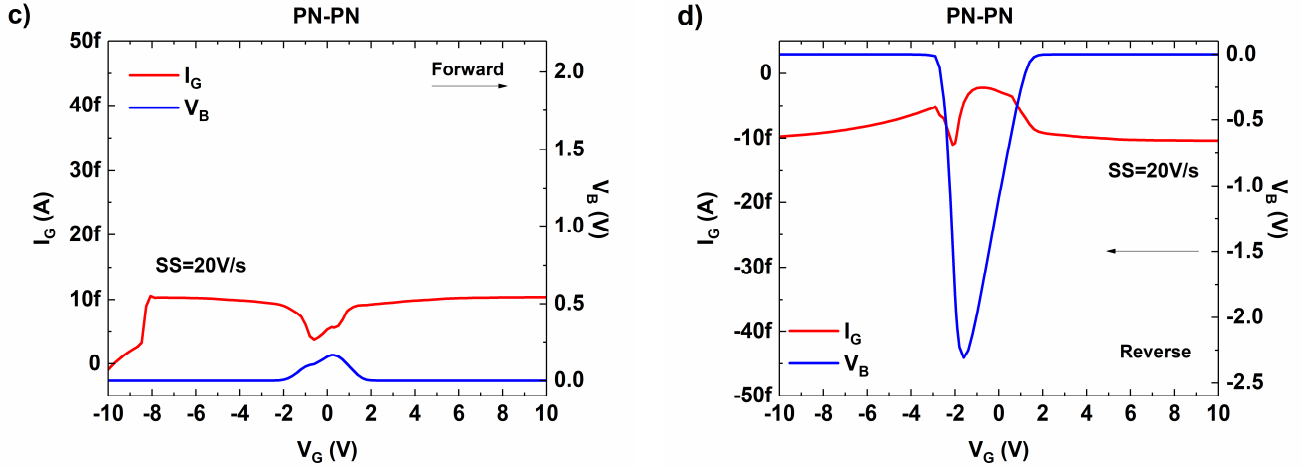


Figure 17: Simulated I_G and of V_B versus V_G for a) NP-NP structure scanning from accumulation to inversion b) NP-NP structure scanning from inversion to accumulation c) PN-PN structure scanning from accumulation to inversion d) PN-PN structure scanning from inversion to accumulation. Simulation ramp time=1s.

4. Conclusion

We propose a novel approach to simulate the pseudo-MOS configuration with a single structure that works from accumulation to strong inversion. Its validity was highlighted by a direct comparison to sweep and transient measurements. The new structure emulates the experimental configuration with the controlled pressure probes by combining N^+ and P^+ regions for each source/drain electrodes. It is capable of reproducing the out-of-equilibrium phenomena with good agreement with the experiments, even if the actual experimental configuration is rather 3D than 2D as in the simulations. However, the order of the N^+ and P^+ regions has to be modified to successfully reproduce the results for scanning from accumulation to inversion or the opposite. All the observed phenomena in the different experiments are reproduced, starting from I_D in ohmic regime (low V_D), to I_G and to the transient body potential.

In transient measurements, the drain current in the pseudo-MOSFET configuration can be described as the sum of two components, static and transient. The transient starts to affect the static-like curves for scanning speeds higher than 20V/s. The effect on the drain

current versus gate voltage curves that is visible over this limit, is actually the result of the strong capacitive induced gate current, which in this configuration has a really high value due to the large device area. For a strong transient character (high scanning speeds), I_G is comparable to the ON-current. Therefore, the deformation of I_D is strong. The plateau gate current in equilibrium regimes is **induced** by the BOX capacitance and the respective peak originates from its charging with the appropriate type of carriers.

The out-of-equilibrium phenomena are enhanced by the dynamic character of the transient measurements although special equipment and treatment is needed to observe their behaviour, especially for the transient body potential. The high impedance of the configuration in the depletion region requires a high input impedance circuit to measure V_B properly.

Finally, the transition from quasi-static to transient measurements was established. All the experimental results are reproduced by the simulation and the connection between the gate current and the body potential is validated.

Acknowledgments

Authors would like to thank SOITEC for providing the wafers and inspiring conversations.

Appendix A: Response of the emulated contacts through I_D - V_D characteristics

The simulated I_D - V_G curves in section 2.2 showed that the alternating-doping contacts (PN-PN or NP-NP) are the most appropriate ones. In order to further assess the behaviour of the emulated probes, drain current versus drain voltage I_D - V_D simulated curves are benchmarked with the experimental ones. In Fig.A1, the experimental I_D - V_D curves show a linear behaviour for low V_D . For $V_G=5V$, the appearance of the onset of the saturation is noticeable for high V_D values. The increase of V_G enhances the inversion charge and induces a higher I_D .

We simulated I_D - V_D for the two alternating combinations of contacts NP-NP (Fig.A2) and PN-PN (Fig.A3) under two bias conditions: $V_G=5V$ (corresponding to the subthreshold regime) and $V_G=8V$ (corresponding to strong inversion). The contact length (L_{con}) was added as a supplementary parameter.

The smallest contacts ($L_{con}=0.1\mu m$), give a linear behaviour in I_D - V_D curves, in every case. As the contact size increases the deviation from the linearity is more evident especially for lower gate voltage ($V_G=5V$). Short contacts have similar response to the experiments. This can be related to the ratio between the total area of the contacts and of the silicon island. Indeed, the size of the contact in the experimental configuration is several orders of magnitude smaller compared to the total size of the device (about $30\mu m$ diameter of contact for $5mm$ side of silicon). In the case of the large simulated contacts, the length of the contacts is almost half of the total device length. Additionally in the 2D simulation, the profile of the device is the same on the full width of the device but in experimental conditions, the current density surrounds the contact [13]. A more appropriate approach could be the 3D simulations which are more complex. However, since the 2D simulation with these structures reproduce well the experimental results, we use them in this paper for the proof of concept of the transient signatures.

Although, the short contacts mimic well the I_D - V_D characteristics under quasi-static conditions, larger contacts enhance the transient response as shown in section 3.4. A fully quantitative study would require a fine tuning of the structure which is not the purpose here. Consequently we studied the dynamic phenomena with higher L_{con} in order to amplify the out-of-equilibrium responses.

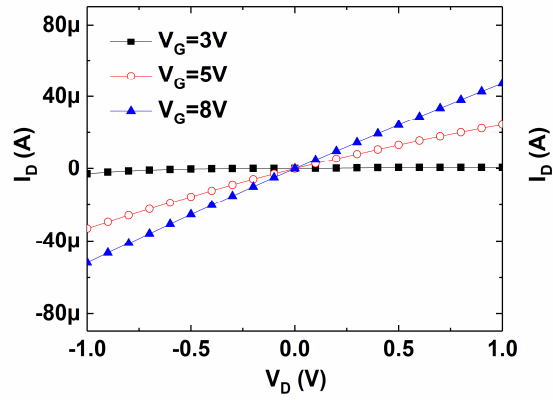


Figure A1: Experimental I_D - V_D characteristics for three positive V_G biases.

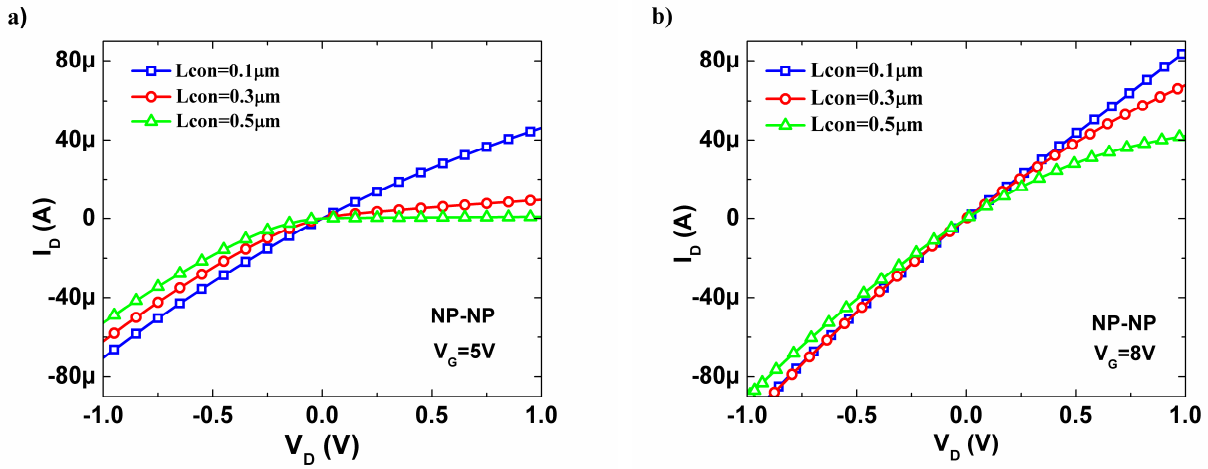


Figure A2: I_D - V_D characteristics reproduced with NP-NP structure for a) $V_G=5V$ and a) $V_G=8V$ for three contact lengths.

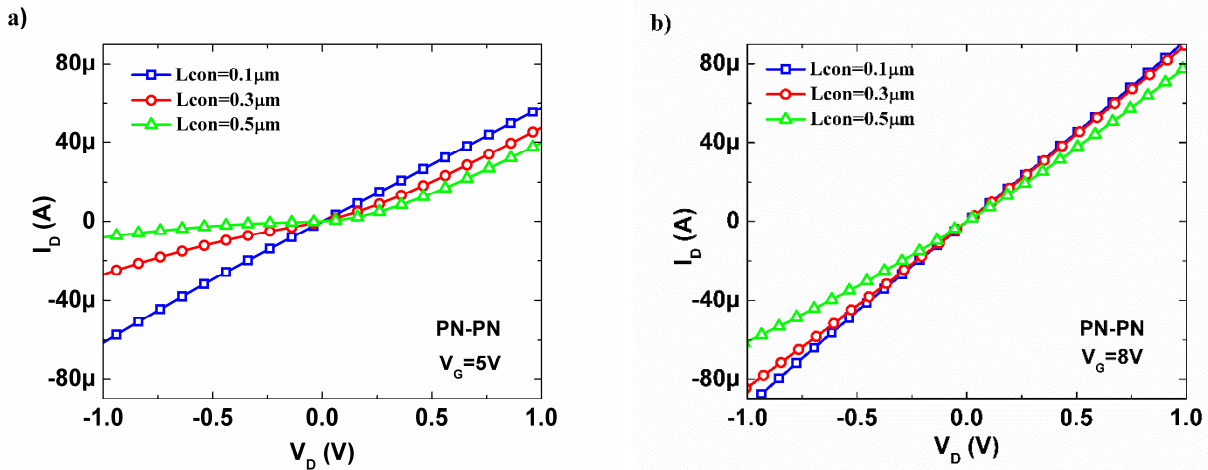


Figure A3: I_D - V_D characteristics reproduced with PN-PN structure for a) $V_G=5V$ and a) $V_G=8V$ for three contact lengths.

Appendix B: Data treatment

Fig.B1, B2, B3 are illustrating the fast Fourier transform (FFT) filtering treatment for a slow ($T=24s$), medium ($T=2s$) and fast ($T=0.05s$) scans of the back-gate voltage in transient

measurements (Fig.14). As already mentioned, the “home-made” reading circuit is vulnerable to environmental noise and to the 50Hz harmonic. To illustrate this clearly, we present the magnitude of the FFT on the frequency domain (Fig. B1a, B2a, B3a). For the slow scanning speeds an isolation of the harmonic by blocking frequencies between 25Hz and 75Hz results in a clear imprint of the body potential in the depletion region. However, high frequency noise is still present. An increase in the range of frequencies that are blocked results in a clean representation of the monitored signal. The most interesting case correspond to the medium frequency, Fig. B2. In this situation, during the linear increase in V_B , several periods of the 50Hz noise are present. This becomes clear from Fig. B2a. Since, the frequencies of the output are comparable to the harmonic, a proper isolation of it is not feasible. Lastly, when the scanning speed is sufficiently high, the monitored signal has a frequency close to 50Hz so, the 50Hz no longer appears independently in the Fig.B3a. To be consistent with the data treatment, a 6kHz low pass filtering was applied the raw experimental data with high scanning speed to exclude the high frequency noise.

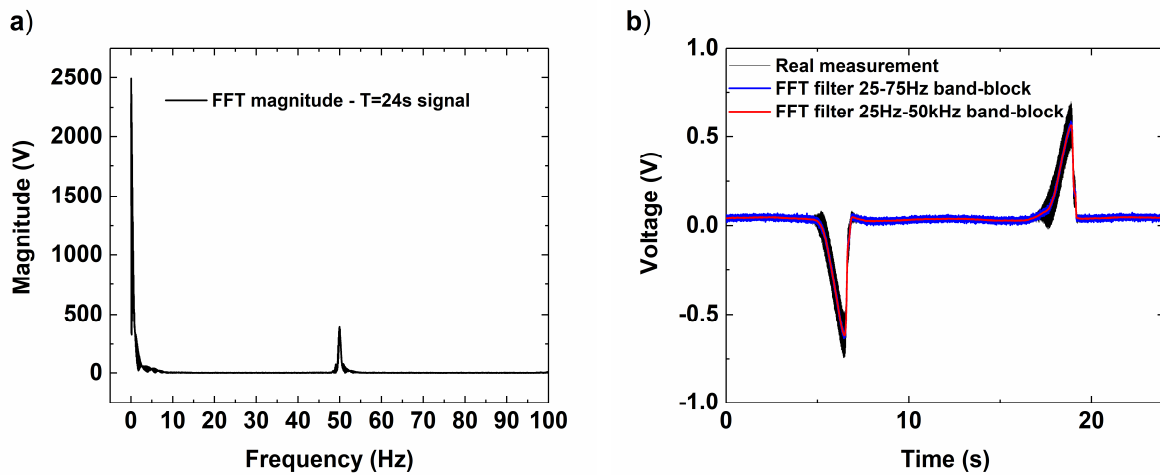


Figure B1: a) FFT magnitude in frequency domain. b) Measured V_B versus time and two signals treatments. Signal period $T=24s$.

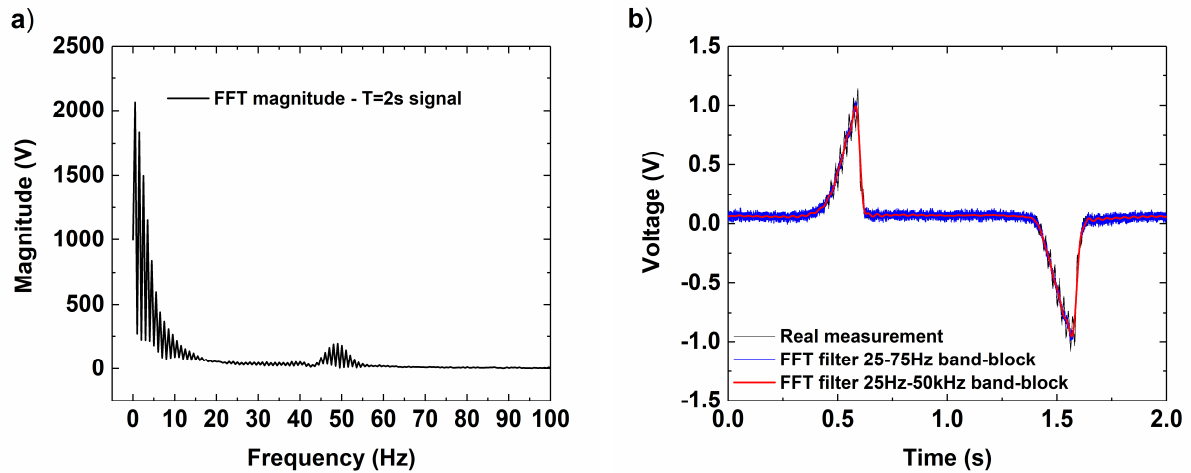


Figure B2: a) FFT magnitude in frequency domain. b) Measured V_B versus time and two signals treatments. Signal period $T=2s$.

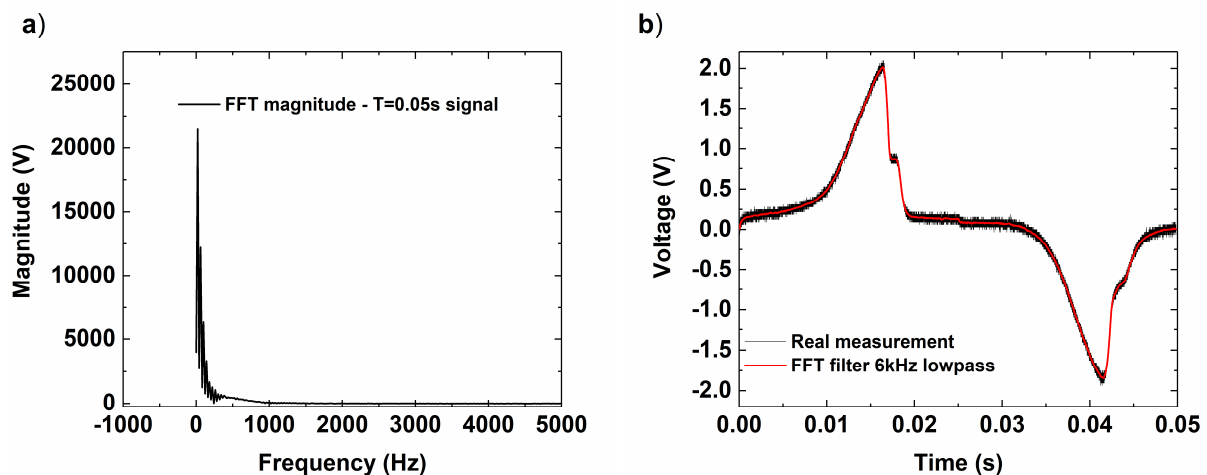


Figure B3: a) FFT magnitude in frequency domain. b) Measured V_B versus time and two signals treatments. Signal period $T=0.05s$.

References

- [1] Cristoloveanu S, Munteanu D, Liu MST. A review of the pseudo-MOS transistor in SOI wafers: operation, parameter extraction, and applications. *IEEE Transactions on Electron Devices* 2000;47:1018–27. doi:10.1109/16.841236.
- [2] Fernandez C, Rodriguez N, Marquez C, Ohata A, Allibert F. On the effective mobility extraction by point-contact techniques on silicon-on-insulator substrates. *Journal of Applied Physics* 2015;117:035707. doi:10.1063/1.4906123.
- [3] Pirro L, Ionica I, Ghibaudo G, Mescot X, Faraone L, Cristoloveanu S. Interface trap density evaluation on bare silicon-on-insulator wafers using the quasi-static capacitance technique. *Journal of Applied Physics* 2016;119:175702. doi:10.1063/1.4947498.
- [4] El Hajj Diab A, Ionica I, Cristoloveanu S, Allibert F, Bae YH, Chroboczek JA, et al. Low-frequency noise in SOI pseudo-MOSFET with pressure probes. *Microelectronic Engineering* 2011;88:1283–5. doi:10.1016/j.mee.2011.03.096.

- [5] Cristoloveanu S, Bawedin M, Ionica I. A review of electrical characterization techniques for ultrathin FDSOI materials and devices. *Solid-State Electronics* 2016;117:10–36. doi:10.1016/j.sse.2015.11.007.
- [6] Cristoloveanu S, Elewa T. Model for carrier lifetime extraction from pseudo-MOSFET transients. *Electronics Letters* 1996;32:2021–3. doi:10.1049/el:19961319.
- [7] Kang SG, Schroder DK. SOI bulk and surface generation properties measured with the pseudo-MOSFET. *IEEE Transactions on Electron Devices* 2002;49:1742–7. doi:10.1109/TED.2002.803639.
- [8] Benea L, Bawedin M, Delacour C, Ionica I. Out-of-equilibrium body potential measurements in pseudo-MOSFET for sensing applications. *Solid-State Electronics* 2018;143:69–76. doi:10.1016/j.sse.2017.11.010.
- [9] Bawedin M, Cristoloveanu S, Flandre D, Udrea F. Dynamic body potential variation in FD SOI MOSFETs operated in deep non-equilibrium regime: Model and applications. *Solid-State Electronics* 2010;54:104–14. doi:10.1016/j.sse.2009.12.004.
- [10] Benea L, Cerba T, Bawedin M, Delacour C, Cristoloveanu S, Ionica I. Nanoindentation effects on the electrical characterization in Ψ -MOSFET configuration. 2018 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS), 2018, p. 1–4. doi:10.1109/ULIS.2018.8354754.
- [11] Ionica I, Savin I, Van Den Daele W, Nguyen T, Mescot X, Cristoloveanu S. Characterization of silicon-on-insulator films with pseudo-metal-oxide-semiconductor field-effect transistor: Correlation between contact pressure, crater morphology, and series resistance. *Appl Phys Lett* 2009;94:012111. doi:10.1063/1.3030987.
- [12] Williams S, Cristoloveanu S, Campisi G. Point contact pseudo-metal/oxide/semiconductor transistor in as-grown silicon on insulator wafers. *Materials Science and Engineering: B* 1992;12:191–4. doi:10.1016/0921-5107(92)90284-G.
- [13] Munteanu D, Cristoloveanu S, Guichard E. Numerical simulation of the pseudo-MOSFET characterization technique. *Solid-State Electronics* 1999;43:547–54. doi:10.1016/S0038-1101(98)00293-7.
- [14] Van Den Daele W, Malaquin C, Baumel N, Kononchuk O, Cristoloveanu S. Adaptation of the pseudo-metal–oxide–semiconductor field effect transistor technique to ultrathin silicon–on–insulator wafers characterization: Improved set-up, measurement procedure, parameter extraction, and modeling. *Journal of Applied Physics* 2013;114:164502. doi:10.1063/1.4826631.
- [15] Shen C, Li M-, Wang XP, Yeo Y-C, Kwong D-. A fast measurement technique of MOSFET $I_{sub\ d}/V_{sub\ g}$ characteristics. *IEEE Electron Device Letters* 2006;27:55–7. doi:10.1109/LED.2005.861025.
- [16] Gurfinkel M, Xiong HD, Cheung KP, Suehle JS, Bernstein JB, Shapira Y, et al. Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques. *IEEE Transactions on Electron Devices* 2008;55:2004–12. doi:10.1109/TED.2008.926626.
- [17] Broqvist P, Alkauskas A, Pasquarello A. Defect levels of dangling bonds in silicon and germanium through hybrid functionals. *Phys Rev B* 2008;78:075203. doi:10.1103/PhysRevB.78.075203.
- [18] Tsipas P, Dimoulas A. Modeling of negatively charged states at the Ge surface and interfaces. *Appl Phys Lett* 2009;94:012114. doi:10.1063/1.3068497.
- [19] Diab A, Ionica I, Ghibaudo G, Cristoloveanu S. RC Model for Frequency Dependence of Split C–V Measurements on Bare SOI Wafers. *IEEE Electron Device Letters* 2013;34:792–4. doi:10.1109/LED.2013.2257663.
- [20] Sato S, Ghibaudo G, Benea L, Ionica I, Omura Y, Cristoloveanu S. Impact of contact and channel resistance on the frequency-dependent capacitance and conductance of pseudo-MOSFET. *Solid-State Electronics* 2019. doi:10.1016/j.sse.2019.03.059.