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Circuit Design using Schmitt Trigger to Reliability Improvement

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Abstract – This paper presents a design strategy to reduce the impact of process variations and soft error susceptibility in FinFET circuits. The mitigation is provided by connecting a Schmitt Trigger at the logic gate output. The improvements in power and delay variability can reach up to 32.6% and 42.1%, respectively, with logic cells almost immune to soft error even at the near-threshold regime. When compared with other circuit-level methods such as sleep transistor, decoupling cells, and transistor reordering, on average, the Schmitt Trigger technique is at least 6%, 8%, and 10.5% more robust to process variability, respectively.

1. Introduction

The electronic devices are approaching the size of atoms, imposing the creation of new guidelines to deal with the challenges in sub-22nm designs. Process variability mitigation and radiation hardness are relevant reliability requirements as the chip manufacturing advances in-depth into the nanometer regime. Integrated circuits under process variability effects can fail to meet some performance or power criteria that lead to the parametric yield loss as well as demand several redesign steps [1]. Traditionally, the soft errors (SE) arise from the interaction between energetic particles coming from space or terrestrial radiations with the silicon [2]. However, the technology scaling introduces the charge sharing phenomenon and pulse quenching [3]. Moreover, the process variations can alter the linear energy transfer (LET) to induce a soft error. The consequences are temporary data loss, inducing to the critical failures on system behavior even at the ground level.

Both industry and academy are pursuing novel materials, structures, devices, and design strategies to be implemented in the mainstream circuit to meet these demands and avoid unwanted effects. The debate on which of them is the best way is still open, but potential alternatives need to be pointed out and should be well investigated. Although very efficient, techniques related to the fabrication changes have an expensive cost and high complexity involved. In this context, this work explores the Schmitt Trigger circuit to ensure more reliable FinFET logic cells, highlighting all pros and cons of adopting it. Furthermore, the comparison with three other circuit-level techniques called transistor reordering, decoupling cells, and sleep transistor [4-7] will be provided in this paper.

2. Evaluation Methodology

The mitigation strategy consists in connecting a Schmitt Trigger in the cell output, as shown in Fig. 1 (a), using the topology proposed by [8]. Schmitt Triggers have an inherent hysteresis property used to enhance signal stability and noise immunity. The P_F and N_F devices provide a feedback scheme that increases the I_{ON} -to- I_{OFF} ratio, minimizing the output

degradation. The shift on voltage transfer curve due to process variation is reduced using Schmitt Trigger due the strong influence of gate-source voltage of the inner transistors (N_1 and P_1) over the switching point, as shown in Fig. 1 (b). Moreover, the Schmitt Trigger circuit increases the capacitance of the output node, reducing the critical charge to generate a SE.

Fig. 2 shows all steps of this work. First, all the design flow was performed with the traditional version of logic cells. After, the Schmitt Trigger circuit was connected in each FinFET logic cell. This paper adopts a 7-nm FinFET process design kit (PDK) developed by ASU in partnership with ARM Ltd for academic use [9], called ASAP7. A summary of device parameters and layout layers from ASAP7 can be seen at Table I. All layouts are submitted to the verification flow, and the parasitic extraction, and the Schmitt Trigger layout can be seen in Fig. 1 (c). The experiments consider the same sizing for all transistors of logic cells (three fins). The impact of transistor sizing is only explored in the extra transistors imposed by Schmitt Trigger technique.

The work-function fluctuations (WFF) cause the major deviation in the circuit behavior in FinFET technologies [10]. Process variability is inserted by 2000 Monte Carlo simulations [11] with the WF parameter modeled as a Gaussian function with 3σ of deviation, which represents 99.7% of the normal distribution curve. The logic cells were submitted to high (5%), medium (3%), and low (2%) levels of WF variation due to the lack of information from industry about these values in current FinFET nodes. The normalized standard deviation (σ/μ) is used to indicate the gate sensitivity against process variation. The deviation on power and delay due to the impact of process variations are denominated as power and delay variability in this work, respectively.

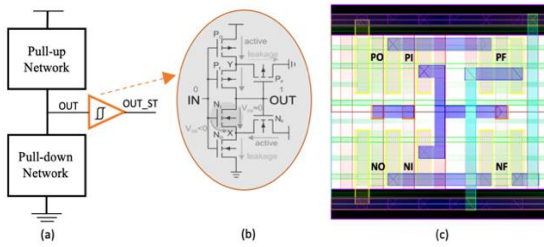


Fig. 1 Generic representation of the technique application (a), Schmitt Trigger schematic (b) and layout with three fins (c)

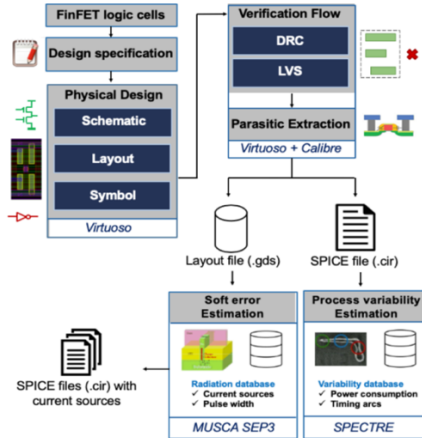


Fig. 2 Complete design flow used in this work

Table I. Device parameters and layout layers from ASAP7

Device Parameters		Layout Layers (nm)	
Gate length	21nm	Width	Pitch
Fin thickness	6.5nm	Fin	6.5 27
Fin height	32nm	Active	54 108
Oxide thickness	2.1nm	Gate	21 54
Channel doping	$1 \times 10^{22} \text{ m}^{-3}$	SDT/LISD	25 54
S/D doping	$2 \times 10^{26} \text{ m}^{-3}$	LIG	16 54
Work- NFET	4.3720eV	VIA0-3	18 25
Function PFET	4.8108eV	M1-M3	18 36

The SE susceptibility of logic cells is estimated with the MUSCA SEP3 tool developed by ONERA [12]. MUSCA SEP3 is a radiation event generator tool, also based on the Monte Carlo method, which models from the strike of an energetic particle into the matter until the manifestation of a transient pulse. The current sources include internal and external nodes considering the most vulnerable input vector of logic cells. The collection charge of each transistor is calculated from a reverse engineering or using front-end-of-line (FEOL) report from the GDSII file. All the electrical properties of devices also are considered by this tool. This work simulates heavy ion irradiation at normal angle of incidence, and room temperature (27°C).

The 3D structure of FinFET devices reduces the volume of silicon exposed to a charge collection mechanism decreasing the SE susceptibility [13]. FinFET devices are immune to soft error in the voltage interval from 0.7V to 0.5V using ASAP7 PDK. However, technology scaling increases the number of portable devices powered by a battery [14]. The demand for ultra-low power applications points out the need for methods to minimize consumption like the voltage scaling, but low

voltages make the circuits more susceptible to radiation effects. For this reason, this paper evaluates the SE into the near-threshold regime. The logic cells were evaluated under low LET, i.e., less than $15 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$, which corresponds to the representative secondary particles induced by proton or neutrons in avionics and ground applications. The SE susceptibility also was investigated under higher LET (30 to 58 $\text{MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$), representing the space environment. This work adopts the cross-section as the figure of merit to estimate the SE susceptibility of FinFET cells. A fault is detected if the voltage amplitude of the impacted node exceeds the gate threshold voltage ($V_{DD}/2$).

3. Reliability Improvement using Schmitt Triggers

The use of a Schmitt Trigger circuit in the design minimizes the impact of process variation on delay and power as shown in Fig. 3 and Fig. 4, respectively, for a set of FinFET cells under 5% of deviation from nominal conditions. Delay enhancements can reach 42.1% for the OAI211 logic cell. Even that the OAI21 is the less benefited cell to the use of Schmitt Trigger design, the gain is still significant, with an impact reduction of 21.6% on delay. On the other hand, the NAND2 cell had the minimum power improvement using a Schmitt Trigger design. A Schmitt Trigger design allowed a reduction of process variation impact on power around 19.3%. The most robust cell under process variations was the NOR4, with a gain of 32.6% on power.

Table II shows the tendency of delay variability mitigation when the logic cells were submitted to different levels of WF fluctuations. The average (AVG) of delay variability using a Schmitt Trigger design considering 2%, 3%, and 5% of WFF is around 9.17%, 14.23%, and 27.17%, respectively. The delta relation (Δ) specifies how much the sensitivity to the process variation changes when the logic cells are designed using an ST circuit instead of the standard version (std). Except for INV and NAND cells (highlighted in grey), the gain of an ST design increases as levels of WFF decreases. For example, if the AOI21 cell is submitted to 2%, 3%, or 5% levels of variation using an ST design, the impact on delay reduces in 36.4%, 31.6%, and 21.6%, respectively, if compared with the standard version. For the INV and NAND cells, the best mitigation results were achieved with 3% of variation from nominal conditions.

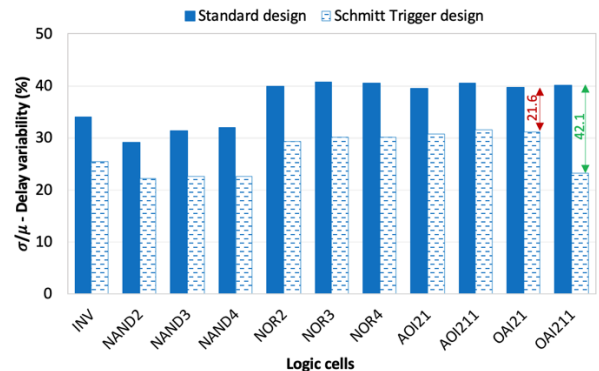


Fig. 3 Delay variability mitigation using a Schmitt Trigger

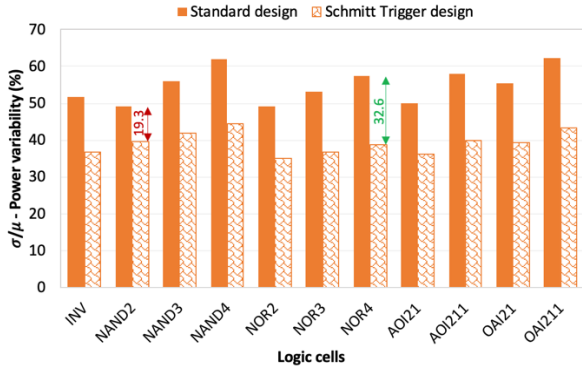


Fig. 4 Power variability mitigation using a Schmitt Trigger
Table II. Impact of different levels of WFF on delay

Logic Cells	2%			3%		
	σ/μ (%)		Δ (%)	σ/μ (%)		Δ (%)
	std	ST		std	ST	
INV	10.46	8.49	18.8	18.01	13.16	26.9
NAND2	9.25	7.93	14.3	15.93	12.21	23.4
NAND3	11.12	8.01	28.0	18.26	12.35	32.4
NAND4	12.45	8.03	35.5	19.44	12.38	36.3
NOR2	16.21	9.58	40.9	23.68	15.00	36.7
NOR3	18.06	9.96	44.9	24.70	15.51	37.2
NOR4	18.34	10.09	45.0	24.64	15.58	36.8
AOI21	15.83	9.96	37.1	23.10	15.60	32.5
AOI211	17.48	10.38	40.6	24.12	16.13	33.1
OAI21	15.97	10.16	36.4	23.25	15.91	31.6
OAI211	16.08	8.24	48.8	23.23	12.72	45.2
AVG	14.66	9.17	-	21.67	14.23	-

The power variability attenuation trend is the same for all logic cells investigated. The benefits of the Schmitt Trigger increase as levels of WFF also raises. Schmitt Trigger technique minimizes the power variability in 4.5%, 11%, and 19.3% of the NAND2 cell with 2%, 3%, and 5% levels of WF fluctuations, respectively, when compared with a standard design. The NAND2 and NOR4 continue to be the logic cells with less and more gains in power variability mitigation, respectively, even considering 2% and 3% level of variations.

The influence of a Schmitt Trigger design with different numbers of fins in the output of the AOI21 cell is shown in Fig. 5. Larger Schmitt Triggers decrease the impact on power variability considerably. For example, with process variations of 2%, 3%, and 5%, the use of a Schmitt Trigger with five fins improves the power variability in 23.2%, 22.8% and 10.8%, if compared with a layout with three fins, respectively. The increase of number of fins is more advantageous for circuits submitted to lower levels of WFF. On the other hand, larger Schmitt Triggers contributes less than 3% for delay variability mitigation, independently of the levels of WFF. The same behavior was observed for all the other logic cells investigated.

The SE susceptibility of NAND2, NOR2, and AOI21 cells was analyzed under low and high LETs, varying from 5 to 58 MeV.cm².mg⁻¹. Moreover, all input vectors were tested as well as the core voltage was modified until the near-threshold regime (0.3V). The results show that an ST design is very promising for soft error mitigation. The ST technique makes

the logic gates almost immune of faults, independently of LET, input vector, or core voltage applied in the design.

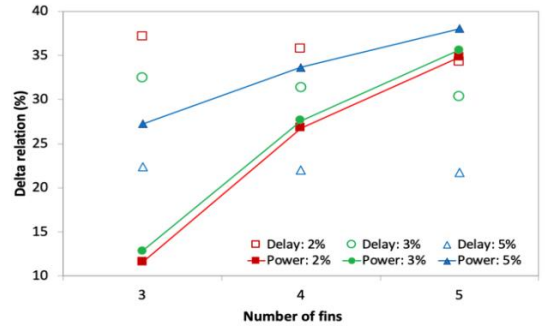


Fig. 5 Improvements in connecting a Schmitt Trigger with different number of fins in the output of AOI21 logic cell

4. Comparison with other circuit-level techniques

To the best of our knowledge, only a few works are focusing on circuit-level methods for increasing the robustness of FinFET circuits to soft errors and process variability [15-19]. A dual-interlocked logic demonstrates to be resilient to SET impact for even for dual-node strikes using a 14nm FinFET technology [15]. Three types of redundancy (spatial, temporal, and hybrid) were investigated in [16] to SET mitigation at near-threshold regime using a 16nm FinFET node. The multi-level design instead of complex cells was studied in [17] as a mitigation strategy using the 7nm FinFET technology. The replacement of traditional inverters by Schmitt Triggers significantly decreases the process variability sensitivity in FinFET full adders designed in 7nm FinFET node [18]. The SET robustness due to the low-pass filter and redundancy strategies was explored in [19], adopting a 10nm FinFET node.

Our previous works considered three approaches to reliability improvement: transistor reordering [4], the decoupling cells [5,6], and sleep transistor [7]. Transistor reordering consists of placing the serial transistors of a given network in different positions in the schematics keeping the same logic function. The adoption of decoupling cells in the circuit output is a capacitive approach to reduce the noise on signal lines and to increase the critical charge of the output node. The use of sleep transistor between the pull-down network and the ground rail is a power-gating technique which acts as a supply-voltage regulator.

The sensitivity of cells to 5% of WFF considering a standard version, a Schmitt Trigger design, and three other circuit-level mitigation methods [4-7] are compared in Fig. 6 and Fig. 7 for power and delay variability, respectively. The Schmitt Trigger design is at least 4.9% more efficient than the three other approaches to attenuate the impact on power consumption due to process variations. Transistor reordering was only applied for complex gates, with gains less than 2% to power variability.

There is no obvious pattern in the delay variability mitigation. Except for the AOI21 and OAI21 cells, the ST design is the best way to improve the delay variability. The maximum gain of the Schmitt Trigger design is around 19.4% and 14.6% when compared with sleep transistor and

decoupling cell designs, respectively. The use of a sleep transistor is better than decoupling cells for the NAND and OAI211 cells while the opposite happens for the INV, NOR, and AOI211 cells. The OAI211 is the only logic cell to present significant benefits with the transistor reordering method.

Fig. 8 and Fig. 9 compare the SET cross section of AOI21, NAND2 and NOR2 cells with different supply voltages for a LET of $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ and $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$, respectively. For all gates, it is only observed effects for voltages below

0.4V due to the 3D structure of FinFET devices. The AOI21 cell is the unique immune to soft errors at 0.4V under $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$. The NOR2 cell is around 21% more robust than NAND2 cell to soft error impact for both LETs at 0.3V. However, the opposite happens at 0.4V where the NAND2 gate becomes less susceptible to SE effects. The error bars are defined as one divided by the square root of the number of SETs representing the statistical error induced by Monte Carlo simulations.

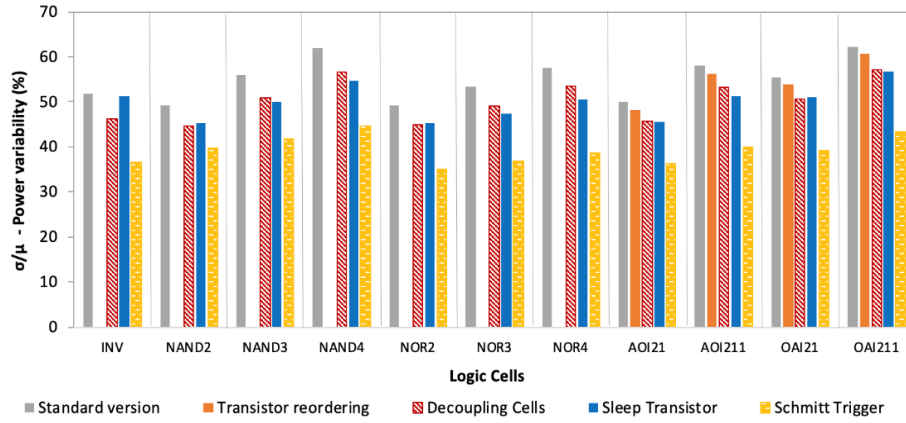


Fig. 6 Comparison of power variability using different circuit-level mitigation techniques

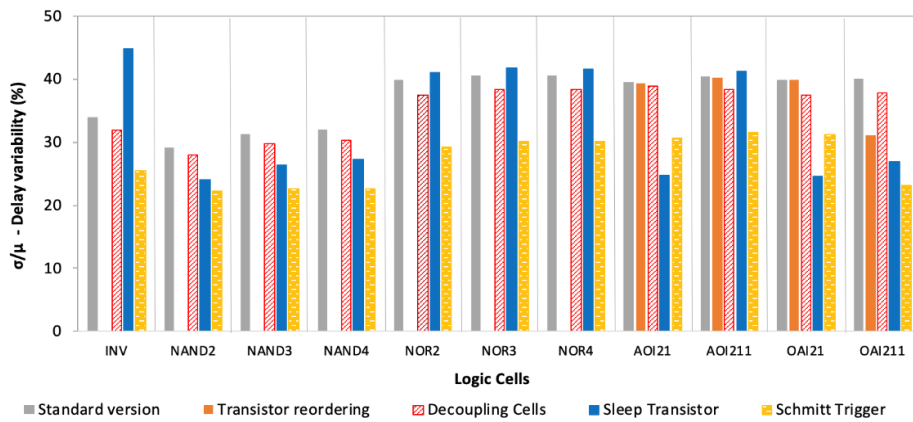


Fig. 7 Comparison of delay variability using different circuit-level mitigation technique

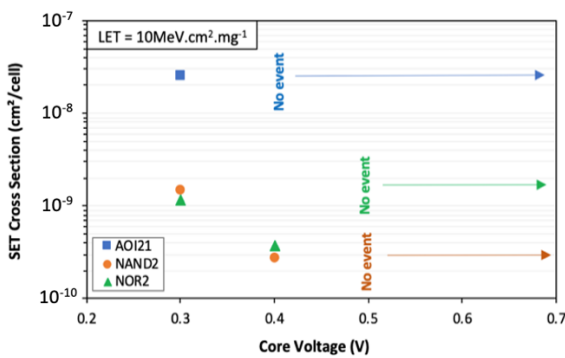


Fig. 8 SET cross section varying the core voltage with a LET = $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$

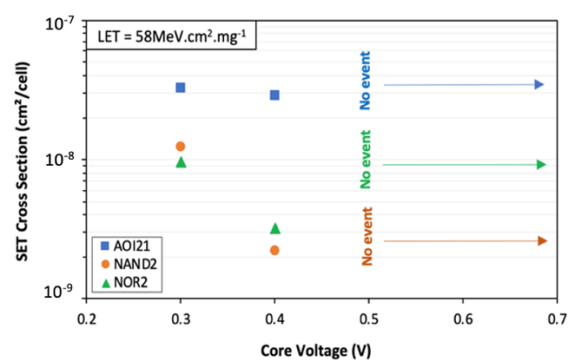


Fig. 9 SET cross section varying the core voltage with a LET = $58\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$

Considering that the AOI21 logic cell is the most susceptible to SE impact at near-threshold voltage (0.3V), Fig. 10 shows the SET cross section using three layout versions. The standard corresponds to a traditional design, without apply mitigation methods. The transistor reordering is not favorable to soft error attenuation, because increase the SE vulnerability. On the other hand, the decoupling cells reduces the soft error susceptibility around 23.7%, 19.8%, and 11.4% for LET equal to 20, 30, and 58MeV. $\text{cm}^2.\text{mg}^{-1}$, respectively. The design using a Schmitt Trigger or sleep transistor is immune to SE because no events were seen in the output of logic cells. For this reason, the results are not presented in Fig. 10.

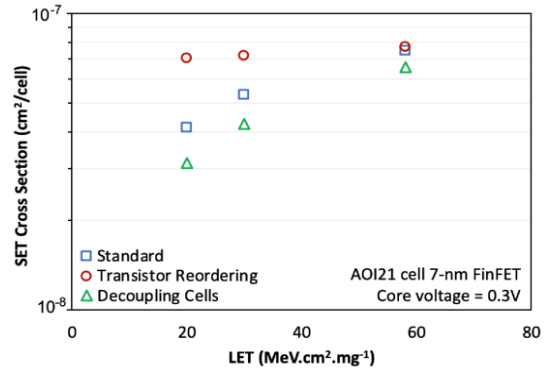


Fig. 10 Comparison of the soft error susceptibility using different designs and higher LET values

4.1. Technique Drawbacks

A Schmitt Trigger design is an interesting way to mitigate process variations and radiation-induced soft errors as presented in Section 3. However, this approach imposes a huge area, delay, and power penalties. Table III presents the area overhead for the Schmitt Trigger and the other approaches [4-7]. As the evaluated cells on the transistor reordering technique had three or four inputs, this work has no results about area for Transistor Reordering technique for one and two input functions indicating this condition with an (-) signal in Table III. The area of logic cells using a Schmitt Trigger with three fins can increase between 2.2x and 3.3x, depending on the number of inputs, as shown in Table III. Each fin added by the Schmitt Trigger design increases the area by 17.2%. Transistor reordering is the best technique because it has no area penalties compared with the standard circuits area.

The insertion of decoupling cells or Schmitt Trigger in the logic cell output introduces different number of extra transistors, but the area penalty for both is the same. This happens due to the limitations of ASAP7 PDK demanding more space to adjust each input of the transistors in cross-coupled mode. The use of a sleep transistor generates a small increase in the area of logic cells that vary from 1.2x to 1.8x in most of the cases. The diffusion break requires two dummy gates increasing the estimated area around 33% and 28% for OAI21 and OAI211 cells designed with sleep transistor, respectively.

The power and delay impact of these techniques compared with the Standard power and delay expected behaviour is presented in Fig. 11 for all logic cells, considering 5% of WFF deviation and extra transistors with three fins. The transistor reordering and the decoupling cells techniques introduced the smaller impacts on power consumption. On average, the impact is around 11% for transistor reordering, and 15% for the insertion of decoupling cells. Also, these two techniques show less dependence of the circuit logic and the power increase, with the power results concentrated in a same region of the Fig. 11. The smallest average impact on delay also happens for using decoupling cells or transistor reordering reaching 21.2% and 3.5%, respectively.

In the other hand, sleep transistor and Schmitt Trigger technique shows large dependence of the circuit function, both for increase on power and delay. The Sleep transistor design introduces a power overhead around 33% for each logic cell.

Even that the decoupling cells demanding more transistors in the design, a cross-coupled mode is favourable to consume less power. The Schmitt Trigger design suffers a higher average impact in order of 45% on power consumption. The power overhead increases even more for lower levels of WFF and larger sizing for all mitigation approaches, where the sleep transistor design is the least influenced statistically for both factors. However, the delay penalty decreases around 36% when sleep transistors were adopted instead of Schmitt Triggers.

Observing the circuit dependence for the evaluated techniques in the Fig. 12, the basic inverter cell is the most impacted by all the techniques. Fig. 12 also makes clear how large is the Schmitt Trigger drawback on the power for all evaluated circuits, and the outstanding influence on the AOI211 delay. For any case, the transistor reordering or decoupling cell techniques impact delay or power over 20%. The sleep transistor overhead is the most related with the circuit function, the delay impact can range from exceptionally low levels (2.5% for NOR functions) to increasing over 60% for the Inverter gate. Also, as an exception the delay impact on the inverter cell is greater than on the power consumption. With exception of decoupling cells technique, the delay penalties decrease for low levels of WFF. Larger sleep transistors decrease the impact on delay, but if decoupling cells or Schmitt Triggers are connected to the output, the influence on the delay overhead grows as the sizing also increases.

Table III. Area impact of circuit-level techniques with 3 fins

Technique	Extra devices	Area (nm^2) for the # of Inputs			
		1	2	3	4
Standard version	0	50.9	67.8	84.8	101.7
T. Reordering	0	-	-	84.8	101.7
Schmitt Trigger	6	169.6	186.5	203.5	220.4
Decoupling cells	4	169.6	186.5	203.5	220.4
Sleep transistor	1	67.8	84.8	*101.7	*118.7

* These values change for the OAI logic cells.

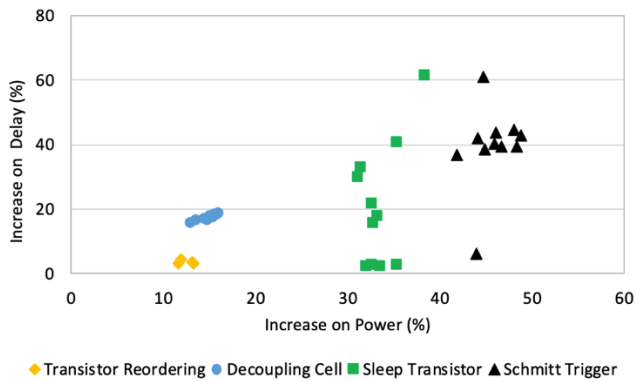


Fig. 11 Power and delay overhead of using circuit-level mitigation approaches

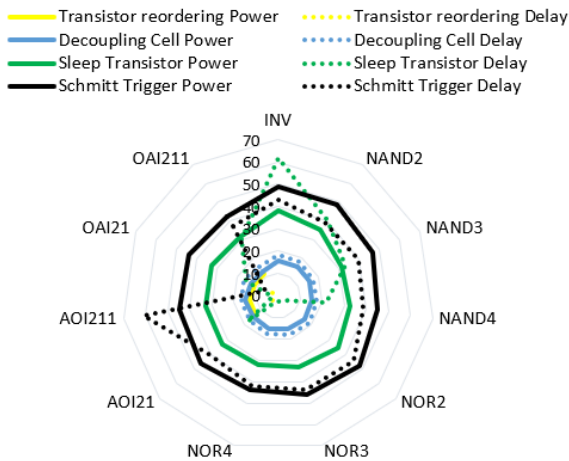


Fig. 12 Circuit dependency for power and delay interference

5. Conclusions

This work explored a circuit-level method based on the insertion of an ST in the design to increase the robustness of FinFET cells to the process variations and radiation-induced soft errors. The ST design is a promising way to obtain more reliable logic cells for all scenarios investigated. This technique tends to be more advantageous for lower levels of WFF (2%) for delay variability, except for NAND and INV cells. The benefits of power variability increase as levels of WFF also raises in the most of FinFET cells. The increase of ST sizing is not profitable for delay variability, but can be an interesting strategy for power variability, mainly for lower levels of WFF. Moreover, the ST design is almost immune to soft errors for all LET and supply voltages studied.

However, depending on the design requirements, the use of other approaches can be more suitable due to the area, delay, and power penalties. In this way, the ST insertion is more advisable for designs with huge reliability requirements. For designs with area constraints, the sleep transistor is more indicated for reliability improvement. Otherwise, the decoupling cells are suggested for designs with power or delay limitations. Although the transistor reordering has few penalties involved, this technique is not efficient to decrease

the SE susceptibility and the attenuation of process variations is not statically significant.

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