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A Non-Closed-Form Mathematical Model for Uniform and Non-Uniform Distributed Amplifiers

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Abstract— A non-closed-form general mathematical model for CMOS distributed amplifier (DA) for broadband applications is presented. Contrary to the artificial transmission line (TL) assumption made in the conventional analytical models, the proposed model treats the DA as a discrete set of cells connected together, and hence considers propagation and mismatch between inter-cells. This approach provides designers with a much more accurate first sizing of the DA compared to conventional ways and, as a result, leads to a reduced design time and complexity. The model enables both quantitative and qualitative analysis of a DA, for the purpose of aiding the designers in predicting the relations between DA performance and its multi-design parameters, especially in the context of non-uniform designs. In addition, it is well suited to Computer-Automated Design (CAutoD), to help in achieving designs having a given set of performance goals. The validation of the model is demonstrated on two designs, by a comparison with simulations done in Keysight's ADS tool and using STMicroelectronics' 55-nm SiGe BiCMOS design kit. First design is inspired from an already published non-uniform DA design while second one proposes a 100-GHz bandwidth CMOS uniform DA with 8 dB of power gain, after using it in a CAutoD process.

Index Terms— Distributed Amplifier, Broadband, Unit-cell, Gm-cell, CMOS, CAutoD, Uniform, Non-Uniform.

I. INTRODUCTION

With the advances in low-cost MMIC technologies, the design of distributed amplifier (DA) has emerged, from large size distributed vacuum tubes amplifier, first patented by William Percival in 1936 [1], into fully integrated wideband microwave amplifier in the 21st century. Its excessively high gain-bandwidth product, as in [2], has been found useful for applications such as high-speed data links, satellite communications and broadband optical communication. For that, considerable research efforts were invested in DAs, historically as in [3] or very recently as in [4]. Efforts were also oriented towards non-uniform design techniques as ways to improve DA performance. As an example, in [5], a transmission line (TL) impedance tapering was used to improve bandwidth whilst in [6] a stage-scaling technique resulted in higher PAE over passband region.

The design of a broadband response, however, poses a great challenge for RF/microwave engineers. Difficulties arise when it is desired to maintain a high-level flat gain with acceptable matching over the entire desired bandwidth of operation and at the same time to cover a small surface area

and consume less power. Those issues are attributed to the large number of intercorrelated design parameters. Simple models as in [7] are useful for underlying the principles of the DA behavior and for a first step in device sizing, but, constrain designers since those models are based on a lumped element assumption where spacing between active Gm-cells must be very small compared with the wavelength of operation. In addition, they are only applicable to uniform structures, due to the Gm-cell per-unit-length distribution assumption made. To overcome those weaknesses, intensive simulations with CAD tools can be used, based on a fixed structural approach. Some charts were provided in [5] through a fine description of the equivalent model of the distributed amplifier stage, including TL tapering. However, this approach does not accurately represent inter-cells mismatches which give rise to gain ripple, since they are founded on the basis of artificial TL assumption besides neglecting the propagation effect of inter-TL segments. Furthermore, the design approach in [5] highly relies on experience and on intensive simulation-based tuning.

In this context, a theoretical analysis of a DA structure is presented in this paper, considering a fine modeling of uniformly, or non-uniformly, distributed Gm-cells, in addition with their inter-cells mismatches. Also, a non-closed-form mathematical model is proposed to describe the DA behavior. This model, combined with a numerical software, enables the proper examination of each building element and its effects on the overall response in order to support designers. For that reason, emphasis was made on keeping the model (as well as its representation) as simple as possible. Also, the number of active Gm-cells, N , will be considered as a variable, and not an input parameter contrarily to what is proposed in [7], to give more flexibility in the design.

In Section II, the background principle of a DA is presented, and a detailed explanation of the derived mathematical tools is reported. In Section III, the proposed model is subjected to a validation test with ADS simulation using CMOS part of BiCMOS 55-nm DK technology, while in Section IV we discuss the attained results.

II. DISTRIBUTED AMPLIFIER ANALYSIS

As shown in Fig. 1, a DA consists of several transconductances embedded between two TLs. The combination of one active element (Gm-cell) and a pair of TL segments on both its ends is commonly referred to as a unit-cell. Since every Gm-cell is loading both physical input and output TLs by their own specific input and output complex

impedances, respectively, each n th cell is considered attached to a defined periodic structure of loaded TLs. RF signal feeds the DA input line, denoted with subscript ‘g’ for gate line, and reaches the DA output line, denoted with subscript ‘d’ for drain line, as an amplified version established by the number of unit cells used (N).

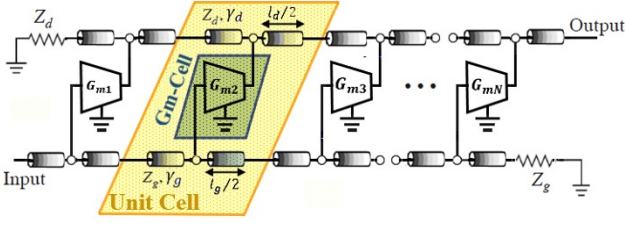


Fig. 1. Conventional distributed amplifier made of N unit cells.

When it comes to the uniform DA designs, as proposed in [7], identical output-side TL segments of similar characteristics (Z_d, γ_d) and same lengths $l_d/2$ are used. The same applies for the input-side TLs. In the model presented in this paper, each unit-cell can differ from its neighbors in terms of Gm-cell, and in terms of left and right TL segments. The CMOS Gm-cell model is detailed hereafter in section A while the output (drain) and input (gate) sides analysis are presented in sections B and C, before their correlation is considered in D.

A. Gm-Cell Model

In this paper, a MOSFET based cascode topology is used in the Gm-cell, as represented in Fig. 2(a), which helps to reduce the Miller effect and to improve reverse-isolation. This Gm-cell is modeled by a simplified equivalent circuit depicted in Fig. 2(b), where the device will be considered unilateral as a first approach, i.e. C_{gd} will be neglected.

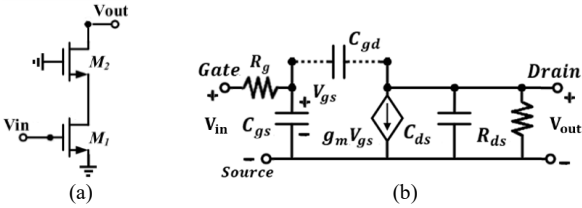


Fig. 2. (a) AC representation of a typical cascode cell and (b) its simplified small-signal equivalent circuit.

B. Drain Line Analysis

1) Single unit-cell Study: The drain side of a Gm-Cell is depicted by a current source in parallel with lumped resistor and capacitor, denoted R_{ds_n} and C_{ds_n} respectively, which characterize the complex admittance seen at the output side of the cascode cell, as in Fig. 2(b). When integrated into the DA, both current source and admittance are connected in the middle of two TLs denoted by subscripts ‘L’, for left side, and ‘R’, for right side, as illustrated in Fig. 3.

In Fig. 3, the effect of the preceding and subsequent Gm-cells is considered as they will influence the total output current generated by that particular unit-cell. For that, both the left and right sides of the n th unit-cell are modeled by an equivalent impedance, Z_{equL_n} and Z_{equR_n} , respectively. Current $I_{out_{n-1}}$, flowing from left side, represents the total equivalent traveling current wave generated by the preceding cells towards right side. Z_{inR_n} (Z_{inL_n}) represents the right

(left) TL input impedance looking towards the load Z_{equR_n} (Z_{equL_n}) of the TL connected to the right (left) of the n th Gm-cell.

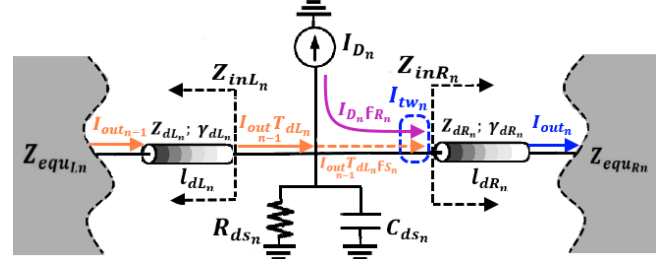


Fig. 3. Drain side of a single unit-cell.

Based on this configuration and with the help of Kirchhoff’s laws and microwave TL theory, the total current wave traveling towards the right side of the n th Gm-cell, I_{tw_n} , is expressed as;

$$I_{tw_n} = -I_{D_n} f_{R_n} + I_{out_{n-1}} f_{S_n} T_{dL_n} \quad (1)$$

where f_{R_n} represents how much current generated by the n th current source, I_{D_n} , is incident on the right TL, and is calculated from (2);

$$f_{R_n} = \frac{Z_{inL_n} R_{ds_n}}{(1 + j\omega R_{ds_n} C_{ds_n}) Z_{inL_n} Z_{inR_n} + (Z_{inL_n} + Z_{inR_n}) R_{ds_n}} \quad (2)$$

and f_{S_n} represents the splitting current factor between the right part of the n th Gm-cell, just before the right TL (Z_{dR_n}, γ_{dR_n}), and the dissipated part in the transistor drain impedance. f_{S_n} is given by (3).

$$f_{S_n} = \frac{R_{ds_n}}{(1 + j\omega R_{ds_n} C_{ds_n}) Z_{inR_n} + R_{ds_n}} \quad (3)$$

Finally, T_{dL_n} is the n th left drain TL (Z_{dL_n}, γ_{dL_n}) transmission coefficient which takes into account the multiple reflections that occur at its boundaries. T_{dL_n} can be calculated using (4) on the basis of Fig. 3:

$$T_{dL_n} = \frac{(1 + \Gamma_{inL_n})(1 + \Gamma_{outdL_n})e^{-\gamma_{dL_n} l_{dL_n}}}{1 + \Gamma_{inL_n} \Gamma_{outdL_n} e^{-2\gamma_{dL_n} l_{dL_n}}} \quad (4a)$$

$$\Gamma_{inL_n} = \frac{Z_{L_n} - Z_{dL_n}}{Z_{L_n} + Z_{dL_n}}; \Gamma_{outdL_n} = \frac{Z_{dL_n} - Z_{R_n}}{Z_{dL_n} + Z_{R_n}} \quad (4b)$$

Z_{L_n} is the TL input impedance seen at the left side of the left TL loaded by Z_{inR_n} in parallel with (R_{ds_n}, C_{ds_n}). Z_{R_n} is the TL input impedance seen at the right side of the left TL loaded by Z_{equL_n} . Previous impedances are plotted on Fig. 3.

In order to determine the amount of current that a given n th unit-cell transmits to subsequent cells, represented as an equivalent load impedance, Z_{equR_n} , in Fig. 3, the transmission coefficient of the right-side TL is introduced to the input current expressed in (1), and hence the total output current comes to:

$$I_{out_n} = T_{dR_n} I_{tw_n} = -I_{D_n} f_{R_n} T_{dR_n} + I_{out_{n-1}} f_{S_n} T_{dL_n} T_{dR_n} \quad (5)$$

where the transmission coefficient T_{dR_n} stands for the n th right drain TL and is calculated using (6):

$$T_{dR_n} = \frac{(1 + \Gamma_{indR_n})(1 + \Gamma_{outdR_n})e^{-\gamma_{dR_n}l_{dR_n}}}{1 + \Gamma_{indR_n}\Gamma_{outdR_n}e^{-2\gamma_{dR_n}l_{dR_n}}} \quad (6a)$$

$$\Gamma_{indR_n} = \frac{Z_{LR_n} - Z_{dR_n}}{Z_{LR_n} + Z_{dR_n}}; \Gamma_{outdR_n} = \frac{Z_{dR_n} - Z_{RR_n}}{Z_{dR_n} + Z_{RR_n}} \quad (6b)$$

Z_{LR_n} is the TL input impedance seen at the left side of the right TL loaded by Z_{equR_n} . Z_{RR_n} is the TL input impedance seen at the right side of the right TL loaded by Z_{inL_n} in parallel with (R_{ds_n}, C_{ds_n}) . Previous impedances are represented on Fig. 3.

2) N-Distributed Unit-cells Study: Fig. 4 illustrates the case where N unit-cells, shown in Fig. 3, are distributed.

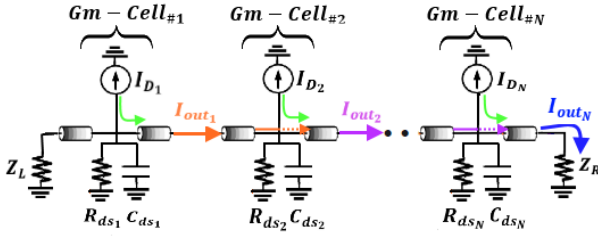


Fig. 4. Drain loaded line representation.

By developing (5), the total output current generated from the drain line of a DA is expressed in (7).

$$I_{out} = \sum_{n=1}^N -I_{D_n} \left[\prod_{i=n}^N (T_{dR_i} \Gamma_{R_i})^{\delta_{(i,n)}} (\Gamma_{S_i} T_{dL_i} T_{dR_i})^{1-\delta_{(i,n)}} \right] \quad (7)$$

where $\delta_{(i,n)}$ represents the ‘‘Kronecker’’ Delta.

C. Gate Line Analysis

For the gate line analysis, a similar approach to that of the drain line analysis was applied. Based on Fig. 2(a), the gate side of the Gm-cell is depicted as an equivalent impedance of series resistor and capacitor, denoted R_g and C_{gs} , respectively. By referring to the definition of a DA, the gate line is thus described as a transmission line periodically loaded by N equivalent R_g in series with C_{gs} impedances.

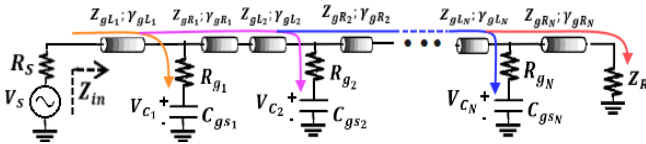


Fig. 5. Gate loaded line representation.

Based on this configuration, the approach was focused on determining the voltage V_{c_n} at each gate-source capacitor C_{gs_n} for the n th unit-cell when a given voltage source V_S is applied and it resulted in the capacitor voltage expression (8).

$$V_{c_n} = V_S \left(\frac{Z_{in}}{Z_{in} + R_S} \right) \left(\frac{1}{1 + j\omega R_{g_n} C_{gs_n}} \right) \prod_{i=1}^n [T_{gL_i} T_{gR_i}^{1-\delta_{(i,n)}}] \quad (8)$$

where Z_{in} is the input impedance of the whole DA and R_S is the internal resistance of the signal source. T_{gL_n} (T_{gR_n}) is the

n th transmission coefficient of the left (right) side gate TL which is determined by using the same equations as (4a) ((6a) respectively). The only difference lies in the expression of the boundary reflection coefficients.

$$\Gamma_{in_{gL_n}} = -\frac{Z_{LL_n} - Z_{gL_n}}{Z_{LL_n} + Z_{gL_n}}; \Gamma_{out_{gL_n}} = -\frac{Z_{gL_n} - Z_{RL_n}}{Z_{gL_n} + Z_{RL_n}} \quad (9)$$

$$\Gamma_{in_{gR_n}} = -\frac{Z_{LR_n} - Z_{gR_n}}{Z_{LR_n} + Z_{gR_n}}; \Gamma_{out_{gR_n}} = -\frac{Z_{gR_n} - Z_{RR_n}}{Z_{gR_n} + Z_{RR_n}}$$

D. Relationship Between DA Gate and Drain Lines.

The parameter linking the drain line, modeled by (7), and the gate line, modeled by (8), is the transconductance, g_m , of the Gm-cell which relates its output current, I_{D_n} , to its input voltage, V_{c_n} , as given below.

$$I_{D_n} = g_{m_n} V_{c_n} \quad (10)$$

E. Summary

Throughout Section II, the quantitative analysis of a non-uniform DA was presented and resulted in two non-closed form mathematical models (7) and (8) for both the drain and gate lines, respectively, linked with a key equation (10). Those equations, when implemented in a numerical software, can give to the DA designer a better comprehension of the relation between the parameters listed in Table I below and the DA behavior.

TABLE I. DESIGN PARAMETERS OF A DISTRIBUTED AMPLIFIER

Parameters	Definition
R_g	Series gate resistance
C_{gs}	Gate-to-source capacitance
R_{ds}	Drain-to-source resistance
C_{ds}	Drain-to-source capacitance
g_m	Transconductance
$Z_{dR,L}, Z_{gR,L}$	Drain and gate, right or left, TL characteristic impedance
$\gamma_{dR,L}, \gamma_{gR,L}$	Drain and gate, right or left, TL propagation constant
$l_{dR,L}, l_{gR,L}$	Drain and gate, right or left, TL physical length

III. VALIDATION EXAMPLES

A. Non-Uniform Distributed Amplifier

In order to examine the degree of accuracy of the proposed mathematical model, initially a non-uniform tapered DA was considered and implemented in Matlab© software. The same DA was designed in Keysight’s ADS software, used as a reference for comparison. For each Gm-cell configuration depicted in Fig. 2(a), the common-gate transistor, M2, is chosen with a channel width double to that of the common-source transistor, M1, to balance input and output capacitances of the cascode cell. Intrinsic elements extraction of Table I, for both NMOS and TLs, is performed on the basis of simulation conducted with the design kit of the B55 technology from STMicroelectronics. We adopted a 4 unit-cell DA with identical TL segments lengths. For the first, leftmost, unit-cell the transistors widths were chosen equal to 20 and 40 μm respectively. The two drain side TL segments were chosen equal to 1.0 μm . Inspired from [5], a tapering coefficient is then applied to the remaining cells where each Gm-cell is widened by a factor kn , in which n represents the

unit-cell position. We adopted $k = 1.1$. However, in contrast to having a continuous tapered output line as in [5], for each unit-cell, the widths of the drain side TLs segments were widened by a coefficient n to deliberately promote much more important mismatch between unit-cells. The gate line width is kept fixed equal to $1.0 \mu\text{m}$. The resulting power gain and input return loss obtained from our model is compared against ADS simulations in Fig. 6, validating the accuracy of the proposed model. Simulation results show a very good agreement up to 200 GHz, with small discrepancy appearing attributed to the Gm-cell unilateral assumption.

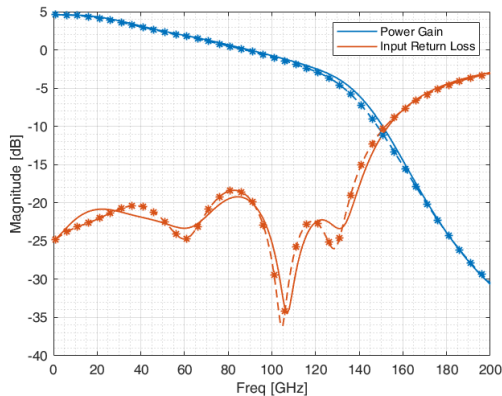


Fig. 6. Comparison between small-signal power gain and input return loss for a non-uniform 4 unit-cells DA, at 50Ω reference impedance, with tapered drain line and cascode cells. Solid line: Model– Dotted line: ADS

B. CAutoD Uniform Distributed Amplifier

Fig. 6 validated the proposed model that can be considered now for another DA design. We propose in this case a uniform one. Traditionally, DA design is performed in two steps. First, based on conventional analytical equations [7], an optimum number of cells is determined, corresponding to an optimum gain, available only at the considered frequency of calculation. In a second step, the uniform DA is tuned in a CAD software. Hence, with this methodology, maximizing the performance consists in tuning each cell independently, that is to say a high number of variables as stated on Table I. Modifying the number of cells assume to redo all the CAD optimization procedure. On the contrary, the proposed model includes this number of cells as any variable parameter.

As a proof of concept, the design analysis is used throughout a CAutoD, implemented on Matlab®, and enabling to optimize both the design parameters listed in Table I and the number of unit-cells, N . The DA is based on the cascode topology and includes inductive peaking to compensate losses, as described in [8]. Results show very good agreement between analytical model convergence and the CAD implementation in ADS as shown on Fig. 7. By only using NMOS transistors available through the B55 DK, a 1-dB bandwidth of 100 GHz was coded as the design goal, which resulted in a DA having a power gain of 8 dB with a maximum of -10 dB matching inside passband, by using only 5 unit-cells.

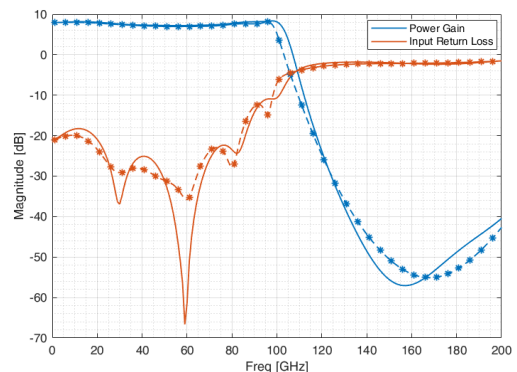


Fig. 7. Comparison between the proposed DA model including inductive peaking and the same DA in ADS for $N=5$ and $W=31 \mu\text{m}$ (M1) - $62 \mu\text{m}$ (M2), in terms of power gain and input return loss. Solid line: Model– Dotted line: ADS. For a gate biasing of 0.7 V and a drain biasing of 1.2 V, with a reference impedance of 50Ω .

IV. CONCLUSION

In this paper, a non-closed-form mathematical model for DA was proposed and tested. The model takes into account propagation and mismatches between adjacent cells and hence showed excellent agreement with ADS simulation results in both uniform and non-uniform cases, even with unilateral assumption. This model was also applied to a CAutoD of a DA targeting 100-GHz bandwidth with successful outcome. The device is under fabrication process at that time. This model will be applied in further DA studies such as parametric analysis in addition to optimization algorithms with the purpose of exploring all the potentialities of non-uniform designs. It can allow amplifier designers to gain a better comprehension of the relation between the main parameters of the DA structure and its performance characteristics, and will hopefully help in coming up with new design techniques targeting specifications not achievable by the conventional design approaches, such as high flat gain, low power consumption and compact form distributed amplifiers.

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