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Review

Towards Monolithic Indium Phosphide (InP)-Based Electronic Photonic Technologies for beyond 5G Communication Systems

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Abstract: This review paper reports the prerequisites of a monolithic integrated terahertz (THz) technology capable of meeting the network capacity requirements of beyond-5G wireless communications system (WCS). Keeping in mind that the terahertz signal generation for the beyond-5G networks relies on the technology power loss management, we propose a single computationally efficient software design tool featuring cutting-edge optical devices and high speed III–V electronics for the design of optoelectronic integrated circuits (OEICs) monolithically integrated on a single Indium-Phosphide (InP) die. Through the implementation of accurate and SPICE (Simulation Program with Integrated Circuit Emphasis)-compatible compact models of uni-traveling carrier photodiodes (UTC-PDs) and InP double heterojunction bipolar transistors (DHBTs), we demonstrated that the next generation of THz technologies for beyond-5G networks requires (i) a multi-physical understanding of their operation described through electrical, photonic and thermal equations, (ii) dedicated test structures for characterization in the frequency range higher than 110 GHz, (iii) a dedicated parameter extraction procedure, along with (iv) a circuit reliability assessment methodology. Developed on the research and development activities achieved in the past two decades, we detailed each part of the multiphysics design optimization approach while ensuring technology power loss management through a holistic procedure compatible with existing software tools and design flow for the timely and cost-effective achievement of THz OEICs.

Keywords: electrical characterization; compact model; heterojunction bipolar transistor; uni-traveling carrier photodiodes; high frequency; indium-phosphide; sub-millimeter wave; terahertz; TCAD and Monte Carlo simulations

1. Introduction

Signals in the frequency range of 30–300 GHz are best suited for ultra-broadband wireless communications. Unfortunately, most of the solid-state sources produce insufficient power (limited to few milliwatts) at the upper end of this spectrum to support high data-rate communication over useful distances (>100 m). To respond to this challenge, novel baseband processing technology, identified as the enabling technology for the future beyond 5G networking, is capable of focusing energy into finer-grained areas and provide significant increase in both transmission energy efficiency and spectrum efficiency.

For some years, in the world of solid-state high-frequency microelectronics, III–V double heterojunction bipolar transistors (DHBTs) on InP substrate have led the frequency race for the electronic amplification of >100 GHz signals and amplifier circuits offering high output power density [1]. In the parallel world of photonics, the uni-traveling carrier photodiode (UTC-PD) has been widely studied for ultrafast optoelectronic applications such as fiber-optic receivers and THz signal generation. InP UTC photodiodes, invented by Nippon Telegraph and Telephone Corporation (NTT) in 1997 [2,3], rely only on electron transport which significantly improves high power capability and the maximum achievable bandwidth of UTC photodiodes compared to that of the PIN photodiodes. Therefore, UTC photodiodes have become a key component for electronic/photonic technology convergence in the mm-wave band [4,5]. Nevertheless, interfacing photodiodes with amplifier circuits is required to obtain sufficient radio-frequency (RF) power and to perform signal processing. Combining these two worlds will thus benefit from the key features of each: bandwidth, tunability, stability and fiber compatibility for the photodiode, as well as the power handling capability of the transistors. To that end, the overall objective would be to develop high-performance terahertz-wave transmitter modules based on a disruptive monolithic opto-electronic integrated circuit (OEIC), which can be installed in radio base stations to directly convert the optical signals coming from midhaul/fronthaul networks into radio signals. This OEIC technology will pave the way for beyond 5G communication technologies, by delivering compact and efficient modules at room temperature. Such an innovative and ambitious objective requires integrating the photonic and electronic technologies monolithically on InP substrate, in order to boost the power of the single photodiode within the frequency range of 220–325 GHz. One of such most sought-after examples demonstrates the integration of UTC-PDs with InP DHBt amplifiers (either a transimpedance amplifier (TIA) or a power amplifier (PA)). Indeed, the optical generation of mm and THz waves represents a promising approach for next generation radio communication to overcome the difficulty in obtaining high-performance (and low-cost) electronic oscillators and modulators. Significant progress has been made on this subject [6] and optical generation appears to be the most suitable solution for frequencies above 100 GHz [7]. Most importantly, at present, the convergence between optical and radio networks offers a timely solution for developing communication technologies beyond 5G communication systems [8].

To realize such a monolithically integrated electronic–photonic technology (sketched in Figure 1), one should ideally rely on the stacked epitaxial growth of the two device structures and the subsequent fabrication process steps of the monolithic OEIC. This approach must be chosen to (i) optimize the epitaxial design of each device independently; and (ii) minimize the distance and the electronic propagation losses between them at very high operating frequencies while (iii) managing the mutual heat coupling. In order to take into account parasitic contributions accurately, passive components required for the integrated circuits should also be developed and optimized. Indeed, in mm-wave frequencies, the connection between a photodiode and an amplifier is critical for limiting the parasitic influence. Therefore, accurate models of UTC-PDs and DHBtS are required to optimize the bias points and the interconnections between the photonic and the electronic parts. Using the same design methodology as the silicon industry, the compact modeling of the photodiodes and the InP DHBtS is the most promising way to achieve the best performance of the monolithically integrated optoelectronic circuits.

As a consequence, accurate compact models and the associated parameter values for the UTC-PDs, the DHBtS as well as the passive elements should be jointly elaborated in order to guide the development of the OEIC at the early stage of its design. These compact models should be included in a single process design kit (PDK) that could be incorporated into the OEIC design tools. Featuring the ensemble of the building blocks, the PDK could thus allow the design and simulation of UTC–TIA–PA.

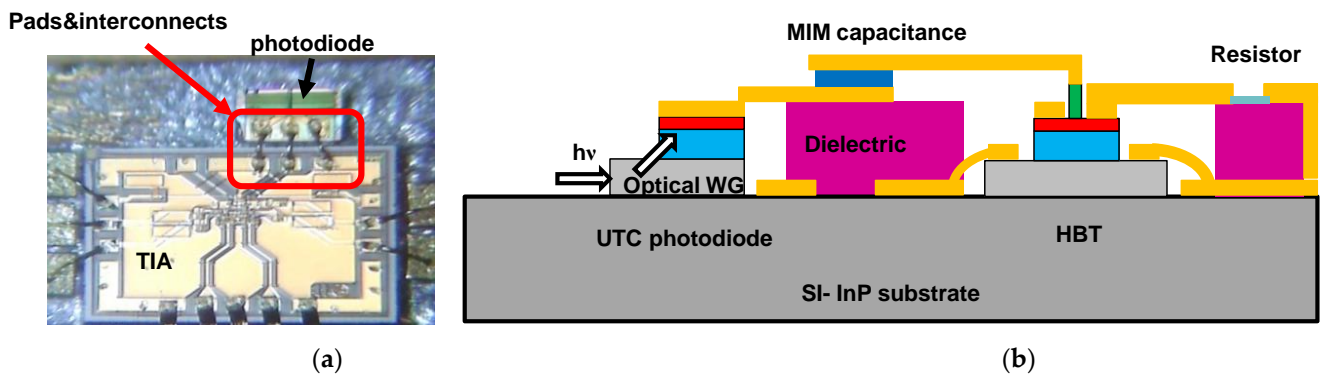


Figure 1. Schematic view of the integration of photodiode and InP heterojunction bipolar transistor (HBT) based trans-impedance amplifier (TIA) on the same substrate: (a) top view of the two dies bound together with three wire bondings highlighted with the red arrow, the electronic and the photonic modules; and (b) schematic view of the integration of the Uni-traveling-Carrier (UTC) photodiode and the HBT on the same substrate with integrated optical waveguide (WG) and metal-insulator-metal (MIM) capacitance.

The aim of this article was to provide a comprehensive evaluation of technological advances both in terms of sheer technological performances (photonic, electrical and thermal) as well as the software tools available for accomplishing this innovative design. In terms of design tools, in particular, electronic and photonic communities have very different simulation tools available, owing to the current status of their respective state of the arts. Integrated circuit design would thus necessitate multiphysics tools for facilitating the development of this emerging technology. Despite the differences in the design methods of the two communities, electronic design automation (EDA) tools have evolved and matured through years of industrial endeavors, leading to an abundance of SPICE compatible compact models and circuit design environments. While the photonic community is still lacking a key circuit design environment, the best possible solution would be to ensure the compatibility of photonic device simulation with existing EDA environments. Therefore, in the current work, we propose not only an up-to-date DHBT compact model dedicated to devices on InP substrate but we also developed and enhanced a compact model specifically for UTC photodiodes with the goal of making way for a common design framework. Both compact models are fully compatible with the EDA circuit libraries. Moreover, to ensure that common key physical quantities be handled, DHBT and UTC-PD compact models compute either electronic or photonic quantities along with their thermal parameters, which can, in the long run, pave the way for multiphysics tools.

In order to pursue the aforementioned ideas further, in this paper, we present efficient compact models that are compatible with UTC photodiode and DHBT technologies developed by III-V Lab, which may be considered as the first step towards the efficient monolithic co-integration of electronic and photonic parts for this unique OEIC technology of the future. The rest of the paper is organized as follows. Section 2 is dedicated to the detailed technologies under investigation, UTC-PD and InP DHBT technologies, both from III-V Lab. Section 3 presents the electrical compact models associated with the two devices. Section 4 shows the DC characterization of UTC-PDs and InP DHBTs for the purpose of compact model validation. Section 5 provides insights into the thermal characterization and associated compact model sub-circuits that allow the management of self-heating as well as the mutual thermal coupling. Section 6 deals with the high frequency characterization and modeling of both devices. Section 7 discusses additional effects to be taken into consideration through the technology computer-aided design (TCAD) simulation, the evaluation of key performance metrics through model extrapolation in comparison with the state of the art as well as the methodology for assessing OEIC circuit reliability. Finally, Section 8 provides the conclusion and future perspectives.

2. Technologies

The III–V Lab develops both UTC-PD and InP DHBT technologies within its clean rooms. UTC-PDs and DHBTs share the same base–collector interface heterostructure and therefore, for this interface, the physical models are similar despite differences in thicknesses and doping levels between optimized UTC-PD structures and optimized DHBT structures. This technological similarity opens up the way to integrate DHBT and UTC photodiodes on the same substrate, in order to suppress the parasitic on the interface between them (Figure 1). This could be done either by finding a shared epitaxial structure with the best compromise between UTC-PD and DHBT structures or by a selective regrowth of UTC-PD layers on a DHBT layer or vice versa.

The InP DHBT structure is grown externally by solid source molecular beam epitaxy on 3 wafers. The vertical structure is optimized in order to achieve balanced frequency performances for $0.7\ \mu\text{m}$ emitter DHBTs with f_T and f_{max} around 400 GHz. The structure is similar to the one described in [9] except for the low doped collector region for which Si-doping level is reduced to $1.5 \times 10^{16}\ \text{at}/\text{cm}^{-3}$ to improve the breakdown voltage. The 0.5 and $0.7\ \mu\text{m}$ InP DHBTs with emitter length varying from 5 to $10\ \mu\text{m}$ are processed using a wet-etched triple mesa technology. Figure 2a presents a simplified cross-sectional view of the transistor.

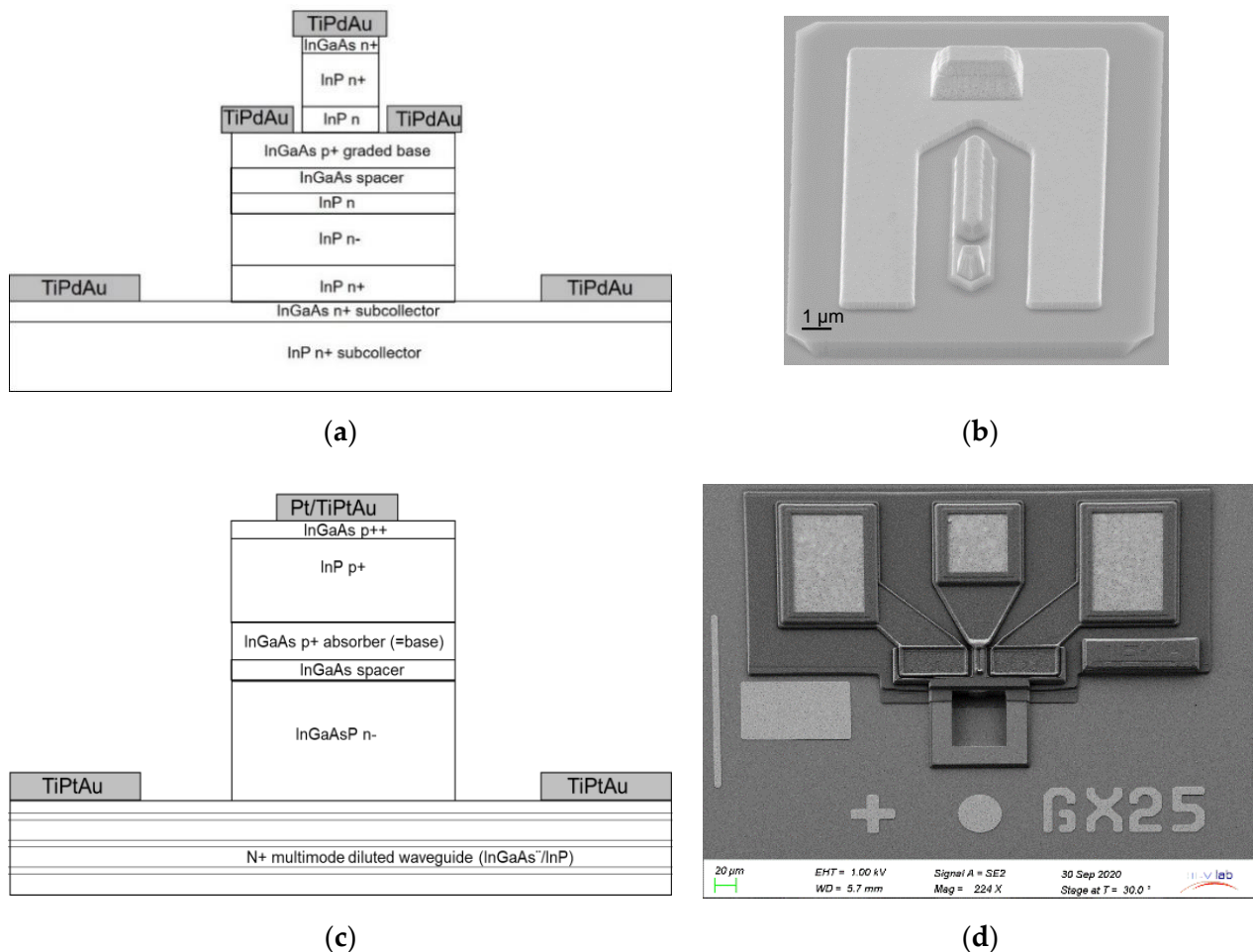


Figure 2. (a) Simplified schematic cross-sectional view of submicrometer InP/InGaAs double heterojunction bipolar transistors (DHBTs) and (b) Scanning electron microphotographs of a $0.7 \times 5\ \mu\text{m}^2$ InP DHBT before metal interconnection level; (c) Simplified schematic cross-sectional view of a waveguide uni-traveling carrier photodiode (UTC-PD), (d) Scanning electron microphotographs of a $5 \times 25\ \mu\text{m}^2$ InP UTC photodiode after metal interconnection level.

Emitter and base contacts as well as the base plug needed for interconnection are defined by e-beam lithography whereas stepper lithography is used for other technological steps. TiPdAu (titanium–palladium–gold), deposited by vacuum evaporation, is used for all contacts. After encapsulation with silicon nitride (SiN) for higher robustness and planarization with polyimide, emitter, base and collector contacts are opened by etching to form device interconnects. Figure 2b presents a scanning electron microphotograph of a $0.7 \times 5 \mu\text{m}^2$ InP DHBT.

The UTC photodiode structure is grown either by gas-source molecular beam epitaxy (GS-MBE) [10] or by metal–organic vapor-phase epitaxy (MOVPE) as in this paper. A multimode diluted waveguide is used for optimal fiber coupling [11]. The process begins with the etching of the top InP layers, followed by base and collector etching using a mixed of dry and wet etching. Pt is used for a P contact followed by a rapid thermal annealing and TiPtAu are used for the N contacts and electrodes (Figure 2c). Figure 2d shows a $5 \times 25 \mu\text{m}^2$ InP UTC photodiode with the metal interconnections.

To evaluate the performances of this integrated co-design approach with the UTC-PDs and the DHBTs, accurate and physics-based compact models are required. This is even more important if the same epitaxy is shared, in order to obtain a precise overview of the impact on the performances of individual UTC-PDs and DHBTs as well as the potential gain offered by the co-design on the circuit performances. To that end, in this paper, we present two compact models compatible with UTC-PD and DHBT structures which are first validated on individual and optimized UTC-PD and DHBT chips.

3. Compact Modelling

Along with the progress in electronic design automation, compact models have continued to serve the electronics community at the core of all industrial integrated circuit design flow. Owing to the analytic forms of its equations, a compact model is significantly efficient in terms of computational burden and practical from a design point of view. Moreover, the correct formulation of the analytic equations can capture device physics with sufficient accuracy and is thus preferable to numerical device simulations by designers in order to speed up the simulation time. For electronic devices, the compact model council has certified a number of such accurate physics-based compact models compatible with SPICE simulation environments, including the High Current Model (HiCuM) model that has been widely accepted by the bipolar transistor community. As justified previously, the photonic community has been missing the equivalent tools in the context of optical devices and therefore, multiphysics formulation is crucial for the successful integration of electronic and photonic devices. With that in mind, as a first step, we present a modeling framework for both devices through an assembly of SPICE compact models for InP bipolar transistor (HiCuM [12]) and UTC photodiodes (in-house [13]). In the following section, we describe the fundamentals of these two models.

3.1. DHBT Compact Modeling

The HiCuM model [12] has focused on improving the dynamic description of bipolar transistors by putting the main emphasis on accurately modeling charge storage. This approach/representation can successfully capture both the static and dynamic behavior of the transistor through a set of analytical equations governed by the physics of charge build-up/partitioning within the bipolar transistor. Circuit design and optimization is based on proper device sizing and thus requires a geometry scalable compact transistor model such as HiCuM which is quite scaling-friendly. Except for the thermal and substrate coupling network, a compact analytical description as a function of device configuration exists for each element of the HiCuM equivalent circuit. Additionally, a new scalable model for the thermal impedance of III–V DHBTs, that has been developed based on the physics of heat diffusion within the HBT architecture [14], has been used to replace the existing simplistic thermal network of the HiCuM equivalent circuit for better accuracy (further elaborated in Section 5).

3.2. UTC Photodiode Compact Modeling

The compact model for the UTC-PDs reported in [13] is a Verilog-A model for describing the semiconductor physics governing the junction currents and the optical response of the photodiode. The model is further enhanced by incorporating improved descriptions of the dark and photocurrents. The schematic (Figure 3) shows the equivalent circuit of the UTC-PD, including extrinsic pads and coplanar waveguide (CPW) parasitic elements. The intrinsic part is represented by the diode dark current source, I_{dark} , the junction capacitance, C_j , the shunt resistance, R_{sh} , the series resistances, R_s , and the photocurrent, $I_{ph}(w)$. In order to facilitate model scaling, the diode currents and the junction capacitances are normalized by the device active area, S , of UTC-PDs.

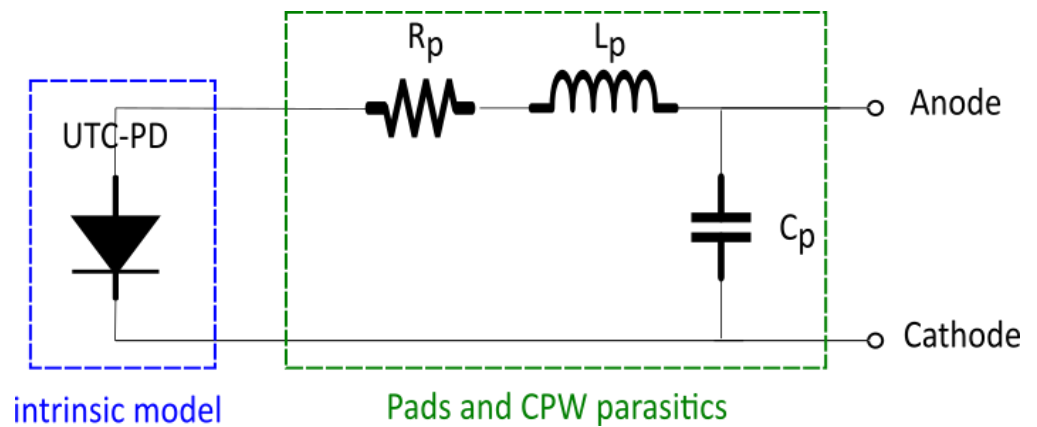


Figure 3. UTC-PD basic electrical equivalent circuit.

3.2.1. Dark Current

In forward bias conditions, the dark current of the UTC-PDs is modeled by the classical diode reverse saturation current, I_s [13]. In reverse bias, in addition to the saturation current and the breakdown current modeled in [13], two other contributions have been introduced to improve model accuracy: the band-to-band tunneling current, I_{BTB} (in A), and the trap-assisted tunneling current, I_{TAT} (in A). The tunneling effect is required to describe the dominant current contribution under high reverse bias ($V < -1$) condition. In the general case, the tunneling current takes the following form [15]:

$$I_{BTB} = S \cdot A_{BTB} \cdot E_{max}^2 \cdot V_d \cdot e^{-\frac{B_{BTB}}{E_{max}}} \tag{1}$$

where A_{BTB} (in A/V^3) and B_{BTB} (in V/m) are parameters to be determined from model optimization, V_d is the diode voltage in V, S is the diode area in m^2 . E_{max} is the maximum electric field in V/m at the collector input. It can be expressed as [15]

$$E_{max} = \frac{C_{j0}(T)}{\epsilon_{InGaAsP} \cdot S} \frac{(V_j(T) - V_d)^{1-M} V_j(T)^M}{(1 - M)} \tag{2}$$

where C_{j0} (in F) is the zero bias junction capacitance, $\epsilon_{InGaAsP}$ is the collector’s relative permittivity, V_j is the junction potential (in V) and M is the grading coefficient of the junction. The trap-assisted tunnel current is dominant at low reverse bias ($V > -1$) [14]. Typically, it is a Shockley–Read–Hall (SRH) generation current enhanced by tunneling effects. It can be expressed as [16]

$$I_{TAT} = S \cdot A_{TAT} \cdot E_{max} \cdot V_d \cdot e^{-\frac{B_{TAT}}{E_{max}}} \tag{3}$$

where A_{TAT} (in $AV^{-2}m^{-1}$) and B_{TAT} (V/m) are trap assisted tunneling current parameters. These parameters can be extracted from model optimization at low reverse bias. It should

be noted that the temperature dependence of the static behavior of the dark current is captured through $J_S(T)$, $C_{j0}(T)$ and $V_j(T)$ and the junction temperature is recalculated dynamically via an external thermal network [13].

3.2.2. Photocurrent

Dynamic photocurrent $I_{ph}(\omega)$ mainly depends on transit times across the absorber, τ_a (in s), and the collector region, τ_c (in s). Its amplitude decreases over the frequency range. The dynamic response of the photocurrent has been modified in the model to take the form [17]:

$$I_{ph}(\omega) = S \cdot J_{ph}(\omega = 0) \frac{1}{1 + j\omega\tau_a} \cdot \text{sinc}\left(\frac{\omega\tau_c}{2}\right) \cdot e^{-j\frac{\omega\tau_c}{2}} \quad (4)$$

where $J_{ph}(\omega = 0)$ is the static photocurrent density (in A/m²) and ω is the angular frequency (in rad/s).

Note that due to the low power and current density used in our experimental results, the dependence of the absorption coefficient on temperature has not been taken into account for photocurrent calculation.

4. DC Characterization and Model Validation

In order to validate the accuracy of the compact models described in the preceding sections, we performed extensive characterization on the two technologies which was followed by model validation and parameter extraction at the device level.

4.1. HiCuM Parameter Extraction Methodology

InP DHBT DC characterization were performed on several device dimensions (0.5 and 0.7 μm emitter widths and emitter lengths of 5, 7 and 10 μm) and compared with the HiCuM compact model simulation. For geometry scalable parameter extraction, we employed a dedicated macro model containing the scaling laws for all HiCuM Level 2.0 (L2) parameters related to emitter dimensions. Before the extraction of the model parameters using HiCuM/L2, some technological parameter values are declared and/or pre-calculated such as, for instance, sheet resistances, zero-bias hole charge, area and perimeter dimensions as well as given design rules and process layout information [12].

Parameters related to low-injection conditions are first extracted [12] since at high-current regime, a strong correlation exists between model parameters. Hence, the next step is the junction capacitances extraction. To extract the junction capacitances, the “cold S-parameters” method has been used, in which the transistor is biased to have negligible DC current flow, rendering forward bias across each junction limited to typically less than 0.5 V. The measured S-parameters under these conditions are then converted into Y parameters from which, after proper de-embedding, the depletion capacitances can be derived. The scalable extraction of collector and base current parameters is performed at low injection to prevent model parameter correlation usually in play between high-injection parameters. Considering the collector current split into its internal region and the periphery of the emitter window dimensions:

$$I_C = I_{CA} A_{E0} + I_{CP} P_{E0} \quad (5)$$

here A_{E0} is the effective emitter area (m²) and P_{E0} is the effective perimeter (in m). I_{CA} (A.m⁻²) and I_{CP} (in A.m⁻¹) are the contributions from the intrinsic region and periphery of the device, respectively.

Once the low-injection parameters are extracted, model parameters related to the high current effects are considered. The starting point is the extraction of the transit time at $V_{BC} = 0$ V using the already extracted low-injection parameters. The following step is to take into consideration the high current as well as self-heating effects when extracting the transit time. The first step of the transit time parameter extraction method consists in determining the transit frequency from S-parameter measurements at various collector current densities and various voltages V_{CE} or V_{BC} . The transit frequency f_T is determined using the current gain bandwidth product by e.g., choosing a spot frequency in

the -20 dB/decade roll-off region of the current gain. The second step is the determination of the low-current transit time τ_{f0} and the transit time increase $\Delta\tau_f$ at high current densities. Then, in the high-current region, HiCuM/L2 model parameters are extracted by optimizing the region where f_T reaches the peak along with the Gummel plot high- V_{BE} region. The extraction of thermal resistance is of particular importance [18] since it is strongly coupled with other model parameters in the high-current regime. To obtain a good estimation of the self-heating effects, we used the intersection method [14] to extract the values of R_{TH} from measurements. Additionally, a more detailed thermal impedance model has been adopted to take into account dynamic self-heating, which is detailed in Section 5. In HiCuM/L2, the temperature dependence of parameters for the collector current and emitter back-injection component of the base current is described through the associated saturation currents [12], while the temperature dependence of the zero bias hole charge is fixed by the previously determined capacitance parameters. In order to extract the model parameters, collector and base current measurements with respect to temperature are employed. Gummel plots at $V_{BC} = 0$ V are well suited for this purpose. By applying the same extraction method for measurements at other temperatures, temperature coefficients of the remaining parameters (parasitic resistances, thermal resistance transit time, etc.) can be determined. These temperature-related parameters can play a significant role for advanced technologies for which the self-heating effect becomes increasingly important.

4.2. Geometry Scalable HiCuM Model Simulation of InP DHBTs

Figure 4a,b show the comparison between the measurements and model simulations of the Gummel and the extracted B–E junction capacitances for the geometries under test with an effective emitter area (A_{E0}) varying from 0.5×5 to $0.7 \times 10 \mu\text{m}^2$. Figure 4c shows the scaling of I_C as a function of the emitter length (for the $0.5 \mu\text{m}$ emitter width device) depicting the good accuracy of the scaling laws implemented through Equation (5). Figure 5a shows the temperature dependence of the collector current, at four different temperatures (-40 , 0 , 25 and 35 °C). Figure 5b,c depict the output characteristics for the representative device ($0.7 \times 5 \mu\text{m}^2$) at different forced V_{BE} (high-injection) and I_B . In all cases, good agreement between the experimental data and model simulation is observed, indicating the accuracy of the temperature-related parameters, high-current and self-heating effects.

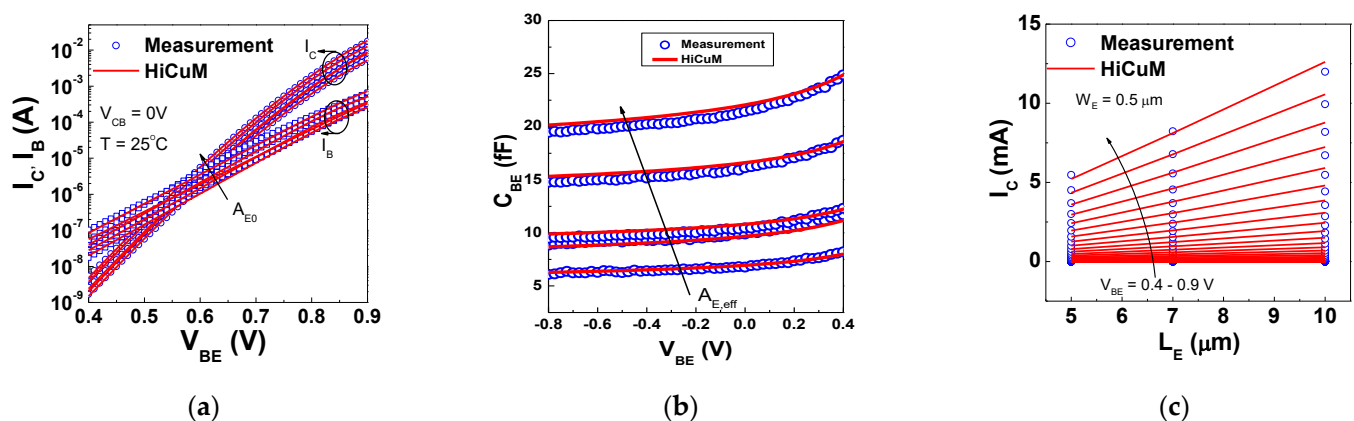


Figure 4. (a) Gummel plots at $V_{BC} = 0$ V; (b) the B–E junction capacitances; and (c) the collector current scaling.

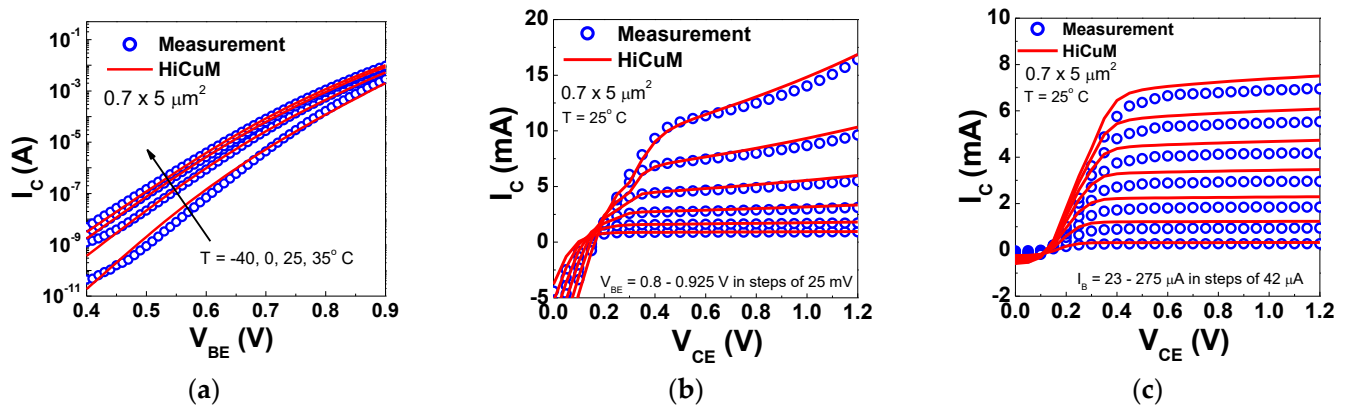


Figure 5. (a) Collector current at different temperatures; output characteristics at forced V_{BE} (a) and at forced I_B (b), for the InP DHBT with an area of $0.7 \times 5 \mu\text{m}^2$.

4.3. UTC Photodiode Compact Model Validation

4.3.1. I–V Characterization and Parameter Extraction

Three UTC-PDs with active areas of $5 \times 15 \mu\text{m}^2$, $5 \times 30 \mu\text{m}^2$ and $7 \times 25 \mu\text{m}^2$ were characterized under a bias sweep in the range of $(-3, 1)$ V. Current–voltage characterizations were performed on each device geometry at three temperatures: 15, 25 and 35 °C. Figure 6 compares measured the DC characteristics and our developed compact model described in Section 3.2, demonstrating good model accuracy over the entire range of forward and reverse bias at different temperatures. The photodiodes present very low dark current levels of around 4, 20 and 55 nA @ -2V for the geometries $5 \times 15 \mu\text{m}^2$, $5 \times 30 \mu\text{m}^2$ and $7 \times 25 \mu\text{m}^2$, respectively, which shows the quality of the fabrication and especially the effective passivation of the photodiode junction. The dark current is very low compared to the photocurrent used for mm-wave generation, which is usually in the mA range to generate sufficient power. Therefore, as the dark current is more than three orders of magnitude below the photocurrent, even if a detailed analysis of the photodiode noise was not realized, we can assume that the impact of a dark current is negligible compared to the global noise of the system. We would like to mention that in order to have a complete view of the impact of the photodiode on the performances of the radio link, one requires the analysis of the nonlinear behavior of the photodiode which is not in the scope of this paper.

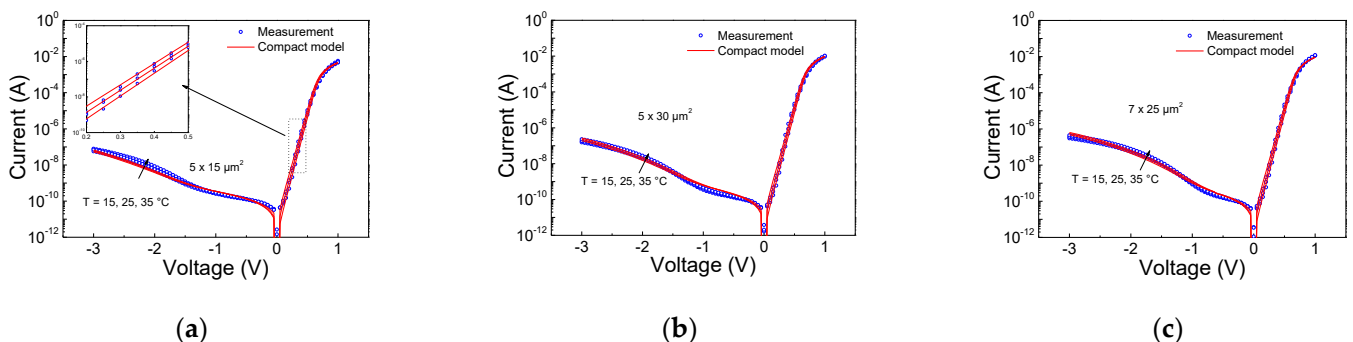


Figure 6. Measured (symbol) and simulated (line) current–voltage–temperature of UTC-PD with an active area of (a) $5 \times 15 \mu\text{m}^2$ (b) $5 \times 30 \mu\text{m}^2$ (c) $7 \times 25 \mu\text{m}^2$.

4.3.2. Photocurrent Characterization

The photocurrent measurements were performed under an optical power ranging between 0 and 9 dBm by illuminating the UTC-PDs with a laser wavelength of 1.55 μm . Figure 7 shows the measured and simulated photocurrents for all geometries under test. We estimated a high responsivity of 0.6 A/W for 15 μm long photodiodes and 0.79 A/W

for 25 and 50 μm -long photodiode. Good accuracy of the photocurrent model, depicted in (4), has been observed. Moreover, good photocurrent scalability is also achieved.

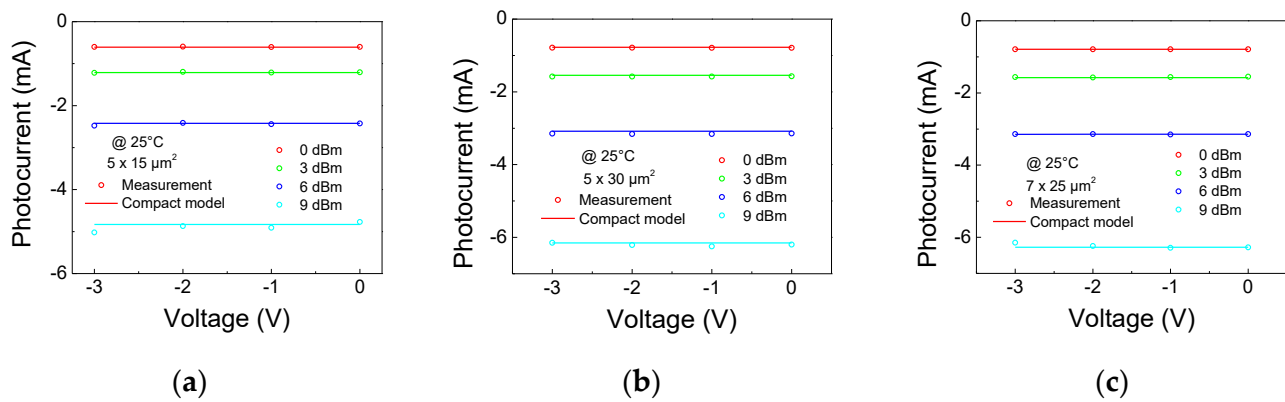


Figure 7. Measured (symbol) and simulated (line) photocurrent of UTC-PD with an active area of (a) $5 \times 15 \mu\text{m}^2$ (b) $5 \times 30 \mu\text{m}^2$ (c) $7 \times 25 \mu\text{m}^2$.

5. Thermal Characterization

Reliability issues such as self-heating and the rise of junction temperature are among the crucial concerns for modern electronic technologies and are becoming increasingly important from the scaling point of view. Additionally, heat-dissipation in photodiodes is also a prominent source of concern that may be coupled to the thermal instability in the electronic part, and can thus further deteriorate the performance of an integrated hybrid monolithic circuit through thermal feedback between the interconnected devices. Thermal management is thus absolutely important for both devices, in order to ensure stable operation. In order to alleviate the thermal issues, thermal impedance modeling approaches have been proposed for InP heterojunction bipolar transistor (HBT) s [14] including the accurate estimation of thermal resistances and thermal R–C network representations. Similar strategies have been adopted for UTC photodiodes, in this work, to provide an estimation of the thermal resistances and ultimately to develop a unified thermal management strategy for monolithic integrated circuits.

5.1. Dynamic Self-Heating and Thermal Impedance Modeling in InP DHBTs

The Low-Frequency S-parameter measurement setup consists of a semiconductor parameter analyzer, HP 4155, for DC biasing and a vector network analyzer, Agilent E5061B (5 Hz–3 GHz). In order to couple RF and DC bias, bias tees (bandwidth of 30 kHz to 3 GHz) were used. The dynamic self-heating is observed in the 30 kHz–300 MHz range where thermal impedance is extracted. A standard short-open-load-thru (SOLT) calibration was used with an RF input power of -28 dBm, followed by open-short de-embedding. DC bias points were chosen with higher V_{BE} and V_{CE} , where self-heating effects are dominantly visible.

5.1.1. Thermal Impedance Extraction Method from Low-Frequency S-Parameters

Figure 8 shows the magnitude and the phases of the Y_{12} -parameters of one of the HBT geometries ($0.7 \times 5 \mu\text{m}^2$) under test, depicting two distinct zones over the entire frequency range, separated by a threshold thermal frequency (f_{TH}) around 0.1 GHz. This frequency denotes a phase shift at the minimum amplitude of the Y_{12} -parameter. The first region (frequencies higher than f_{TH}) reflects only static self-heating and the behavior in this region is purely electrical. In the other region, at frequencies below f_{TH} , dynamic self-heating is dominant and electro–thermal networks can be used to extract the thermal impedance. The

extracted Y parameters are used to calculate the normalized thermal impedance using the following [14]:

$$Z_{TH,norm}(\omega) = \left(\frac{Y_{22}(\omega) - Y_{22}^{AC}}{Y_{22}^{DC} - Y_{22}^{AC}} \right) \left(\frac{I_C + V_{BE}Y_{12}^{DC} + V_{CE}Y_{22}^{DC}}{I_C + V_{BE}Y_{12}(\omega) + V_{CE}Y_{22}(\omega)} \right) \quad (6)$$

where Y_{22}^{AC} corresponds to Y_{22} without dynamic self-heating, i.e., when the thermal capacitance, C_{TH} , is zero, Y_{12}^{DC} and Y_{22}^{DC} are the Y parameters in the DC condition (i.e., $\omega \rightarrow 0$). Here, the units of all Y parameters are in S and I_C , V_{BE} and V_{CE} are expressed in A, V and V, respectively. The extraction of Y_{22}^{AC} has been performed using the HiCuM model simulation, described in the preceding sections, of the Y_{22} parameters with C_{TH} set to zero.

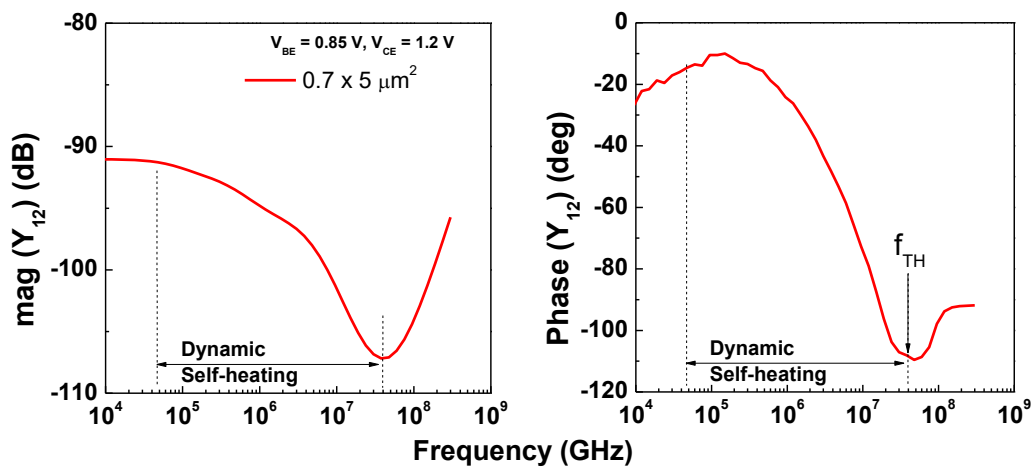


Figure 8. Y_{12} parameter versus frequency showing the zone where dynamic self-heating activates.

5.1.2. Geometry Scalable Thermal Impedance Model

Two scenarios of the pyramidal downward heat flow through the device have been schematically illustrated in Figure 9a,b. The heat diffusion angle, θ , dictates the temperature distribution along the vertical cross section of the device. For an angle $\theta < \theta_C$ (where θ_C is the critical angle at which the heat flow changes from scenario (a) to (b), with $\theta_C = \tan^{-1}[(W_{COL} - W_E)/2D_{ox}]$, with W_{COL} and W_E being the lateral widths of the collector and the emitter, respectively, and D_{ox} is the height of the passivation layer, the heat flow is not stopped by the isolation surrounding the collector and the heat diffusion is pyramidal along the depth of the transistor (Figure 9a). On the contrary, for an angle $\theta > \theta_C$, the heat flow is first blocked by the mesa edge, thus leading to a uniform heat diffusion in one subsection (see Figure 9b), followed by a pyramidal diffusion pattern toward the substrate. Based on previous works [14,19], the heat diffusion angle is found to be always lower than 65° , leading to the heat-flow scenario depicted in Figure 9a. Hence, for the rest of the thermal modeling approach, scenario (a) was considered. Following our previous modeling approach [14] to obtain an optimal representation of the behavior of dynamic self-heating in the DHBTs, we considered three major vertical sections of the heat diffusion, which included the collector region beneath the heat source located at the B–C junction, the sub collector and the substrate. The upward heat flow through the emitter metal layers is represented only by a thermal resistance, R_{THM} , in parallel with the remaining electrical part, as shown in Figure 9c. The emitter-metal layer thermal resistance is calculated in a similar manner as the intrinsic device, considering three different thermal conductivities of the emitter layers: InP, InGaAs (indium gallium arsenide) and TiPdAu [20]. A modified Foster-like thermal network was used to represent heat diffusion through these three sections, as illustrated in Figure 9d. Considering the average thermal conductivity for

each section, one can write the following expressions for the thermal resistances of each subsections [14]:

$$\begin{aligned}
 R_{THF,1} &= \frac{1}{2\tan\theta(L_E - W_E)\kappa_{avg1}} \ln \left[\frac{L_E(W_E + 2h_1\tan\theta)}{W_E(L_E + 2h_1\tan\theta)} \right] \\
 R_{THF,2} &= \frac{1}{2\tan\theta(L_E - W_E)\kappa_{avg2}} \ln \left[\frac{(L_E + 2h_1\tan\theta)(W_E + 2(h_1 + h_2)\tan\theta)}{(W_E + 2h_1\tan\theta)(L_E + 2(h_1 + h_2)\tan\theta)} \right] \\
 R_{THF,3} &= \frac{1}{2\tan\theta(L_E - W_E)\kappa_{avg3}} \ln \left[\frac{(L_E + 2(h_1 + h_2)\tan\theta)(W_E + 2t_{si}\tan\theta)}{(W_E + 2(h_1 + h_2)\tan\theta)(L_E + 2t_{si}\tan\theta)} \right]
 \end{aligned} \tag{7}$$

here h_1 , h_2 and h_3 denote the depths of the three regions calculated depending on the geometry and the heat flow angle. W_E and L_E are the effective emitter width and length, respectively, and κ_{avg1} , κ_{avg2} and κ_{avg3} are the average thermal conductivities of the three regions calculated for InP following the approach in [21]. Similarly, the expressions of the thermal capacitances of the three regions are as follows:

$$\begin{aligned}
 C_{THF,1} &= \frac{\kappa_{avg1}}{D_{th}} \left[\frac{4}{3}h_1^3\tan^2\theta + (L_E + W_E)h_1^2\tan\theta + L_E W_E h_1 \right] \\
 C_{THF,2} &= \frac{\kappa_{avg2}}{D_{th}} \left[\frac{4}{3}h_2^3\tan^2\theta + (L_E + W_E + 4h_1\tan\theta)h_2^2\tan\theta \right. \\
 &\quad \left. + (L_E + 2h_1\tan\theta)(W_E + 2h_1\tan\theta)h_2 \right] \\
 C_{THF,3} &= \frac{\kappa_{avg3}}{D_{th}} \left[\frac{4}{3}h_3^3\tan^2\theta + (L_E + W_E + 4h_2\tan\theta)h_3^2\tan\theta \right. \\
 &\quad \left. + (L_E + 2h_2\tan\theta)(W_E + 2h_2\tan\theta)h_3 \right]
 \end{aligned} \tag{8}$$

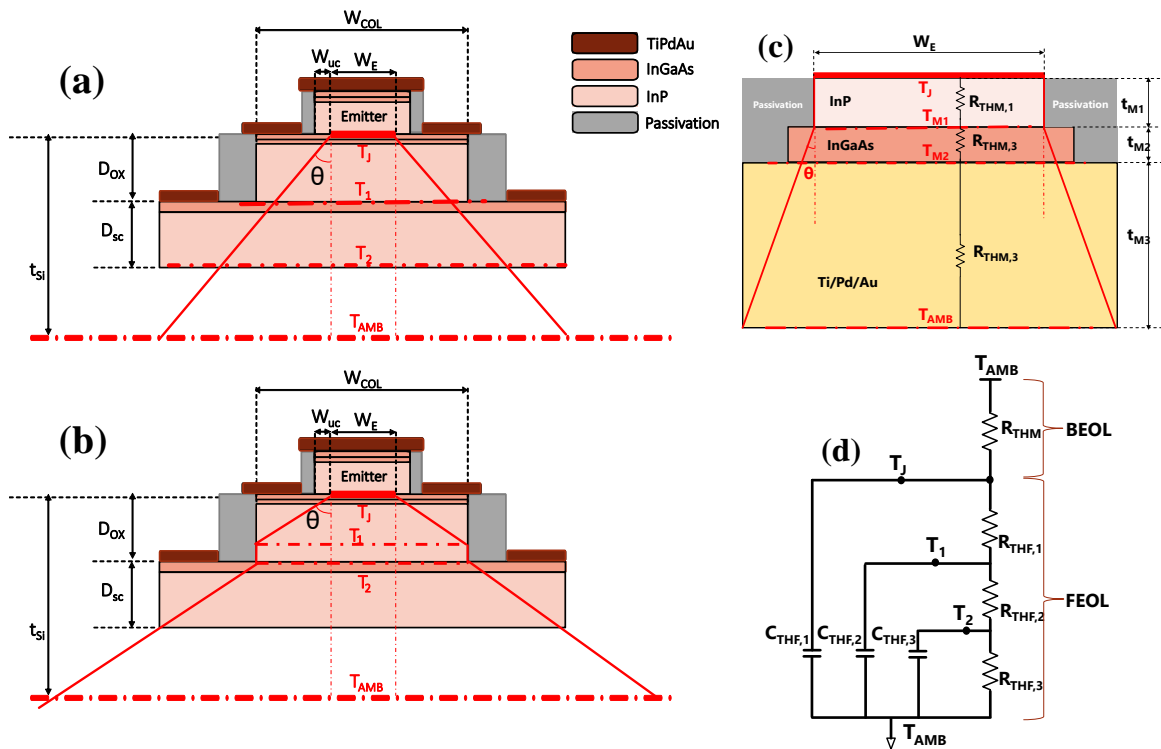


Figure 9. Two scenarios of heat flow through the HBT structure (a) $\theta < \theta_c$, (b) $\theta > \theta_c$; distributed electro-thermal network for the (c) upward and (d) downward heat flow.

The complete electro-thermal network including both downward and upward heat diffusion, replaces the one-pole thermal network in HiCuM compact model to estimate the junction temperature more accurately. In Equations (7) and (8), the thermal resistances ($R_{THF,1}$, $R_{THF,2}$, $R_{THF,3}$) are expressed in K/W, thermal capacitances ($C_{THF,1}$, $C_{THF,2}$, $C_{THF,3}$) in pJ/K, average thermal conductivities (κ_{avg1} , κ_{avg2} and κ_{avg3}) in $W.m^{-1}, K^{-1}$, θ in degrees, heat diffusion coefficient D_{th} in m^2/s and all geometrical dimensions are expressed in m.

5.1.3. Thermal Impedance (Z_{TH}) Extraction and Model Validation

Low-frequency S-parameters have been measured on six device geometries. Figure 10 illustrates the results comparing the magnitudes and phases of the measured low-frequency Y-parameters (symbols), Y_{12} and Y_{22} , and the scalable thermal model simulation (solid lines) for different device geometries. The results are shown for a bias condition of $V_{BE} = 0.85$ V and $V_{CE} = 1.2$ V, chosen specifically around peak f_T of the transistors, where self-heating becomes dominant. Both Y-parameters show good agreement between the measurement and the simulation results. Furthermore, good model scalability has been observed across all geometries.

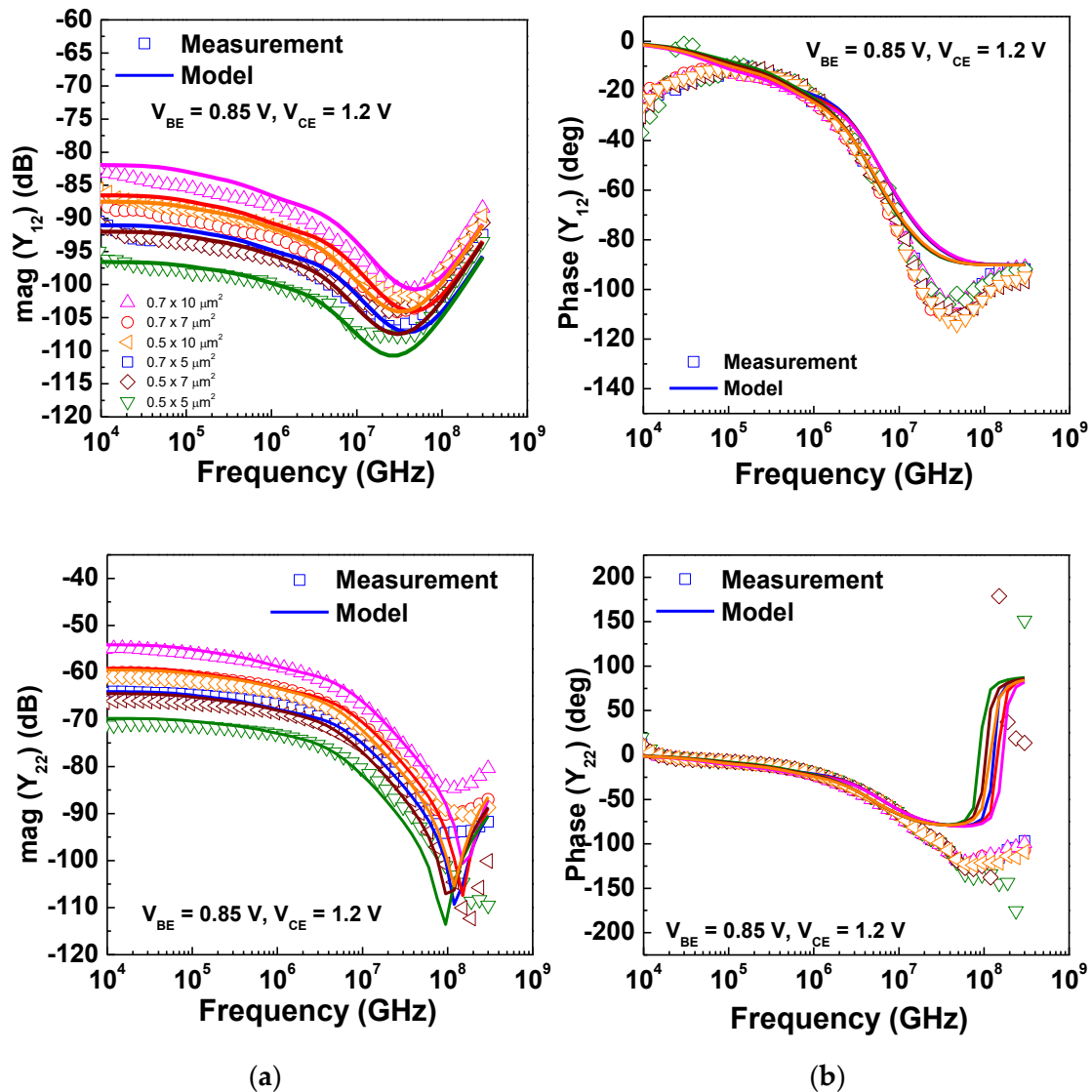


Figure 10. Comparison of the magnitudes (a) and phases (b) of the measured low-frequency Y-parameters (solid symbols), Y_{12} and Y_{22} , and the scalable thermal model simulation (solid lines) for different geometries.

Figure 11 presents the magnitudes of the thermal impedance, Z_{TH} , extracted using (6), comparing the measurements (solid symbols) and the scalable thermal impedance model simulation (solid lines), depicting good model accuracy and scalability. Figure 11a shows the magnitude of the Z_{TH} for emitter length scaling for the fixed emitter width of (a) 0.7 μm and (b) 0.5 μm . In both cases, the model describes the behavior of the dynamic self-heating (below f_{TH}) quite well.

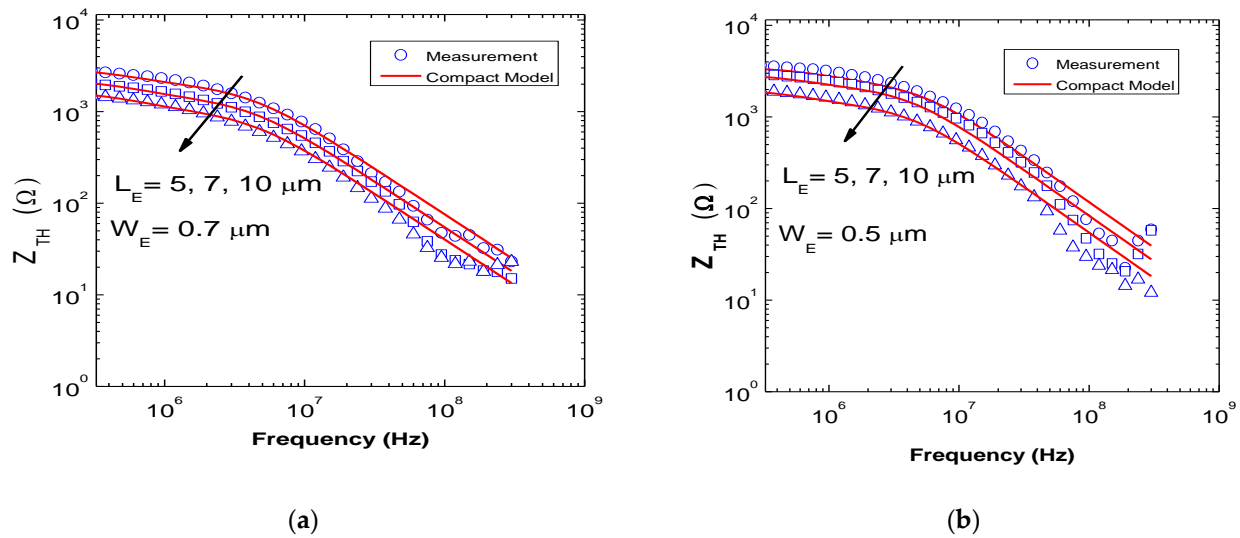


Figure 11. Magnitudes of the thermal impedance, Z_{TH} , for two emitter width $W_E = 0.7 \mu\text{m}$ (a) and $0.5 \mu\text{m}$ (b).

The thermal resistances and capacitances for the three regions of the intrinsic device are shown in Table 1, extracted from compact model simulations, for six geometries with different emitter lengths and two chosen emitter widths of 0.5 and 0.7 μm . The total thermal resistance is calculated taking into account both intrinsic devices and the contribution from the emitter metal layers, R_{THM} . R_{TH} is extracted from the measurement using the intersection technique [14]. The extraction results are shown in Table 2 for all geometries, depicting a very good estimation of the thermal resistances by the developed model.

Table 1. Thermal resistance and capacitance contributions from the different epitaxial layers of the DHBT.

Device Area (μm^2)	0.5×5	0.5×7	0.5×10	0.7×5	0.7×7	0.7×10
R_{TH1} (K/W)	3680	2910	1980	2714	1865	1456
R_{TH2} (K/W)	1195	1095	777	1297	1108	856
R_{TH3} (K/W)	920	768	680	868	825	773
C_{TH1} (pJ/K)	12.5	17	29	21	28	43
C_{TH2} (pJ/K)	140	215	320	165	220	340
C_{TH3} (nJ/K)	1.75	1.9	2.23	1.9	2.13	2.45

Table 2. Thermal resistances extracted from the thermal impedance model and measurements.

Device Area (μm^2)	0.5×5	0.5×7	0.5×10	0.7×5	0.7×7	0.7×10
R_{THF} (K/W)	5795	4773	3437	4879	3798	3085
R_{THM} (K/W)	17,500	12,050	9800	11,050	9250	6960
R_{TH} (model) (K/W)	4353	3418	2544.6	3384	2687	2137
R_{TH} (measured) (K/W)	4114	3257	2526	3675	2720	2289

5.2. Thermal Characterization and Modeling of UTC Photodiodes

To take into account the self-heating effect in the UTC photodiodes, a classical thermal network, consisting of a thermal resistance and capacitances, has already been implemented in the compact model, as described in [13]. From the extraction point of view, the thermal resistance, R_{th} , of this network can be estimated using the following equations [22]:

$$\frac{I_d}{V_d} - \frac{Nk_B T_j}{qI_d} \ln\left(\frac{I_d}{I_s(T_j)}\right) = R - \frac{Nk_B T_j}{qI_d} \quad (9)$$

with

$$T_j = T_{amb} + R_{th} \cdot I_d \cdot V_d \quad (10)$$

where I_d and V_d are the current (in A) and voltage (in V) across the UTC-PD, N is diode current ideality factor, k_B is the Boltzmann constant (in eVK^{-1}), T_j and T_{amb} are the junction and ambient temperatures (both in K), respectively, q is the electronic charge (in C), I_s is the reverse saturation current (in A) and R is the total resistance (in Ω) in series with the photodiode. The parameters in Equation (9) have been extracted under high-current injection (at 1 V) conditions, where self-heating occurs. In order to converge on a solution for T_j from both sides of Equation (9), an iteration of the values of R_{th} was performed to solve the expression. In order to facilitate optimal convergence, the model parameters I_s , N or R were slightly varied, within an acceptable tolerance that is summarized in Table 3. Subsequently, the extracted values of the thermal resistances of the UTC-PDs are also summarized in Table 3. Interestingly, the extracted values of the thermal resistances of the UTC-PDs are not significantly different (slightly higher) from what can be predicted for these geometries using the R_{TH} scaling law implemented for the DHBTs. Since the two technologies have been developed by the same foundry with similar epitaxial compositions and similar substrate thermal conductivity (InP), the results are coherent and promising for achieving homogeneous monolithic integration with the two devices. Despite the reasonable R_{TH} values obtained for the UTC-PDs, further model improvement and refinement of the extraction methodology lie within the scope of future work.

Table 3. Thermal parameter values according to the UTC-PD dimensions.

Dimensions.	Parameters	Model	Standard Deviation	R_{Th} (K/W)
$5 \times 15 \mu\text{m}^2$	$R(\Omega)$	60.58	± 2	1013
	$I_s(\text{A})$	4.6×10^{-12}	$\pm 0.4 \times 10^{-12}$	
	N	1.365	± 0	
$5 \times 30 \mu\text{m}^2$	$R(\Omega)$	36.31	± 5	844
	$I_s(\text{A})$	8.77×10^{-12}	$\pm 0.07 \times 10^{-12}$	
	N	1.363	± 0	
$7 \times 25 \mu\text{m}^2$	$R(\Omega)$	27.7	± 2	612
	$I_s(\text{A})$	6.6×10^{-12}	$\pm 0.1 \times 10^{-12}$	
	N	1.360	± 0.03	

As emphasized earlier, unlike the HBT modeling framework, which has been refined and standardized for a long time, the UTC compact modeling approach is under development and still has several aspects to improve. While the current framework is reasonably accurate, further improvements can include the addition of more material parameters, the description of photocurrent saturation and the more in-depth analysis of self-heating.

6. High Frequency Characterization and Modelling

Since monolithic integrated optoelectronic circuits are targeted to operate at terahertz frequencies in beyond 5G communication systems, it is crucial to analyze the performances of the electronic and photonic devices at a very high frequency of operation. The difficulties of this approach lie with the conventional test-structures and on-wafer characterization setup that often suffer from characterization technique, calibration and de-embedding techniques adapted to (sub) millimeter-wave frequency bands. The extrapolation of measurements to higher frequencies can often lead to errors and even the models might lack additional effects that can only be understood from actual measurements beyond 200 GHz. Hence, this section sheds light on this aspect through test structure design strategies, in order to correctly “de-embed” the real intrinsic device characteristics, as well as to demonstrate model validity in comparison with the on-wafer measurements performed at very high frequencies.

6.1. High Frequency Characterization of InP DHBTs

6.1.1. Dedicated Test Structure Design

An on-wafer thru-reflect-line (TRL) calibration kit was developed and implemented in the InP DHBT process. Its purpose is to allow on-wafer RF transistor measurements beyond 110 GHz. In fact, at such high frequencies, conventional calibration methods fail to provide sufficiently accurate measurements as demonstrated in [23], by comparing short-open-load-thru (SOLT) on commercial calibration substrate on alumina and on-wafer TRL calibrations up to 500 GHz. Thus, on-wafer calibrations are of particular interest for device characterization in the sub-millimeter-wave frequency ranges [24].

In [25], coplanar waveguide (CPW) transmission lines in InP technology proved to be suitable for on-wafer TRL calibration for InP DHBT characterization up to 500 GHz. Hence, the same methodology for designing calibration structures was applied to the III–V Lab InP DHBT process (Figure 12). As shown in Figure 12, the calibration kit contains one 50 Ω Thru and two 50 Ω Lines of length 180 and 120 μm , covering, respectively, the bandwidths of 35–315 GHz and 70–630 GHz for the TRL calibration. The layout of the RF pads allowed a probing pitch of 50–100 μm . After the on-wafer TRL calibration, the reference plane is set at the inner edge of the pads (see Figure 12b), which is also the beginning of the 50 Ω Thru standard. Hence, the RF pads are included in the calibration error terms.

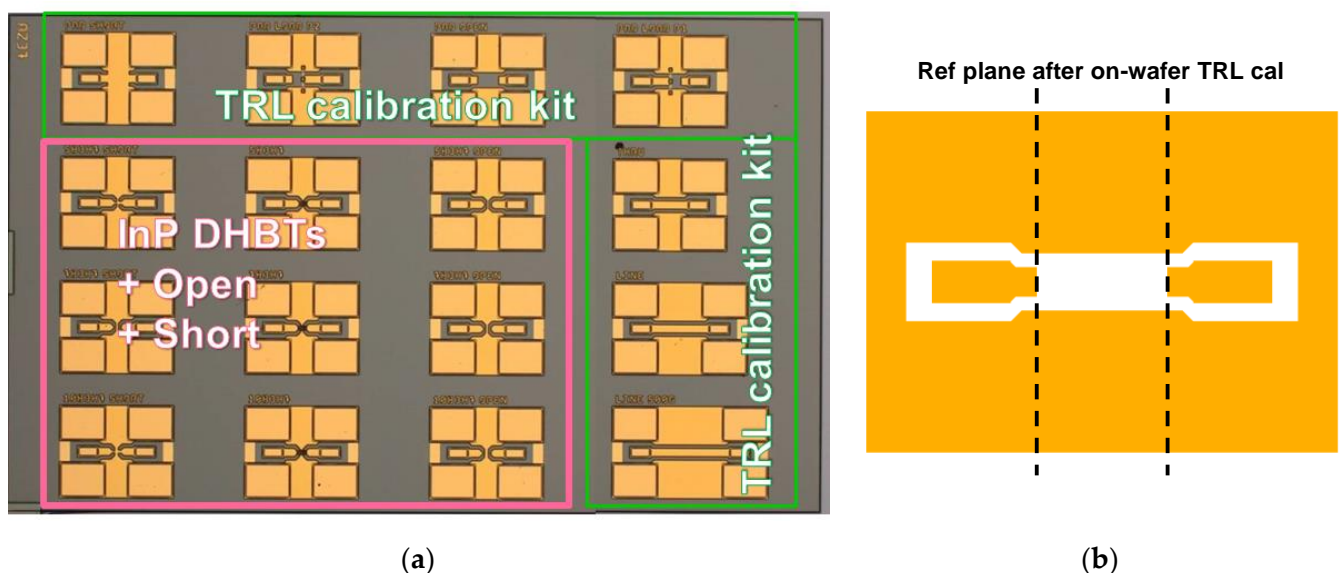


Figure 12. (a) InP DHBT test structures for measurements beyond 110 GHz; (b) Layout view of the Pad-Open.

6.1.2. Measurement Results and HiCuM Compact Model Validation Up to 330 GHz

The HiCuM model parameter extraction was performed with S-parameter measurements up to 40 GHz and validated against the measurements up to 330 GHz. Among these two separate measurement campaigns, the former was dedicated to parameter extraction while the latter targets high-frequency characterization and model validation. The HiCuM compact model scalability was first verified with RF measurements up to 40 GHz. Five different geometries of transistors were measured and the transit frequency, f_T , was extracted at 15 GHz for different bias points. The complexity of the HiCuM model requires a systematic extraction of device parameters, especially when different parameters are strongly correlated at high-current conditions. Hence, the interlinked parameter extraction flow described in Section 3 has been used to extract the parameters related to transit time along with the capacitance and current parameters. Moreover, the temperature-related parameters are also extracted for each quantity at all steps. The comparison between the measurement and simulation results is depicted in Figure 13a. A good agreement is observed between the measurements and the geometry-scalable compact model simulation

with HiCuM, where the $0.7 \times 5 \mu\text{m}^2$ InP DHBT presented the maximum RF performance. The corresponding Gummel plot and static gain are shown in Figure 13b.

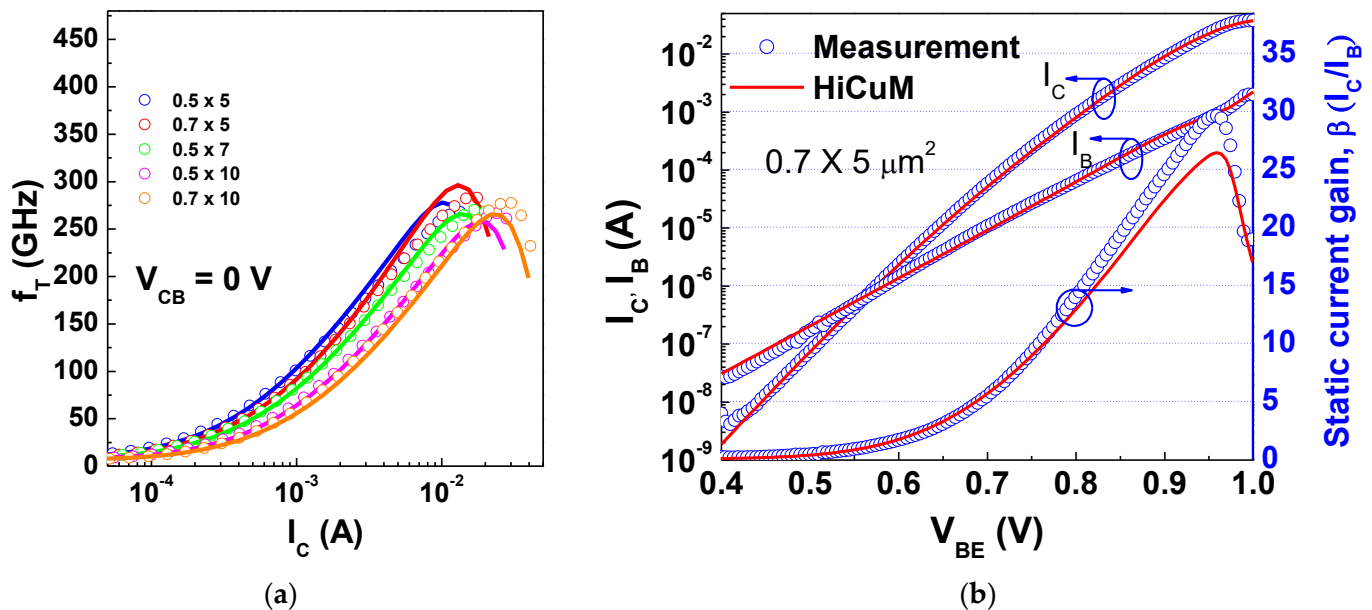


Figure 13. (a) Measured and simulated f_T versus I_C for several transistor geometries; (b) Gummel plots and static current gain curve superimposition between measurement and HiCuM simulation.

Then, the S-parameter measurements were carried out up to 330 GHz using three measurement benches: (i) up to 110 GHz using an Agilent® E8361 PNA, with frequency extenders for the 67–110 GHz frequency range; (ii) in the G-band (140–220 GHz) and J-band (220–330 GHz) using a Rohde & Schwarz® ZVA24, coupled with Rohde & Schwarz® frequency extenders. Hence, Picoprobe® probes were used in the 1–110 GHz and J-band, and Cascade Infinity® probes in the G-band.

As mentioned earlier, the transistor under test has an emitter length of $5 \mu\text{m}$ and an emitter width of $0.7 \mu\text{m}$, since it showed the maximum current gain among all the geometries measured. The measurements were made up to 330 GHz using on-wafer TRL calibration. The transistor was biased under a fixed 1.6 V collector-to-emitter voltage and a sweep of the base-to-emitter voltage from 830 to 910 mV with a 10 mV-step. The maximum gain is obtained for $V_{BE} = 910$ mV.

The gain curves, cut-off frequencies and S-parameters are depicted in Figure 14, where a comparison is drawn between the measured quantities and the ones obtained after simulation of the HiCuM compact model up to 330 GHz. A pretty good agreement can be observed between measurement and simulation up to 330 GHz for the different bias points. Interestingly, a slight discrepancy can be observed between the measurement and the HiCuM simulation for the Mason's gain (Figure 14b). This is due to the limitation of the TRL calibration below 35 GHz. The design of the on-wafer TRL calibration kit focuses on the very high-frequency measurements beyond 110 GHz, and due to the constraints of wafer area, a compromise was made in selecting the line dimensions to be fabricated. Hence, a maximum length of $180 \mu\text{m}$ (equivalent to a minimum frequency of 35 GHz) was chosen for the lines. In addition, due to the high sensitivity of the measurements of the Mason's gain, even the slightest variation in the measurement environment may lead to deviation from what is predicted by the model. Despite the use of three different on-wafer probing setups, an excellent band continuity could be achieved among the measurement frequency bands.

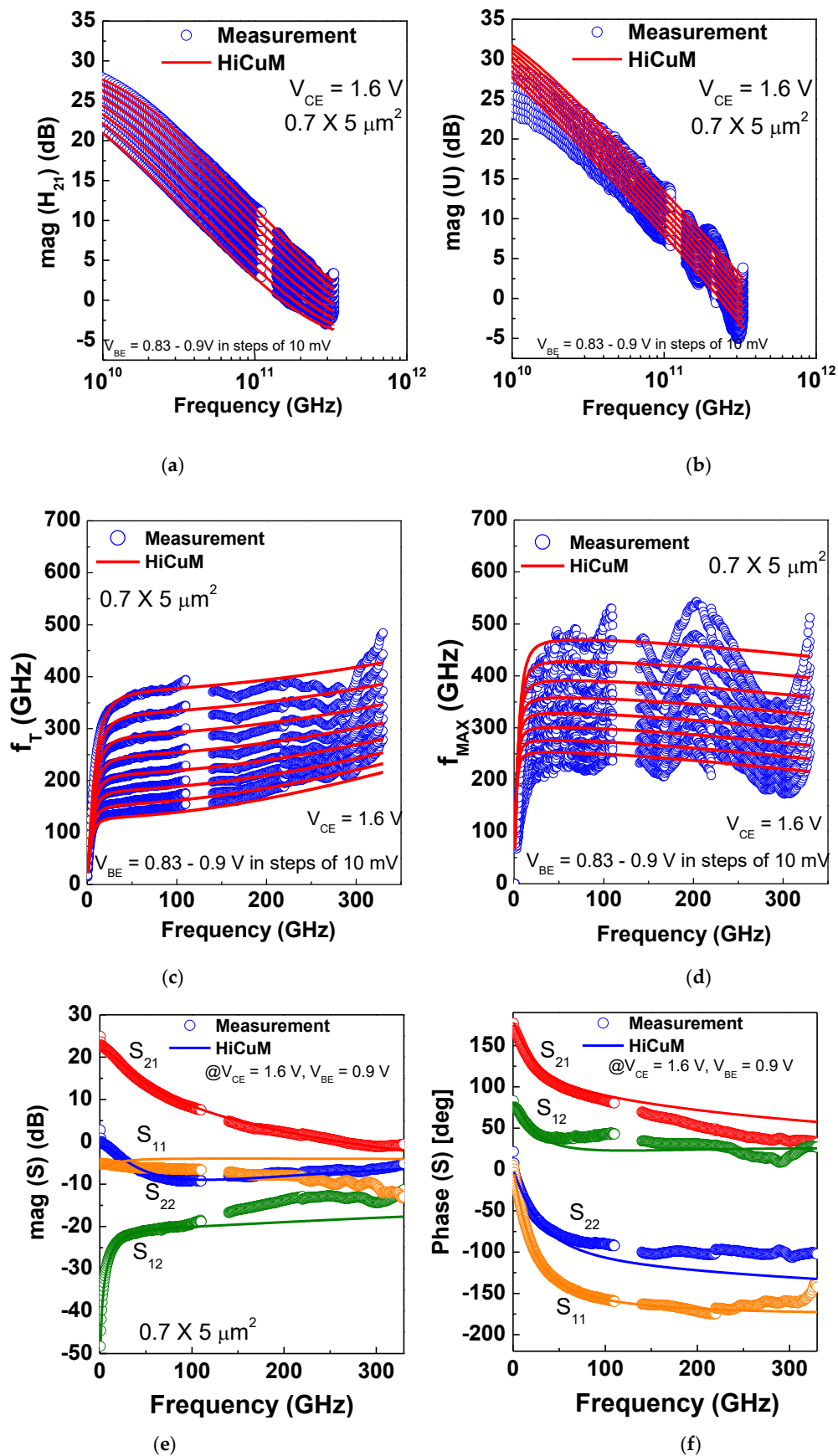


Figure 14. Comparison between HiCuM extrapolation and measurements up to 330 GHz: (a,b) gain curves, (c,d) cut-off frequencies and (e,f) S-parameters at peak f_T .

Overall, this demonstrates again the accuracy of the HiCuM compact model to accurately reproduce the behavior of InP DHBT transistors in the sub-millimeter-wave frequency range, provided accurate and reliable measurements are performed with on-wafer TRL calibration.

6.2. High-Frequency Characterization of UTC Photodiodes

6.2.1. Extrinsic Elements

The pads and the coplanar waveguide (CPW) transmission lines have been modeled using a network of lumped elements located in the extrinsic part of the model. The extrinsic circuit includes the series resistance R_p , the inductance, L_p and the capacitance, C_p .

In order to extract the values of these parasitic lumped elements, UTC-PD test structures in open (Figure 15a) and short (Figure 15b) configurations are characterized. One-port S-parameter measurements were performed up to 40 GHz with an RF power of -25 dBm using a vector network analyzer (VNA). Figure 16 shows the Smith chart depicting the measured reflection coefficients for the open and short test structures. From the measured real (Re) and imaginary (Im) parts of the Y (in S) and Z_{11} (in Ω) parameters of the open and short structures, the values of C_p (in F), L_p (in H) and R_p (in Ω) can be extracted using the following expressions:

$$C_p = \frac{\text{Im}(Y_{\text{open}})}{\omega}, L_p = -\frac{1}{\text{Im}(Y_{\text{short}})\omega} \text{ and } R_p = \text{Re}(Z_{11_{\text{short}}}) \quad (11)$$

The average values of resistance R_p , C_p and L_p extracted at high frequency are summarized in Table 4.

Table 4. Extracted parameter values of the UTC-PD de-embedding test structures.

C_p (fF)	L_p (pH)	R_p (Ω)
26	61.5	1.5

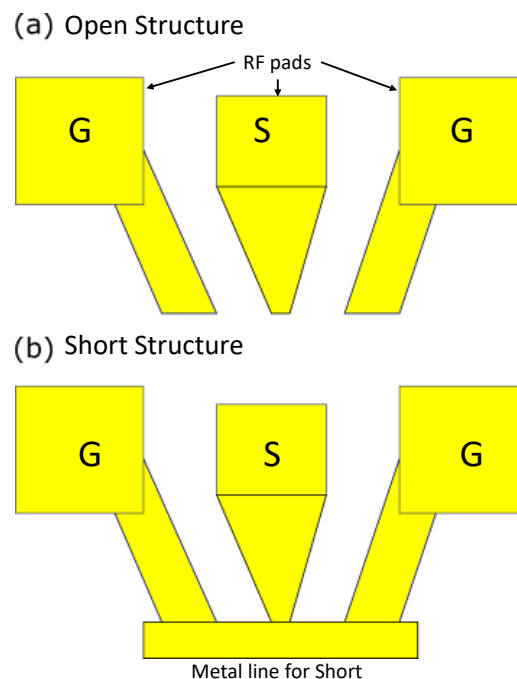


Figure 15. RF test structures with Ground-Signal-Ground (G-S-G) pads: (a) open and (b) short.

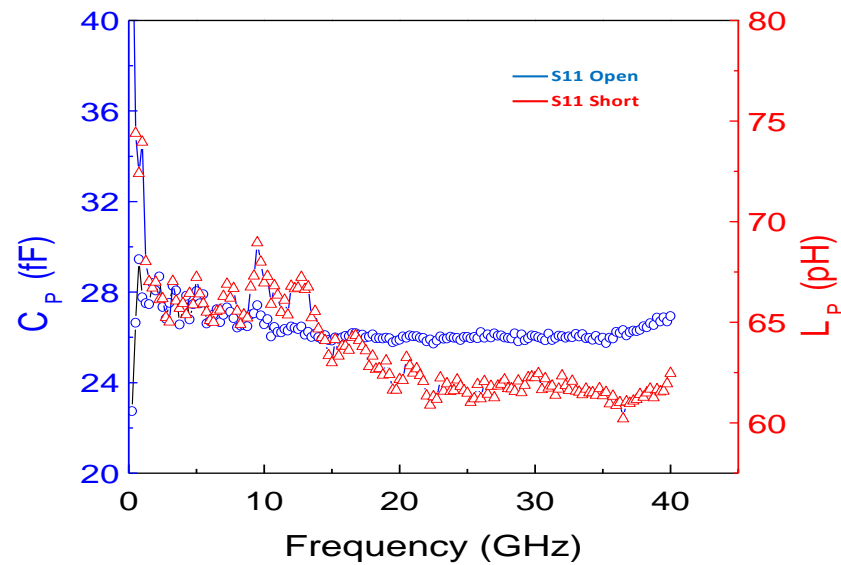


Figure 16. Measured S_{11} for open (blue) and short (red) patterns.

6.2.2. De-Embedding (Extraction of Parasitic Elements)

The process flow of the on-wafer RF measurements and the parameter extraction is summarized in Figure 17. First, the S -parameters of the open and short test structures are measured up to the targeted frequency. Then, one-port S -parameters of the UTC-PDs are measured under various bias conditions. This is followed by an open-short de-embedding process to extract the intrinsic frequency-dependent behavior of the UTC-PD.

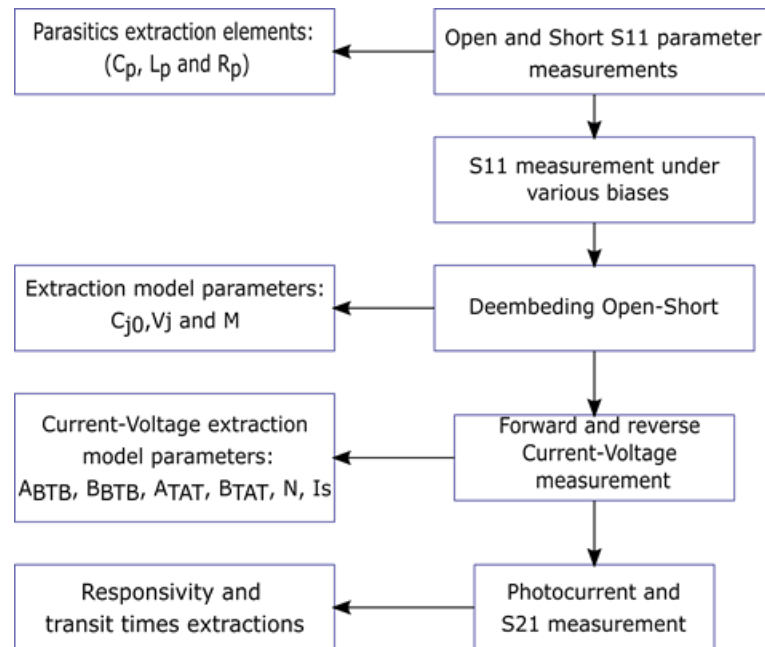


Figure 17. The flow chart of measurements and parameters extraction process.

The intrinsic admittance of a device (Y_{int}) can be extracted from the measured total admittance of the device (Y_{tot}), by subtracting the admittance of the measured open (Y_{open}) and short (Y_{short}) test structures. The following extraction step is the model optimization of the magnitude and the phase of the S_{11} under different bias to extract the frequency as well as the bias dependence of the junction-related parameters of the UTC-PD. One-port S -parameters, measured up to 40 GHz under a bias range of 0 to -2 V, are shown in

Figure 18 for the three geometries under test, comparing the de-embedded experimental data and the compact model simulation, affirming a good model accuracy over the entire frequency and bias range.

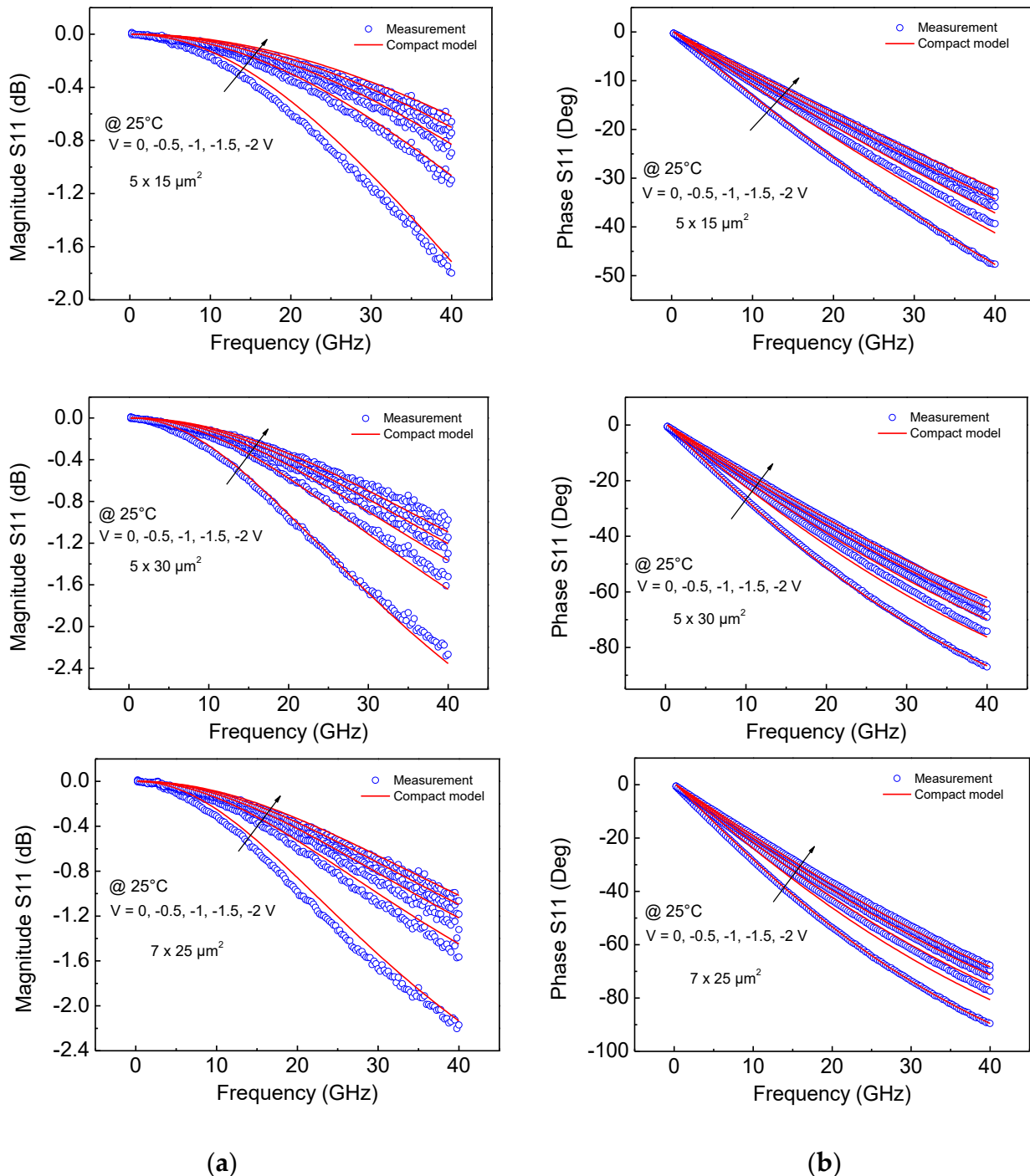


Figure 18. Measured (symbol) and simulated (line) S_{11} parameter for three geometries 5×15 , 5×30 and $7 \times 25 \mu\text{m}^2$: (a) magnitude, (b) phase.

6.2.3. Optical Frequency Response

The optical frequency response of the photodiodes was measured using a heterodyne bench measurement setup. All UTC-PDs were biased at -2 V under a photocurrent of 1 mA. In addition, 3-dB bandwidths of above 35 GHz for the largest geometry, $7 \times 25 \mu\text{m}^2$,

and about 50 GHz for the smallest UTC-PD geometry, $5 \times 15 \mu\text{m}^2$, can be observed in Figure 19. The model simulation shows good agreement with the measured data validating the accuracy of Equation (4) implemented in the model.

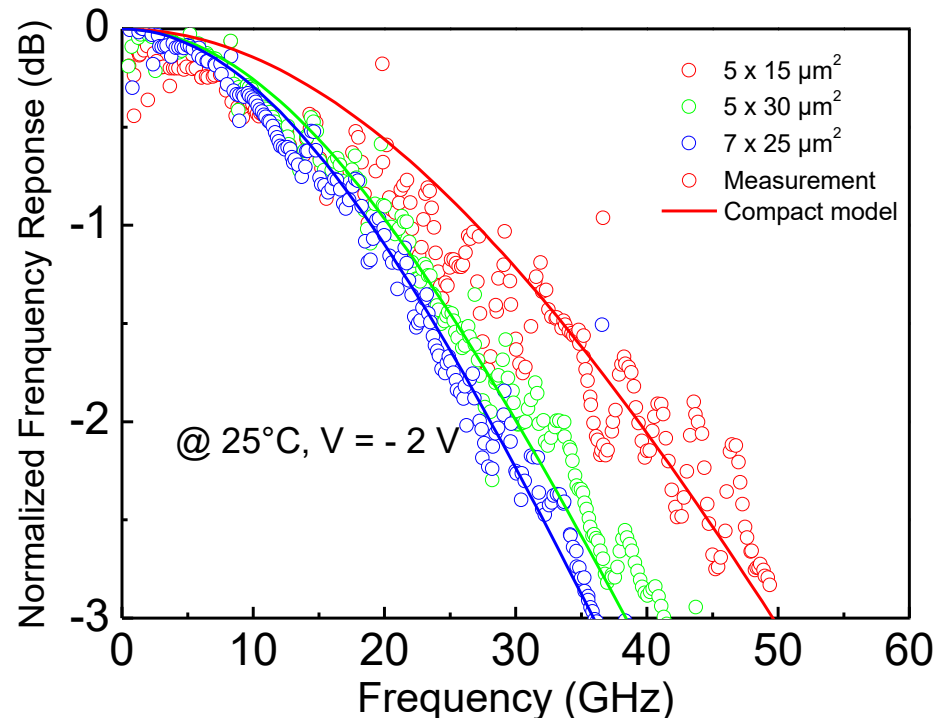


Figure 19. Measured (symbol) and simulated (line) normalized frequency response of UTC-PD with geometries of $5 \times 15 \mu\text{m}^2$ (red symbol), $5 \times 30 \mu\text{m}^2$ (green symbol) and $7 \times 25 \mu\text{m}^2$ (blue symbol).

7. Co-Simulation for Design of Future Electronic–Photonic Integrated Circuits and Performance Prediction

While the previous sections presented detailed characterization and compact modeling approaches of the individual electronic and photonic modules, in order to develop a predictive, multiphysics simulation framework for the OEICs, in-depth understanding of underlying transport mechanisms is crucial. With that in mind, this section provides insights into these aspects through a complementary TCAD simulation framework, performance evaluation using compact model extrapolation to scaled dimensions and ultimately a unified reliability-aware design methodology for the conception of the OEICs.

7.1. TCAD and Monte Carlo Simulations

To strengthen the physical basis of the developed compact models, numerical simulations can be used to unravel the principles of additional effects. For example, the high-frequency S -parameters show a deviation from the expected behavior especially at very high V_{CE} and beyond 200 GHz, in comparison with the measurements obtained at low to medium V_{CE} (around 1V). The observed discrepancies between the experimental measurements and the HiCuM model at high V_{CE} have been investigated using a calibrated multi-scale TCAD model [26]. By combining a full-band, atomistic, and ballistic quantum transport (QT) solver [27] with the hydrodynamic (HD) model of the Sentaurus Device (S-Device) tool [28], qualitatively and quantitatively reliable agreements between the simulated and the experimental data can be produced. Utilizing the configured simulation framework, the influence of a high electric field in the collector region is studied. Figure 20a shows the bulk bandstructure of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, as calculated with tight-binding after calibrating the model with the recommended band gap energies of Ref. [29]. The position of the different valleys of $\text{In}_x\text{Ga}_{1-x}\text{As}$ are plotted as a function of the Indium composition x

in Figure 20b. Note that to achieve a balanced agreement among all targeted parameters, slight discrepancies exist in the calculated and recommended bandgaps, especially in E_X . However, the bowing parameters obtained from our tight-binding approach remains in the recommended range.

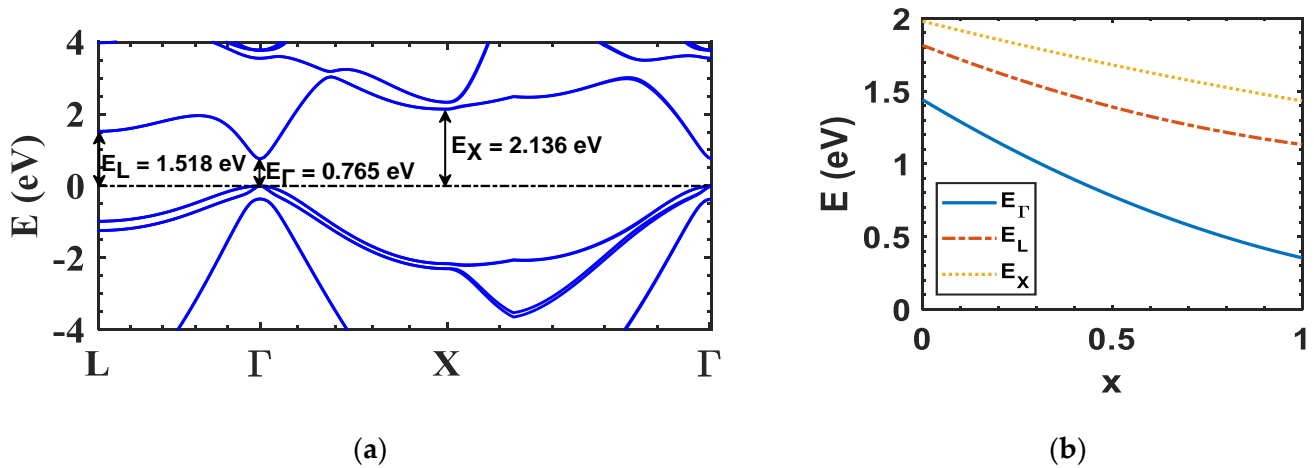


Figure 20. (a) Simulated bulk bandstructure of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$; (b) energy level of the different valleys of $\text{In}_x\text{Ga}_{1-x}\text{As}$ as a function of x [30].

After calibrating the bandstructure model, the conduction band diagrams of the considered DHBT have been simulated at different V_{CE} with S-Device, as shown in Figure 21a. As V_{CE} goes from 1 to 2 V, the conduction bands in the collector region are pushed downwards and the electric field at the base–collector interface increases. These potential profiles have then been inserted into a QT solver to compute the electron distribution inside the active E–B–C domain. Results are summarized in Figure 21b. For $V_{CE} > 1.6$ V, a significant increase in the electron concentration inside the collector region is observed. The origin of this phenomenon has been investigated utilizing the energy and spatially resolved electronic distribution inside the simulated structure, as depicted in Figure 21c,d. At low V_{CE} (Figure 21c), most of the electrons are confined in the emitter region, while the base and collector electron concentrations are almost constant and relatively low. However, as the electric field increases with V_{CE} , electrons situated in the Γ valley start to be transferred to two of the six X valleys, those that can be reached without scattering, i.e., those whose principle axis is aligned with the electron transport direction. This can be directly observed in Figure 21d. In contrast to Figure 21c, the region with the highest electron density in Figure 21d is located in both the emitter region and the X valley of the collector. The transfer of electrons from the Γ to the X valleys is commonly observed in III–V materials, where the electronic occupancy probability of the X valleys increases with electric field [29]. It should be noticed that the transition of electrons from the Γ to the L valleys could also contribute to the observed charge increase, but this would require the absorption or emission of a phonon to compensate for the momentum mismatch. The probability for such events to occur is much lower than the elastic transfer of electrons from Γ to X .

A discrepancy between the experimental and theoretical onset of this effect can nevertheless be observed. It can be attributed to the energy level of the X valley, E_X , which, on one hand, is not exactly known, and whose behavior, on the other hand, is not accurately reproduced by our tight-binding model.

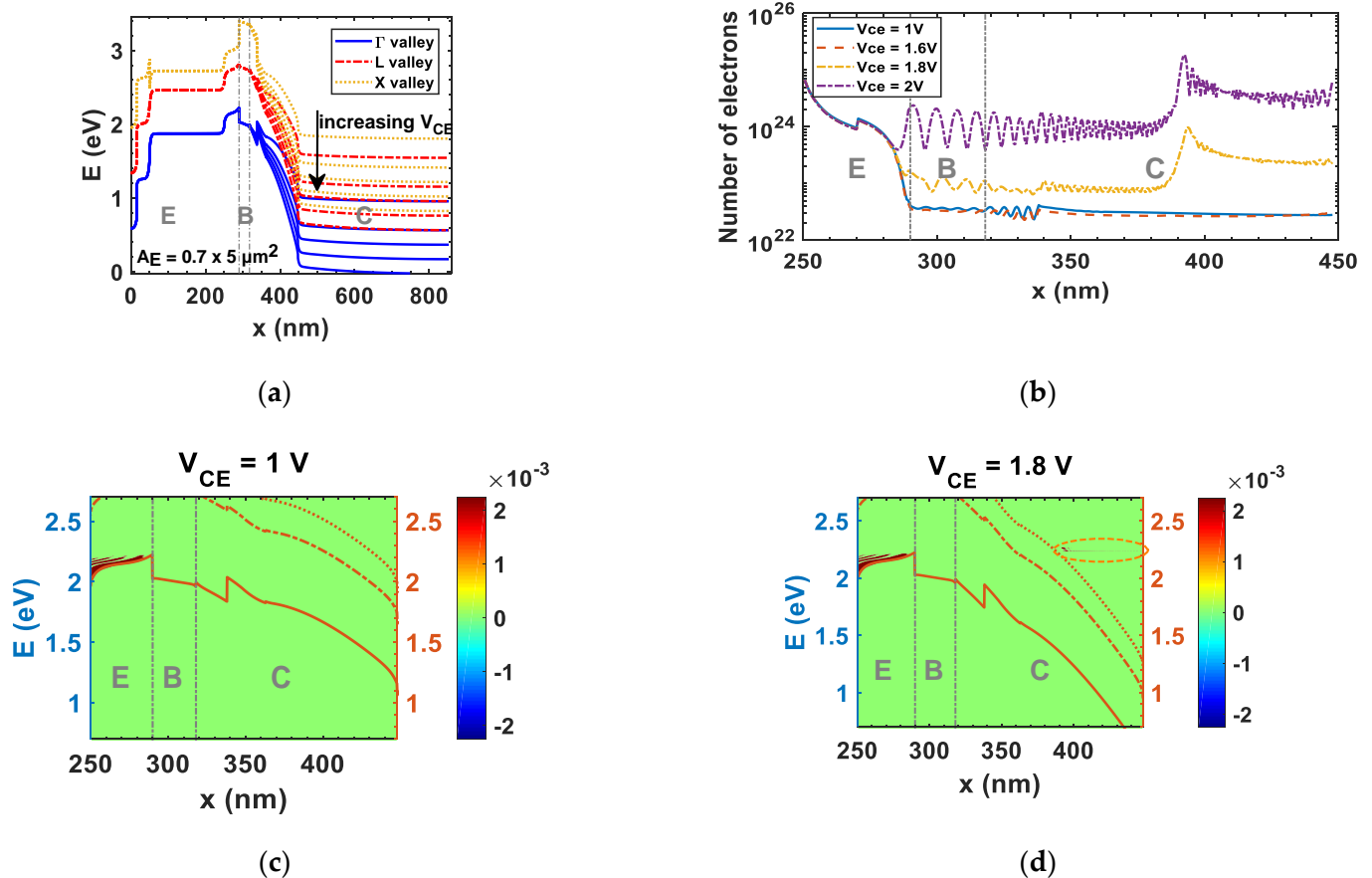


Figure 21. (a) Simulated conduction band diagrams of the considered DHBT with increasing V_{CE} (1, 1.4, 1.6, 1.8 and 2 V) at $V_{BE} = 0.9$ V; (b) spatially resolved electron concentration inside the active E–B–C domain at $V_{CE} = 1, 1.6, 1.8$ and 2 V for $V_{BE} = 0.9$ V; (c) energy and spatially resolved electron concentration $n(x, E)$ inside the active E–B–C region at $V_{CE} = 1$ V, $V_{BE} = 0.9$ V. The solid line refers to the Γ valley, the dashed dotted one to the L valley, and the dashed one to the X valley; (d) same as (c), but at $V_{CE} = 1.8$ V and $V_{BE} = 0.9$ V. The increased number of electrons in the X valley highlighted by the orange dashed oval indicates a significant transfer of electrons from the Γ to the X valleys at high electric field.

7.2. Extrapolation of Figures of Merits to State-of-the-Art ($0.13 \times 2 \mu\text{m}^2$) DHBTs Using Compact Model

Another important aspect of a co-simulation framework is the predictive capabilities of the compact models. In order to achieve the desired functionality of an integrated circuit, it is imperative that the mathematical model formulation ensures a strong correlation between geometry scaling and model parameters to be able to correctly predict performances for an extrapolated dimension. In order to continually enhance figures of merits along the technology scaling roadmap, various scaling approaches have been adopted or envisioned including process optimization to reduce the capacitances and transit delays [31], or even a hybrid approach for silicon–germanium (SiGe) HBTs consisting doping profile optimization through TCAD simulations and predictive compact modeling through HiCuM/L2 model simulation [32]. With the same fundamental approach for III-V DHBTs, we used geometry scaling laws for HiCuM model parameters to extrapolate the major figures of merit (f_T , f_{MAX} , β and R_{TH}), without modifying the epitaxial structure or any other process features, to obtain reasonable prediction results. This requires an accurate scalable model card extracted for the geometries under test, which was further used to extrapolate the figures of merit of the current technology generation to DHBTs with the emitter dimensions of $0.13 \times 2 \mu\text{m}^2$, in order to compare them with those of the state-of-the-art InP HBT [1,33].

Figure 22 shows the scaling prediction results for these figures of merit using our scalable HiCuM model card for the current technology generation (G1). The extrapolated

f_T and f_{MAX} are compared with that of the $0.13 \times 2 \mu\text{m}^2$ state-of-the-art for a V_{CE} of 1 V. The predicted peak f_T [Figure 22a] shows that a higher value can be expected compared to the reported value for the experimental devices [33]. The new technology generation shows a similar f_T compared to the previous generation [34]. The reduction in the transit time with emitter width scaling has been observed at high current densities, which can be attributed to a pronounced collector current spreading in smaller emitter dimensions [34], leading to larger critical current and smaller transit time values. Small emitter dimension particularly poses a challenge to maintain an acceptable current gain (β), of which rather low (15–20) values have been reported for the $0.13 \mu\text{m}$ InP HBT process [1,33]. On the other hand, the prediction for the current generation shows an extrapolated current gain of 25–30 for the $0.13 \times 2 \mu\text{m}^2$ DHBT (Figure 22b). The predicted current gain is comparatively lower than the prediction of the previous generation [33], owing to the higher effective base doping in the new technology generation, which in turn lowers the base sheet resistance and results in a lower static current gain as well as a higher f_{MAX} . Subsequently, in Figure 22c, a lower peak f_{MAX} was observed (even though the new generation exhibits a slightly higher f_{MAX} compared to what had been predicted in [34]), in comparison with the values reported in [33] for the $0.13 \times 2 \mu\text{m}^2$ state of the art InP HBTs. In fact, the technologies under study have a balanced $f_T - f_{MAX}$ performance, and extrapolation to smaller geometries maintains this feature. Despite the improvement in overall f_{MAX} for the new generations, due to higher significance of peak f_{MAX} for circuit applications, further efforts are required to achieve enhanced performances, in order to attain the targeted terahertz operations. These efforts mainly require the modification of the epitaxial base, either at the epitaxial level to induce a higher quasi-electric field [33] or base emitter spacer optimization at the process level [1]. In terms of thermal performances of the DHBT technology, we obtain very similar thermal resistances compared to the preceding generation [34], as depicted in Figure 22d. Similar to our predictions for the previous technology generation, the $0.13 \times 2 \mu\text{m}^2$ HBT shows significantly elevated values of R_{TH} . Despite appearing as a crucial drawback at such scaled dimensions, we previously observed that the increase in the internal junction temperature ($\Delta T_j = R_{TH} \times V_{CE} I_C | f_{T, peak}$) at peak- f_T (Figure 22a) (plotted with solid symbols in Figure 22d, right y axis) exhibited a slightly downward trend with scaling. The prediction for the current technology generation (G1) demonstrates that there is an even stronger reduction in the internal device temperatures in the scaled version of this technology. This is due to the fact that the scaling of the DHBTs reduces the $V_{CE} I_C$ product predominantly, which in turn results in the drastic reduction in the junction temperature, even though a high thermal resistance was predicted. This is promising from the scaling point-of-view indicating an already improved thermal response has been achieved between subsequent process runs. Approaches such as transferring epitaxial structures on a substrate of higher thermal conductivity [35,36] without modifying the epitaxial structure [36], substrate thinning or even using a quaternary graded base alloy gallium–indium–arsenic–antimonite (GaInAsSb) [37] could be followed in future process runs that can further enhance the figures of merit. Guidelines from the predictive scalable compact model simulations will continue to accompany the future technology generations through further process optimization at the epitaxial level along the InP HBT scaling roadmap.

7.3. Toward a Reliability-Aware Design Framework

To emphasize the aforementioned discussions, one of the prerequisites of the monolithic integration of electronic and photonic technologies, that are capable of functioning at terahertz/sub terahertz frequencies, is a systematic assembly of existing design software that will not only take into account multi-physics transport, electro-magnetic simulation as well as interconnect modeling, but will also address emerging reliability concerns.

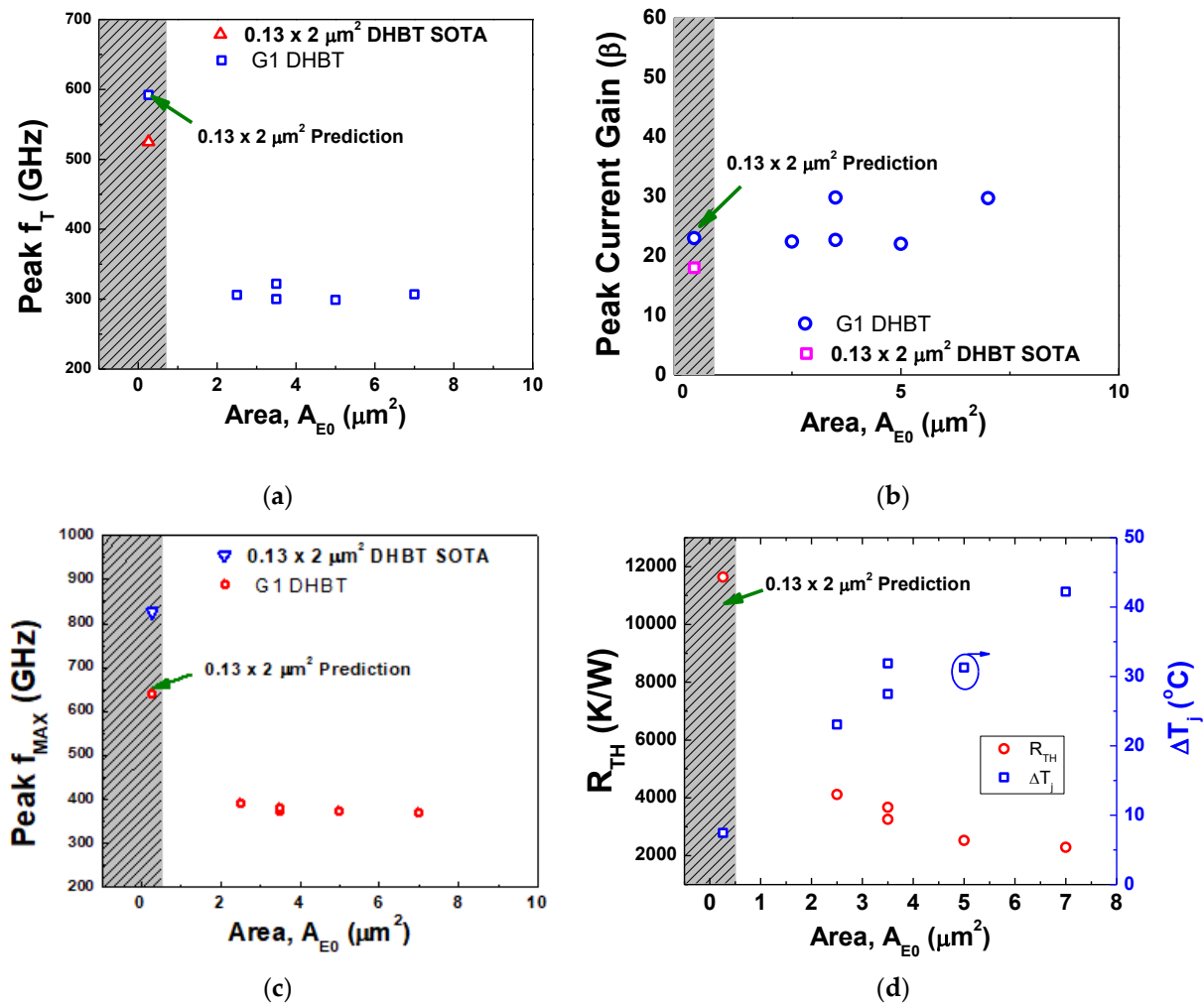


Figure 22. Extrapolating figures of merit of the III-V DHBTs: (a) f_T ; (b) β ; (c) f_{MAX} ; and (d) R_{TH} .

Optical devices, in particular photodiodes, are prone to significant heat dissipation [38], which may consequently impact the electronic part and can eventually become a serious reliability issue. Catastrophic failure (burn-out) can occur at constant power dissipations of 240 mW for the UTC-PDs [39]. On the other hand, owing to continuous scaling of electronic devices, self-heating is already a severe problem in highly scaled electronic components such as in advanced bipolar transistor technologies including SiGe or InP HBT [40]. As made evident in Section 7.2, thermal resistances (R_{TH}) of DHBTs increase rapidly as device geometries are scaled down. Self-heating management has become the major issue of further HBT process development. The first problem due to increased junction temperature is the impact on its electrical performance. The second problem is reliability related. In fact, increasing junction temperature has a negative impact on the device lifetime [21]. Most of the degradation modes of InP HBTs are strongly accelerated by temperature. Rise in device temperature will ultimately lead to pronounced self-heating at the circuit level and the failure mechanisms are likely to activate leading to degradation in the circuit performances.

To address the emerging reliability concerns in InP-based monolithic integrated circuits, [41] has proposed a reliability-aware design methodology to “pre-diagnose” failure mechanisms in advanced circuits and to design optimized “robust” circuit architectures in order to maximize circuit operation lifetime. The overall goal of this methodology is to provide a holistic reliability analysis solution for next-generation electronic system design that will meet the pre-requisite reliability-constraints prior to manufacturing. This unique methodology is achievable with already available design tools and can be applied regardless of the technology type, thus allowing a straightforward implementation into

commercial computer-aided design (CAD) flows. In terms of resources, the methodology aims to work with a single simulator-based design approach, i.e., to offer unified simulation capabilities for all parts of the integrated circuit (IC). In the context of monolithic integrated circuits, multiphysics simulation is thus in high-demand, as emphasized in Section 1. Moreover, this methodology can help drastically shorten design time and costs, while ensuring the same accuracy of results compared to conventional reliability analysis methodologies, by avoiding rigorous circuit aging tests and IC redesign phases for technology qualification. Figure 23 shows the different phases of the IC qualification process which are typically repeated several times in order to meet the qualification criteria. Apart from the obvious time constraints owing to redesign cycles, process optimization and especially mask redesigning costs tens of thousands of dollars for InP-based technologies [41]. The reliability-aware design and optimization at the circuit simulation stage thus allows to carefully choose most “robust” circuit architecture leveraging dynamic degradation laws directly implemented in the compact models compatible with all Berkeley-SPICE derivative simulators. A “virtual degradation acceleration mechanism” is pivotal for ensuring the simulation efficiency of the aging model in order to emulate years of circuit aging by picoseconds of simulation time [41]. While each phase of the reliably aware design methodology can be performed on both electronic and optical parts of the Monolithic Microwave Integrated Circuit (MMIC) until the circuit simulation stage, the reliability improvement short loop is applicable for the entire monolithic integrated circuit. The feasibility and advantages of this methodology has already been demonstrated for an InP/InGaAs DHBT process [41]. The performance of complex circuits such as a transimpedance amplifier, consisting 24 transistors based on this technology, have been analyzed over long-term aging. Design optimization to minimize the circuit failure rate has been demonstrated, making use of the reliability improvement loop. The following steps can be to demonstrate this methodology for photonic components, such as UTC photodiodes, and ultimately to leverage this methodology for the development of monolithic integrated circuits. Owing to the emerging nature of this technology, reliability-aware design will be even more important in order to ensure the desired level of maturity and demonstrate the desired technology readiness level.

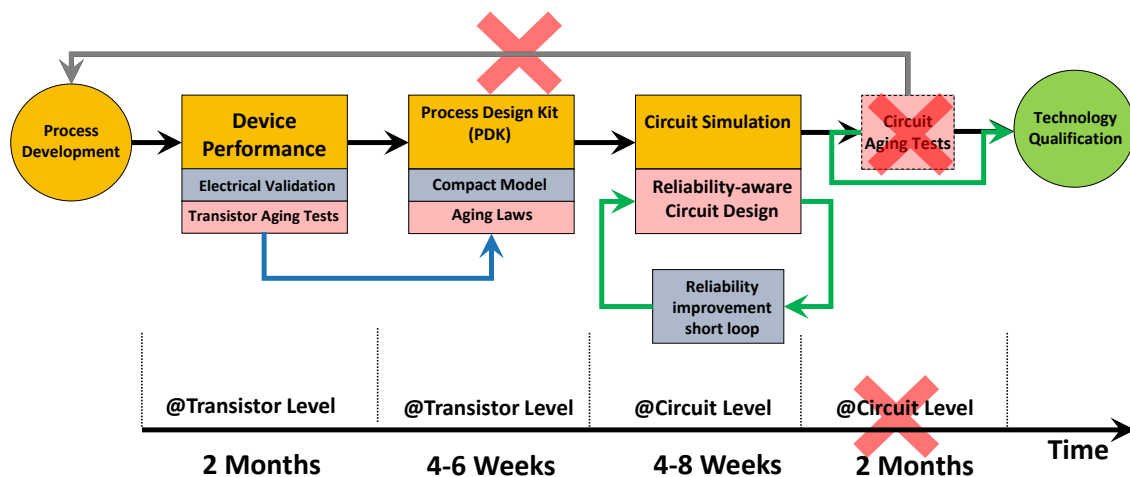


Figure 23. Methodology flow illustrating the reliability improvement loop.

8. Conclusions

In this review, we addressed several of the most important aspects of monolithic integrated circuit design for future applications in beyond-5G communication systems. For the design of such novel technology, InP-based bipolar transistors and UTC photodiodes integrated on the same substrate are viewed as the most promising solution, owing to the respective merits of these two technologies. However, aspects such as the absence of a multiphysics simulation tool, requirement for interconnect electromagnetic modeling at

high-frequency operation and tedious thermal management are some of the roadblocks for the current state-of-the-art. Most importantly, reliability and thermal management framework at the system level is a prerequisite in the electronic–photonic co-simulation infrastructure. In this paper, design methodologies and modeling approaches as well as integrated reliability analysis modules are discussed in detail in order to converge towards a multiphysics design approach equipped to tackle these emerging concerns. Extensive characterization, including DC, RF (up to 300 GHz) and optical measurements, have been realized on InP DHBTs and UTC photodiodes, based on the same InP substrate, both technologies developed at III–V Lab. Compared to our previous study [34] where the previous generation of the DHBT technology was investigated up to 40 GHz, the characterization and parameter extraction have been extended to 300 GHz for the new generation of the DHBTs. To accommodate the needs of both time and cost-effective design as well as accuracy of the simulations, computationally efficient as well as physics-based compact models have been developed. While the industry-standard HiCuM model was used to extract the parameters of this new generation of DHBT technology, the UTC-PD compact model developed in [13] has been further improved, including more accurate description of the dark and photo currents, and utilized on the UTC-PD technology from the III–V lab. From an industrial design viewpoint, the models are made compatible with existing electronic design framework. In addition, thermal management and reliability analysis modules are integrated within the models. Particularly, inferences are drawn on the similar values of thermal resistances in the two technologies, owing to their similar epitaxial composition. We have noted, however, a higher rise in junction temperature in the DHBTs compared to that of the UTC-PDs owing to their larger device geometry and consequently more efficient heat evacuation. Nevertheless, further investigations are required in order to quantify the heat dissipation and mutual thermal coupling at more severe operating conditions of the UTC-PDs, which were not addressed in this work. Furthermore, in order to study the expected performances of this technology, model projections are compared with state-of-the-art technologies and their predictive capabilities are demonstrated. Coupled TCAD–QT simulations are leveraged to better understand the underlying physics in order to improve the formulation of analytic models. Finally, an elaborate design methodology was detailed that assembles all the preceding modules under one roof, taking into account compact models, thermal management and reliability as well as failure mechanisms, in order to address the system level design of the monolithic optoelectronic integrated circuits.

Among the aspects discussed earlier, electromagnetic (EM) simulations have proven to be quite essential as the frequency of operation of the active devices fast approaches the sub-terahertz range. As illustrated in [28], as the frequency increases beyond 110 GHz, the electromagnetic coupling between the measurement probes and the substrate can have significant as well as detrimental impacts on the correct assessment of device performance. From the metrology viewpoint, the co-simulation of the characterization setup using electromagnetic and standard SPICE simulations [42] can be used to validate the accuracy of the measurements. Moreover, it can also provide insights into the decorrelation of the parasitics, stemming from the environment of the measurement setup, and the intrinsic device architecture in itself. This method has proven to be particularly essential at the (sub)millimeter wave range as the effects of the test-fixtures and passive components on the intrinsic device correctly “de-embedded” provided on-wafer calibration techniques are utilized. Moreover, along with the thermal management between electronic and photonic modules, intra-chip electromagnetic coupling can be foreseen as another factor to be accounted for in OEIC design. Thus, the SPICE-EM co-simulation can be used to further explore the performances of this key-enabling technology and can be implemented within the proposed co-design tool. Thus, this unique, single simulator-based methodology offers the groundwork for a multiphysics design environment that can be further refined along with the progress of the state-of-the-art.

Author Contributions: C.M. (Chhandak Mukherjee) mainly contributed to InP DHBT characterization, compact modeling, parameter extraction and investigations, as well as organization, writing—review and editing. M.D. mainly contributed to the InP DHBT test structures design, calibration and characterization at very high frequencies. M.D.M. contributed to the measurement support as head of the IMS characterization platform. V.N. mainly contributed to the InP DHBT conceptualization and investigation, writing—review and editing. M.R. mainly contributed to InP DHBT conceptualization, design, process development and fabrication. C.M. (Colin Mismar) mainly contributed to InP DHBT process development and fabrication. D.G. mainly contributed to UTC-PD modeling, characterization and writing review. C.C. mainly contributed to the photodiode conceptualization and investigation and writing—review and editing. H.B. mainly contributed to the photodiode process development and fabrication. N.V. mainly contributed to photodiode epitaxy. M.L. and X.W. performed the TCAD and bandstructure calculations and contributed to the writing of the manuscript. P.M. mainly contributed to supervision. C.M. (Cristell Maneux) mainly contributed to the writing—review and editing, visualization, supervision, project administration, funding acquisition. All authors have read and agreed to the published version of the manuscript.

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