Innovative Fault-Tolerant Three-Phase SPMSM Drive Without Split Capacitors, Auxiliary Legs, or TRIACs

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***Abstract*—The existing fault-tolerant three-phase AC drives need split capacitors, auxiliary legs and triode for alternating current (TRIACs) upon a standard three-phase two-level voltage source inverter (VSI) to obtain the self-healing ability towards open-phase faults (OPFs). In order to reduce the cost, volume and weight, this paper proposes a novel fault-tolerant three-phase surface-mounted permanent magnet synchronous machine (SPMSM) drive without split capacitors, auxiliary legs or TRIACs. The proposed drive is still built upon a three-phase two-level VSI, while its DC-source is directly connected to the neutral point of the motor. First, mathematical model and equivalent circuit are established to reveal the existence of an equivalent DC/DC boost converter in the drive system. Second, the brand-new *d*-0 axes current references are proposed in order to preserve the motor's performance when an OPF occurs. In this case, both i_d and i_0 are non-constant. Third, an overall control strategy including the healthy and fault-tolerant modes is presented. In the fault-tolerant mode, a deadbeat current controller is developed to track the non-constant current references. Finally, experiments are carried out on a SPMSM test-bench to verify the effectiveness of the proposed scheme.**

***Index Terms*—Permanent magnet synchronous machine, open-phase fault, fault-tolerant control, DC/DC boost converter, equivalent circuit, deadbeat current controller.**

I. Introduction

DUE to their merits of high torque and power density, high efficiency and structure simplicity, surface-mounted permanent magnet synchronous machines (SPMSMs) are preferred in various applications [1]. With the development of power electronic devices, AC drives have occupied a dominant position in industrial fields, such as air conditioning/heat pumps, wind turbines, robotics and electric vehicles (EVs) [2] [3]. Nevertheless, the failure rate of AC drives increases with the use of these devices. According to [4], open-circuit and short-circuit failures occurring in switching devices or one of motor phases are the most common faults at the power level. As the demand for high reliability drives grows, researchers and engineers have put extensive efforts into developing fault-tolerant AC drives. Although multi-phase motors, such as five-phase [5], six-phase [6] and nine-phase [7] motors, have gained special attentions during the past few years due to their inherent fault-tolerant capability, three-phase machines are still the workhorses in industrial areas owing to low cost and simple structure. This paper focuses on fault-tolerant three-phase SPMSM drives.

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For a three-phase two-level voltage source inverter (VSI) fed AC motor with Wye-connection (as shown in Fig. 1), there are four typical fault-tolerant topologies [8]–[10], as shown in Fig. 2. Thanks to the fast-acting fuses (F_j and $F_j^{'}$, $j = A, B, C$), the short-circuit fault will eventually lead to one phase being open-circuit. Therefore, the open-phase fault (OPF) is an usual fault. To be specific, if the fault occurs in inverter legs, remedial strategies can be achieved by moving the motor terminal of the faulty leg to the midpoint of split capacitors or to an auxiliary inverter leg via triode for alternating current (TRIACs) [11]. These topologies are known respectively as 3 legs with phase to capacitor midpoint (3L-PCM) and (3+1) legs with phase to an auxiliary leg ((3+1)L-PAL), as shown respectively in Fig. 2(a) and Fig. 2(b). The two topologies still allow the motor to operate with three phases under post-fault operations. As for the post-fault control strategy, the 3L-PCM should adopt the control approach of a three-phase four-switch VSI [12] while the (3+1)L-PAL can continue using the same control as that in healthy operations. In addition, both the 3L-PCM and (3+1)L-PAL are able to output the rated torque under post-fault operations. However, the motor speed in the 3L-PCM is limited to around half of the base speed because of the voltage limitation. Besides, the 3L-PCM is exposed to a risk of performance degradation caused by the oscillation of the capacitor midpoint voltage [12].

If an OPF occurs in motor windings, fault-tolerance can be achieved by connecting the motor's neutral point either to the midpoint of split capacitors or to an auxiliary inverter leg [13]–[17]. These topologies are known respectively as 3 legs with neutral point to capacitor midpoint (3L-NCM) and (3+1) legs with neutral point to an auxiliary leg ((3+1)L-NAL), as shown

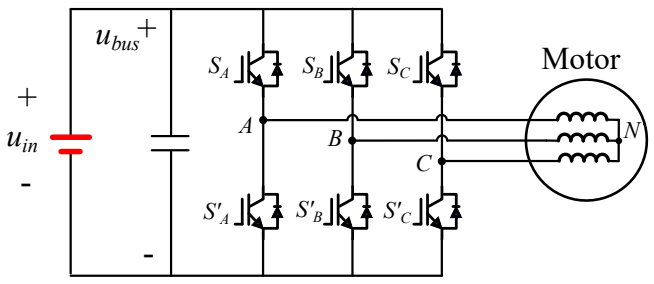

Fig. 1. VSI-fed three-phase AC motor drive.

respectively in Fig. 2(c) and Fig. 2(d). For the two topologies under post-fault operations, the motor must operate with two active phases and the control method needs to be modified appropriately. Generally speaking, the 3L-NCM and (3+1)L-NAL are more popular because they can tolerate the faulty cases appearing both in inverter and motor sides. Numerous fault-tolerant strategies based on the 3L-NCM and (3+1)L-NAL were presented in [18]–[26].

The first effective example of the 3L-NCM applied to a three-phase induction machine was presented in [18], in which a crucial conclusion indicated that it is still possible to generate the same rotating magnetic motive force by imposing a 60° phase-shift between the remaining phase-currents (the current amplitude should increase to $\sqrt{3}$ times) when an OPF occurs.

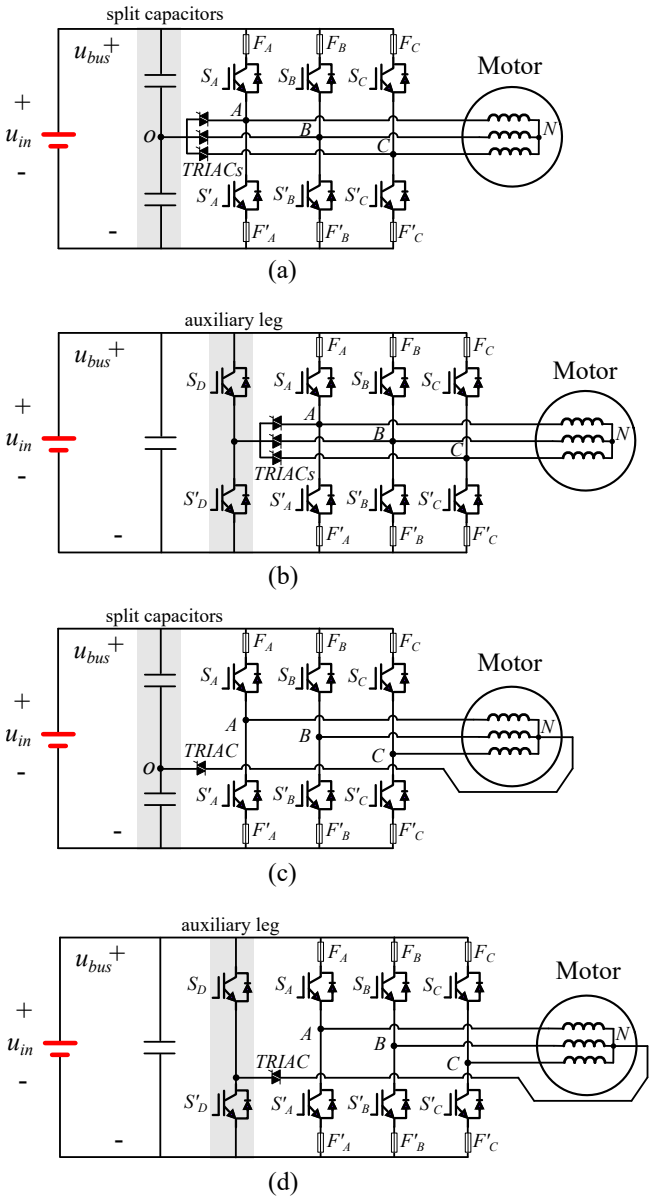

Fig. 2. Four typical fault-tolerant topologies for three-phase AC motors. (a) 3 legs with phase to capacitor midpoint (3L-PCM); (b) (3+1) legs with phase to an auxiliary leg ((3+1)L-PAL); (c) 3 legs with neutral point to capacitor midpoint (3L-NCM); (d) (3+1) legs with neutral point to an auxiliary leg ((3+1)L-NAL).

Based on this conclusion, a simple fault-tolerant implementation is to use hysteresis controllers [19]. However, hysteresis controllers suffer from the problem of inconstant switching frequency. Afterwards, [20] proposed a field-oriented control method by exploiting a suitable reference frame, in which the pulse-width modulation (PWM) with constant switching frequency can still be used. It needs to note that the 3L-NCM also gets involved in the trouble of drifting capacitor midpoint. To address this problem, a hardware-based solution by using a pair of resistors to clamp the capacitor midpoint was presented in [18].

Compared to the 3L-NCM, the (3+1)L-NAL can avoid the problem of drifting capacitor midpoint due to an auxiliary leg provided to the motor's neutral point. The reformulating current references (60° phase-shift) for the remaining phases are consistent with that in the 3L-NCM. Therefore, hysteresis controller based fault-tolerant control is also applicable to the (3+1)L-NAL. [21] and [22] proposed a voltage feed-forward compensation method whose effectiveness was verified on a PMSM. Moreover, an unified voltage feed-forward compensation method by injecting suitable zero-sequence voltages was developed in [23], which is general and applicable both in the 3L-NCM and (3+1)L-NAL. Nevertheless, voltage feed-forward compensation method is sensitive to motor's parameters so that it is unfavorable in some high-precision applications. Recently, [24] [25] proposed a new fault-tolerant control method for the (3+1)L-NAL, in which the neutral current is proactively controlled due to an additional control degree of freedom provided by the auxiliary leg. Meanwhile, a novel reference frame was introduced, in which the neutral current reference remains constant so that a classic proportional-integral (PI) regulator is sufficient to track the reference.

A detailed comparison of all these existing fault-tolerant topologies was presented in [26]. In a word, compared to the standard three-phase two-level VSI, the existing fault-tolerant topologies need redundant components (split capacitors or auxiliary legs) to obtain the remedial ability when an OPF occurs. These redundant components definitely increase the cost, volume and weight of the drive system. Besides, the circuit structure changes by triggering TRIACs. This actually increases the complexity and reduces the reliability of the whole system.

In order to achieve the objectives of lower cost and simpler structure, this paper aims to propose a novel fault-tolerant three-phase SPMSM drive without using split capacitors, auxiliary legs or TRIACs. The rest of this paper is organized as follows: In Section II, a brief description of the proposed drive is presented. Then, mathematical model and equivalent circuit are established. In order to maintain the torque performance when an OPF occurs, the novel fault-tolerant scheme is proposed in Section III. In this case, the d-0 axes current references are non-constant. An overall control strategy including the healthy and the fault-tolerant modes is presented in Section IV, in which a deadbeat current controller is developed to track the post-fault current references. Experiments and assessments are presented in Section V. Finally, conclusions are given in Section VI.

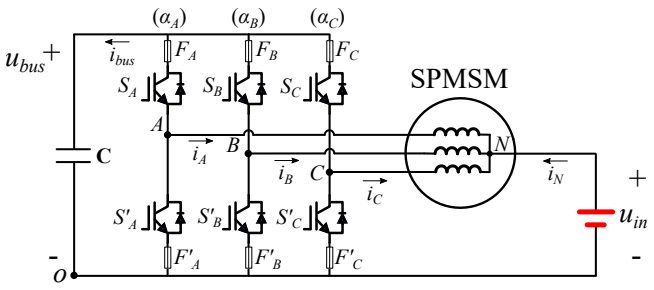

Fig. 3. Proposed fault-tolerant three-phase SPMSM drive.

II. Topology Description and Modeling under The Healthy Operation

The proposed fault-tolerant SPMSM drive is built upon a three-phase two-level VSI, in which the DC-source u_{in} is directly connected to the neutral point 'N', as shown in Fig. 3. The fast-acting fuses (F_j and $F_j^{'}$, $j = A, B, C$) are used to isolate the faulty phase when short-circuit failures appear. However, neither redundant components (split capacitors and auxiliary legs) nor TRIACs are employed. u_{bus} is the DC-bus voltage; **C** is the DC-bus capacitor; S_j and $S_j^{'}$ ($j = A, B, C$) are the PWM signals of switching devices; i_A, i_B and i_C are the phase-currents; i_N is the neutral current; i_{bus} is the DC-bus current.

A. Average Model

In order to study the characteristics of the proposed drive, the average model under the healthy operation will be established in this subsection.

In one PWM period (T_s), the average value of a variable $x(t)$ is defined as

$$\overline{x}(t) = \frac{1}{T_s}\int_{t-T_s}^{t} x(\tau)d\tau \tag{1}$$

Therefore, the average voltage equations of the drive system can be formulated by

$$\begin{bmatrix}\overline{u}_{AO}\\ \overline{u}_{BO}\\ \overline{u}_{CO}\end{bmatrix} = \begin{bmatrix}\alpha_A\\ \alpha_B\\ \alpha_C\end{bmatrix}\overline{u}_{bus} = \begin{bmatrix}\overline{u}_{AN}\\ \overline{u}_{BN}\\ \overline{u}_{CN}\end{bmatrix} + \begin{bmatrix}\overline{u}_{in}\\ \overline{u}_{in}\\ \overline{u}_{in}\end{bmatrix} \tag{2}$$

where $\overline{u}_{AO}$, $\overline{u}_{BO}$ and $\overline{u}_{CO}$ are the terminal voltages of the inverter; $\overline{u}_{AN}$, $\overline{u}_{BN}$ and $\overline{u}_{CN}$ are the motor's phase-voltages; α_A, α_B and α_C are respectively the duty-cycles of S_A, S_B and S_C.

The phase-voltages of the SPMSM can be formulated by

$$\begin{cases}\overline{u}_{AN} = R\bar{i}_A + L_{AA}\dfrac{d\bar{i}_A}{dt} + M_{AB}\dfrac{d\bar{i}_B}{dt} + M_{AC}\dfrac{d\bar{i}_C}{dt} + \overline{e}_A\\ \overline{u}_{BN} = R\bar{i}_B + L_{BB}\dfrac{d\bar{i}_B}{dt} + M_{BA}\dfrac{d\bar{i}_A}{dt} + M_{BC}\dfrac{d\bar{i}_C}{dt} + \overline{e}_B\\ \overline{u}_{CN} = R\bar{i}_C + L_{CC}\dfrac{d\bar{i}_C}{dt} + M_{CA}\dfrac{d\bar{i}_A}{dt} + M_{CB}\dfrac{d\bar{i}_B}{dt} + \overline{e}_C\end{cases} \tag{3}$$

with

$$\begin{cases}\overline{e}_A = -\overline{\omega}_e\psi_f sin(\overline{\theta}_e)\\ \overline{e}_B = -\overline{\omega}_e\psi_f sin(\overline{\theta}_e - 2\pi/3)\\ \overline{e}_C = -\overline{\omega}_e\psi_f sin(\overline{\theta}_e + 2\pi/3)\end{cases} \tag{4}$$

$$\begin{cases}L_{AA} = L_\sigma + L_\Sigma + L_\Delta\cos 2\overline{\theta}_e\\ L_{BB} = L_\sigma + L_\Sigma + L_\Delta\cos 2\left(\overline{\theta}_e - 2\pi/3\right)\\ L_{CC} = L_\sigma + L_\Sigma + L_\Delta\cos 2\left(\overline{\theta}_e + 2\pi/3\right)\\ M_{AB} = M_{BA} = -L_\Sigma/2 + L_\Delta\cos 2\left(\overline{\theta}_e + 2\pi/3\right)\\ M_{BC} = M_{CB} = -L_\Sigma/2 + L_\Delta\cos 2\overline{\theta}_e\\ M_{AC} = M_{CA} = -L_\Sigma/2 + L_\Delta\cos 2\left(\overline{\theta}_e - 2\pi/3\right)\\ L_\Sigma = \left(L_d + L_q - 2L_\sigma\right)/3\\ L_\Delta = \left(L_d - L_q\right)/3\\ L_\sigma = L_0\end{cases} \tag{5}$$

where R is the phase resistance; L_{AA}, L_{BB} and L_{CC} are the self-inductances; M_{AB}, M_{BA}, M_{AC}, M_{CA}, M_{BC} and M_{CB} are the mutual inductances; e_A, e_B and e_C are the back-EMFs; L_d, L_q and L_0 are respectively the d-axis, q-axis and zero-sequence inductances; L_σ, L_Σ and L_Δ are respectively the leakage inductance, average inductance and inductance fluctuation (for a SPMSM, $L_\Delta = 0$); ψ_f is the permanent magnet flux linkage; $\overline{\theta}_e$ is the electrical position; $\overline{\omega}_e$ is the electrical speed.

The average current equations can be expressed by

$$\bar{i}_{bus} = C\frac{d\overline{u}_{bus}}{dt} = -\begin{bmatrix}\alpha_A\\ \alpha_B\\ \alpha_C\end{bmatrix}^T\begin{bmatrix}\bar{i}_A\\ \bar{i}_B\\ \bar{i}_C\end{bmatrix} \tag{6}$$

$$\bar{i}_A + \bar{i}_B + \bar{i}_C + \bar{i}_N = 0 \tag{7}$$

By using the Park transformation, (2) can be transformed from A-B-C to d-q-0 coordinate systems, as

$$\begin{bmatrix}\overline{u}_{dO}\\ \overline{u}_{qO}\\ \overline{u}_{0O}\end{bmatrix} = \begin{bmatrix}\alpha_d\\ \alpha_q\\ \alpha_0\end{bmatrix}\overline{u}_{bus} = \begin{bmatrix}\overline{u}_d\\ \overline{u}_q\\ \overline{u}_0\end{bmatrix} + \begin{bmatrix}0\\ 0\\ \overline{u}_{in}\end{bmatrix} \tag{8}$$

where $\overline{u}_{dO}$, $\overline{u}_{qO}$ and $\overline{u}_{0O}$ represent the inverter's terminal voltages in d-q-0 coordinate system; α_d, α_q and α_0 are the values of α_A, α_B and α_C converted into d-q-0 coordinate system; $\overline{u}_d$, $\overline{u}_q$ and $\overline{u}_0$ are the motor's voltages in d-q-0 coordinate system.

In d-q-0 coordinate system, the voltage equations of the SPMSM can be reformulated by

$$\begin{bmatrix}\overline{u}_d\\ \overline{u}_q\\ \overline{u}_0\end{bmatrix} = \begin{bmatrix}R & 0 & 0\\ 0 & R & 0\\ 0 & 0 & R\end{bmatrix}\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\\ \bar{i}_0\end{bmatrix} + \begin{bmatrix}L_d & 0 & 0\\ 0 & L_q & 0\\ 0 & 0 & L_0\end{bmatrix}\frac{d}{dt}\begin{bmatrix}\bar{i}_d\\ \bar{i}_q\\ \bar{i}_0\end{bmatrix} + \overline{\omega}_e\begin{bmatrix}-L_q\bar{i}_q\\ L_d\bar{i}_d + \psi_f\\ 0\end{bmatrix} \tag{9}$$

where $\bar{i}_d$, $\bar{i}_q$ and $\bar{i}_0$ are the currents in d-q-0 coordinate system.

By substituting the zero-sequence term of (9) into (8), we obtain

$$\alpha_0\overline{u}_{bus} = \overline{u}_0 + \overline{u}_{in} = R\bar{i}_0 + L_0\frac{d\bar{i}_0}{dt} + \overline{u}_{in} \tag{10}$$

According to the Park transformation, i_0 and α_0 can be expressed by

$$\bar{i}_0 = \frac{(\bar{i}_A + \bar{i}_B + \bar{i}_C)}{3} = -\frac{\bar{i}_N}{3} \tag{11}$$

$$\alpha_0 = \frac{\alpha_A + \alpha_B + \alpha_C}{3} \tag{12}$$

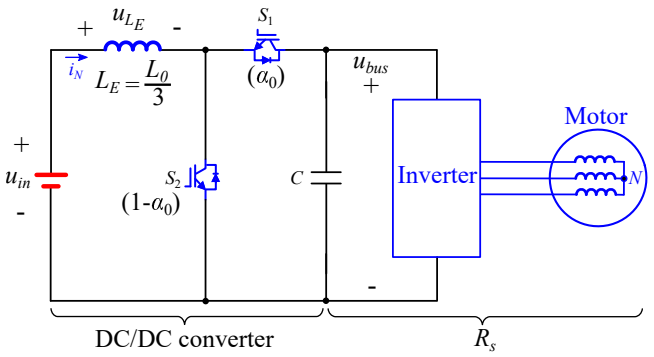

Fig. 4. Equivalent circuit of the proposed drive under the healthy operation.

By substituting (11) into (10), we obtain

$$\overline{u}_{in} - \alpha_0 \overline{u}_{bus} = -\overline{u}_0 = \underbrace{\frac{R}{3}\bar{i}_N + \frac{L_0}{3}\frac{d\bar{i}_N}{dt}}_{\overline{u}_{L_E}} \tag{13}$$

According to (13), the motor can be seen as an equivalent inductor (L_E) whose resistance and inductance are respectively $R/3$ and $L_0/3$ (by looking from the input u_{in} to the output u_{bus}). For convenience, the voltage of L_E is defined as $\overline{u}_{L_E}$. Because the duty-cycles (α_A, α_B and α_C) are strictly bounded between 0 and 1, α_0 is limited between 0 and 1. Therefore, it is interesting to find that the zero-sequence equation of the drive corresponds to a DC/DC boost converter, where $L_0/3$ functions as the filter inductor and (1-α_0) represents the duty-cycle of the boost's chopper. By assuming the positive circuit (without any zero-sequence component) of the drive as an equivalent load (R_s), the proposed drive is equivalent to a DC/DC boost converter followed by a conventional SPMSM drive system (the neutral point is disconnected), as shown in Fig. 4. It needs to note that all the zero-sequence components are embodied in the equivalent boost converter. S_1 and S_2 are two virtual switches for visualizing the zero-sequence duty-cycle α_0. In steady-states, the DC-bus voltage approximates to

$$\overline{u}_{bus} \approx \frac{\overline{u}_{in}}{\alpha_0} \tag{14}$$

In addition, (13) also indicates that the DC-bus voltage is only related to these zero-sequence components ($\overline{u}_0$, $\bar{i}_0$, L_0 and α_0). Meanwhile, according to (9), the motor performance is determined by the components located in d-q plane. This means that the motor and the equivalent DC/DC boost converter are uncoupled in d-q-0 coordinate system. Consequently, it is possible to separate the controls of the motor and the equivalent boost converter.

B. Power Balance Analysis

Because the power of the proposed drive is provided by the DC-source, it is obvious that $\bar{i}_N$ or $\bar{i}_0$ is nonzero.

The input power ($\overline{p}_{in}$) of the drive can be calculated by

$$\overline{p}_{in} = \overline{u}_{in}\bar{i}_N = -3\overline{u}_{in}\bar{i}_0 \tag{15}$$

The torque of the SPMSM is formulated by

$$\overline{T}_e = \frac{3}{2}p\psi_f \bar{i}_q \tag{16}$$

where p is the number of pole-pairs.

Thus, the output power ($\overline{p}_{out}$) of the motor can be formulated approximately as

$$\overline{p}_{out} = \frac{2\pi \overline{T}_e \overline{n}}{60} = \frac{\pi p \psi_f \bar{i}_q \overline{n}}{20} \tag{17}$$

where $\overline{n}$ (rpm) is the rotor speed.

According to energy conservation law, we obtain

$$\underbrace{\int_{t_1}^{t_2} \overline{p}_{in} dt}_{E_{in}} = \underbrace{\int_{t_1}^{t_2} \frac{\overline{p}_{out}}{\eta} dt}_{E_{out}} + \underbrace{\frac{C}{2}\overline{u}_{bus2}^2 - \frac{C}{2}\overline{u}_{bus1}^2}_{E_C} \tag{18}$$

where t_1 and t_2 represent two operating moments; η is the system efficiency; E_{in} is the input energy; E_{out} is the output energy (including system losses); $\overline{u}_{bus1}$ and $\overline{u}_{bus2}$ are respectively the DC-bus voltages at t_1 and t_2; E_C means the energy absorbed by the DC-bus capacitor from t_1 to t_2.

In steady-states, $\overline{u}_{bus}$ is constant thereby E_C is null. In this case, the power balance equation can be derived as

$$\overline{p}_{in} = \frac{\overline{p}_{out}}{\eta} \tag{19}$$

In order to quantify the proportion of the zero-sequence current, a new variable γ is defined. By combining (15), (17) and (19), γ can be formulated by

$$\gamma = \left|\frac{\bar{i}_0}{\bar{i}_q}\right| = \frac{\pi p \psi_f \overline{n}}{60 \overline{u}_{in} \eta} \tag{20}$$

The parameters of the SPMSM drive used in this paper are shown in Table. I. Because the rated DC-bus voltage is 30 V, a 15 V DC-source is sufficient due to the equivalent DC/DC boost function. Under this situation, the trend of γ with respect to $\overline{n}$ and η is illustrated in Fig. 5. The value range of $\overline{n}$ is considered as $(0, 4000)$ rpm and the value range of η is chosen as $(0.6, 1)$. It can be seen that γ increases with the rise of speed and the fall of efficiency. To be specific, γ varies between 0.31 and 0.52 under the nominal speed. Within the nominal operating area, γ is less than 0.52. By using the inverse Park transformation, the representations of phase-currents under the healthy operation can be expressed by

$$\begin{cases} \bar{i}_A = \bar{i}_d cos(\overline{\theta}_e) - \bar{i}_q sin(\overline{\theta}_e) - \gamma \bar{i}_q \\ \bar{i}_B = \bar{i}_d cos(\overline{\theta}_e - 2\pi/3) - \bar{i}_q sin(\overline{\theta}_e - 2\pi/3) - \gamma \bar{i}_q \\ \bar{i}_C = \bar{i}_d cos(\overline{\theta}_e + 2\pi/3) - \bar{i}_q sin(\overline{\theta}_e + 2\pi/3) - \gamma \bar{i}_q \end{cases} \tag{21}$$

Apparently, it can be seen that a DC component ($-\gamma \bar{i}_q$) is superposed to the fundamental current of each phase.

III. Fault-Tolerant Scheme

For the state of art presented in Fig. 2, TRIACs and split capacitors (or an auxiliary leg) are necessary to provide a path to the zero-sequence current when an OPF occurs. Thanks to the original connection of motor's neutral point, the proposed drive does not need any additional component to construct the path.

When the drive system encounters an OPF, it has only two available phases left. In order to preserve motor's performance,

TABLE I
THE PARAMETERS OF THE SPMSM DRIVE

Parameter	Value	Unit
Stator winging resistance R	0.5	Ω
Number of pole pairs p	4	-
d,q-axis inductance L_d, L_q	1.1	mH
Zero-sequence inductance L_0	0.8	mH
Permanent magnet flux linkage ψ_f	0.0056	Wb
Rated speed	4000	rpm
Rated torque	125	mN·m
Rated power P_n	52.5	W
DC-bus capacitor C	940	uF
Switching frequency f_s	20	kHz
Rated DC-bus voltage	30	V

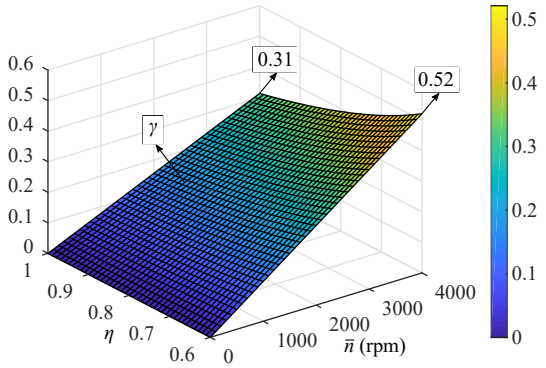

Fig. 5. Trend of γ with respect to $\overline{n}$ and η.

the current references of remaining phases must be reformulated. For convenience, an OPF occurring in phase A is taken into account throughout.

When the OPF occurs, $\bar{i}_A = 0$. By considering this and using the Clark transformation, we obtain

$$\bar{i}_\alpha = -\bar{i}_0 \tag{22}$$

According to the rotation transformation, $\bar{i}_d$ and $\bar{i}_q$ can be reformulated by

$$\begin{cases} \bar{i}_d = \bar{i}_\alpha cos\bar{\theta}_e + \bar{i}_\beta sin\bar{\theta}_e \\ \bar{i}_q = -\bar{i}_\alpha sin\bar{\theta}_e + \bar{i}_\beta cos\bar{\theta}_e \end{cases} \tag{23}$$

where $\bar{i}_\alpha$ and $\bar{i}_\beta$ are the currents in α-β plane.

By substituting (22) into (23), $\bar{i}_d$ and $\bar{i}_q$ become

$$\begin{cases} \bar{i}_d = -\bar{i}_0 cos\bar{\theta}_e + \bar{i}_\beta sin\bar{\theta}_e \\ \bar{i}_q = \bar{i}_0 sin\bar{\theta}_e + \bar{i}_\beta cos\bar{\theta}_e \end{cases} \tag{24}$$

By eliminating $\bar{i}_\beta$, $\bar{i}_0$ is expressed as

$$\bar{i}_0 = \bar{i}_q sin\bar{\theta}_e - \bar{i}_d cos\bar{\theta}_e \tag{25}$$

In order to preserve the torque, $\bar{i}_q$ must remain unchanged before and after the OPF. Defining the d-q axes currents respectively as $\bar{i}_{dh}$ and $\bar{i}_{qh}$ before the OPF, $\bar{i}_0$ under the post-fault operation should follow

$$\bar{i}_0 = \bar{i}_{qh} sin\bar{\theta}_e - \bar{i}_{dh} cos\bar{\theta}_e \tag{26}$$

Most of fault-tolerant strategies in the 3L-NCM and (3+1)L-NAL are on the basis of (26). In this case, $\bar{i}_0$ is a periodic function. Its period is consistent with the fundamental period ($T_f = 2\pi/\overline{\omega}_e$) and its mean is 0.

In regard to the proposed drive, if $\bar{i}_0$ is chosen as (26), the input power ($\overline{p}_{in}$) will be periodic. In one T_f, the mean of $\overline{p}_{in}$ can be calculated by

$$\begin{aligned} &< \overline{p}_{in} >_{T_f} = \frac{1}{T_f}\int_0^{T_f} \overline{p}_{in} dt \\ &= \frac{\overline{\omega}_e}{2\pi}\int_0^{\frac{2\pi}{\overline{\omega}_e}} -3\overline{u}_{in}\left[\bar{i}_{qh} sin(\overline{\omega}_e t) - \bar{i}_{dh} cos(\overline{\omega}_e t)\right] dt \\ &= 0 \end{aligned} \tag{27}$$

This indicates that the average input power will be null. In this case, it is impossible to provide a constant output power to the motor. Therefore, the typical representation (26) is infeasible in the proposed drive.

With the considerations of a non-constant d-axis current and a non-null average input power, we propose a novel d-axis current reference ($\bar{i}_d^*$), as

$$\bar{i}_d^* = -2\bar{i}_{0h} cos\bar{\theta}_e \tag{28}$$

where $\bar{i}_{0h}$ is the zero-sequence current before the OPF.

By substituting $i_q^* = i_{qh}$ and (28) into (25), the new $\bar{i}_0^*$ can be calculated by

$$\bar{i}_0^* = \bar{i}_{qh} sin\bar{\theta}_e + \bar{i}_{0h}\left[1 + cos(2\bar{\theta}_e)\right] \tag{29}$$

With $\bar{i}_0^*$, the average input power is

$$\begin{aligned} &< \overline{p}_{in} >_{T_f} = \frac{1}{T_f}\int_0^{T_f} \overline{p}_{in} dt \\ &= \frac{\overline{\omega}_e}{2\pi}\int_0^{\frac{2\pi}{\overline{\omega}_e}} -3\overline{u}_{in}\left[\bar{i}_{qh} sin(\overline{\omega}_e t) + \bar{i}_{0h}\left[1 + cos(2\overline{\omega}_e t)\right]\right] dt \\ &= -3\overline{u}_{in}\bar{i}_{0h} = \overline{u}_{in}\bar{i}_{Nh} \end{aligned} \tag{30}$$

where $\bar{i}_{Nh}$ is the neutral current before the OPF.

Obviously, (30) demonstrates that the same average input power can be held in one T_f. I.e. the proposed $\bar{i}_d^*$ and $\bar{i}_0^*$ make it possible to provide the required power to the motor for maintaining invariable torque and speed (output power). However, it should be noted that, the instantaneous input power is non-constant because of the non-constant $\bar{i}_0^*$. Therefore, according to (18), the DC-bus capacitor has to absorb or release some instantaneous energy in one T_f.

Based on the new $\bar{i}_d^*$ and $\bar{i}_0^*$, the theoretical phase-currents under the post-fault operation can be expressed by

$$\begin{cases} \bar{i}_A = 0 \\ \bar{i}_B = 2\gamma\bar{i}_{qh} cos\bar{\theta}_e cos(\bar{\theta}_e - 2\pi/3) \\ \quad - \bar{i}_{qh} sin(\bar{\theta}_e - 2\pi/3) + \bar{i}_{qh} sin\bar{\theta}_e - \gamma\bar{i}_{qh}\left[1 + cos(2\bar{\theta}_e)\right] \\ \bar{i}_C = 2\gamma\bar{i}_{qh} cos\bar{\theta}_e cos(\bar{\theta}_e + 2\pi/3) \\ \quad - \bar{i}_{qh} sin(\bar{\theta}_e + 2\pi/3) + \bar{i}_{qh} sin\bar{\theta}_e - \gamma\bar{i}_{qh}\left[1 + cos(2\bar{\theta}_e)\right] \end{cases} \tag{31}$$

Theoretical current waveforms are visualized in Fig. 6 where $\gamma = 0.25$ is considered as an example. It can be seen that $\bar{i}_{dh}$ is 0 for SPMSMs; $\bar{i}_d$ is a cosine function of $\bar{\theta}_e$; $\bar{i}_q$ remains $\bar{i}_{qh}$ for maintaining the desired torque; The shape of

TABLE II
d-q-0 AXES CURRENT REFERENCES UNDER POST-FAULT OPERATIONS

Fault location	$\bar{i}_d^*$	$\bar{i}_q^*$	$\bar{i}_0^*$
Phase A	$-2\bar{i}_{0h}cos\bar{\theta}_e$	$\bar{i}_{qh}$	$\bar{i}_{qh}sin\bar{\theta}_e + \bar{i}_{0h}\left[1+cos(2\bar{\theta}_e)\right]$
Phase B	$-2\bar{i}_{0h}cos(\bar{\theta}_e - \frac{2\pi}{3})$	$\bar{i}_{qh}$	$\bar{i}_{qh}sin(\bar{\theta}_e - \frac{2\pi}{3}) + \bar{i}_{0h}\left[1+cos[2(\bar{\theta}_e - \frac{2\pi}{3})]\right]$
Phase C	$-2\bar{i}_{0h}cos(\bar{\theta}_e + \frac{2\pi}{3})$	$\bar{i}_{qh}$	$\bar{i}_{qh}sin(\bar{\theta}_e + \frac{2\pi}{3}) + \bar{i}_{0h}\left[1+cos[2(\bar{\theta}_e + \frac{2\pi}{3})]\right]$

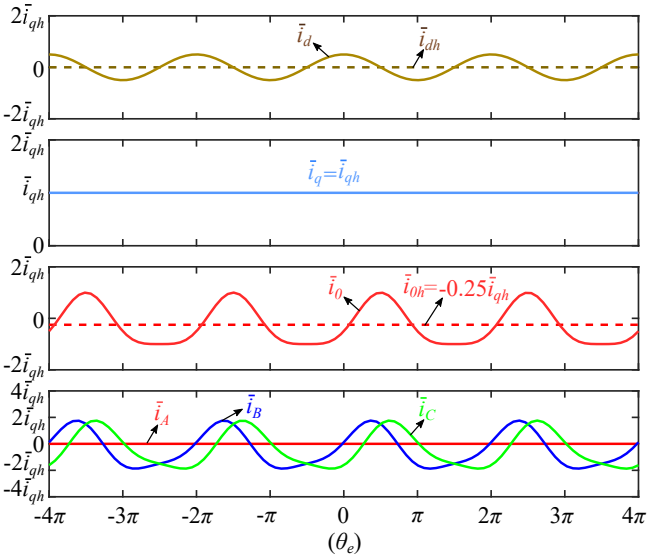

Fig. 6. Theoretical current waveforms of the proposed drive under the post-fault operation (an OPF occurs in phase A).

$\bar{i}_0$ is non-sinusoidal and the mean of $\bar{i}_0$ is equal to $\bar{i}_{0h}$; $\bar{i}_A$ is 0 because of the fault; $\bar{i}_B$ and $\bar{i}_C$ are no longer the standard sinusoidal waves with a 60° phase-shift.

Regarding the faulty cases appearing in phase B and C, the post-fault $\bar{i}_d^*$, $\bar{i}_q^*$ and $\bar{i}_0^*$ can be derived in the same way. For clarity, all the representations are summarized in Table. II.

IV. OVERALL CONTROL STRATEGY

In order to control the motor as well as the DC-bus voltage, an overall control strategy is proposed for the drive system, as shown in Fig. 7. It is divided into the healthy and the fault-tolerant modes. The speed controller, Park transformation and PWM block are consistent both in the healthy and fault-tolerant modes.

A. Healthy Mode

In the healthy mode, the conventional vector control (VC) framework is still employed. It consists of one speed-loop PI controller and two current-loop PI controllers followed by decoupling compensations. n^* is the target speed. The speed-loop PI outputs the q-axis current reference (i_q^*). d-axis current reference (i_d^*) is normally set as 0 for SPMSMs. d-axis current-loop PI outputs d-axis voltage reference (u_d^*) and q-axis current-loop PI outputs q-axis voltage reference (u_q^*).

In addition to speed and d-q axes currents, the zero-sequence current and DC-bus voltage also need to be regulated. As shown in Fig. 7, an additional PI controller is used to control the zero-sequence current. Meanwhile, another PI controller is employed to control the DC-bus voltage. The detailed design of the two PI controllers are presented in the following.

Considering that L_0 is rarely used in most of conventional drives, Fig. 8 depicts the measuring method of L_0. As shown in Fig. 8(a), three phases of the motor are connected in parallel. A voltage pulse (1 V) is applied between the neutral point and the terminals. By implementing a voltage-step test, the step response of neutral currents is obtained, as shown in Fig. 8(b). Accordingly, L_0 can be calculated as

$$L_0 = 3 \cdot \frac{R}{3}\Delta t_{\_0.632} = \frac{3 \cdot 1(\mathrm{V})}{5.9(\mathrm{A})} \cdot 1.7(\mathrm{ms}) = 0.8(\mathrm{mH}) \quad (32)$$

where $i_{N\_0.632}$ means the value of i_N reaching 0.632 times the stable value 5.9 (A); $\Delta t_{0.632}$ is the time spent when i_N increases from 0 to $i_{N\_0.632}$.

According to the zero-sequence model presented in (9), its transfer function (a first-order inertia element) is expressed by

$$H0(s) = \frac{i_0(s)}{u_0(s)} = \frac{1}{R + L_0 s} \quad (33)$$

The transfer function of a PI controller is defined as

$$PI(s) = \frac{K_p \cdot (T_i \cdot s + 1)}{T_i \cdot s} = K_p + K_i \cdot \frac{1}{s} \quad (34)$$

where K_p is the proportional gain; T_i is the integral time; $K_i = \dfrac{K_p}{T_i}$ is the integral gain.

By choosing $T_i = \dfrac{L_0}{R} = 0.0016$, the closed-loop transfer function of the zero-sequence current-loop can be expressed by

$$H1(s) = \frac{1}{1 + \dfrac{R \cdot T_i}{K_p} \cdot s} \quad (35)$$

Apparently, $H1$ is also a first-order inertia element. By designing the time constant (T_0) of $H1$ as 0.01 s, K_p can be calculated by

$$K_p = \frac{R \cdot T_i}{T_0} = 0.08 \quad (36)$$

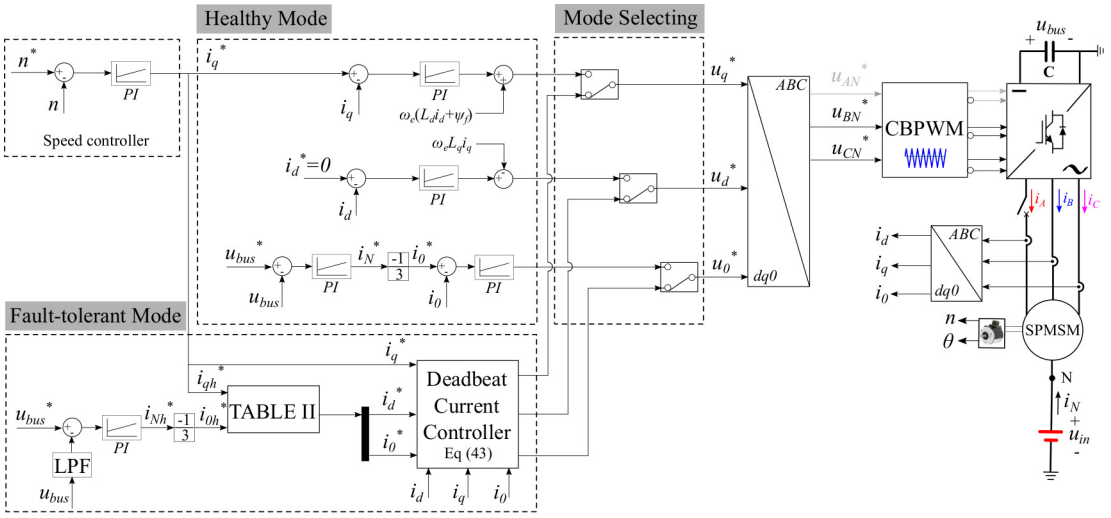

Fig. 7. Overall control strategy of the proposed drive.

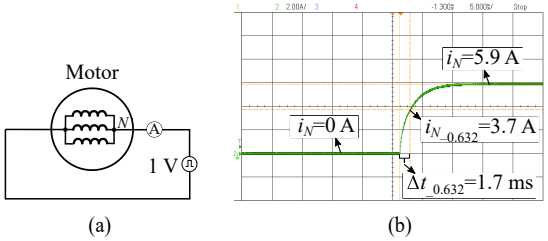

Fig. 8. Measurement of the zero-sequence inductance L_0. (a) Circuit diagram of the measurement. (b) Step response of i_N.

For the DC-bus voltage-loop, its PI parameters can be designed according to the small-signal model of the equivalent boost converter, as

$$\begin{bmatrix} \dot{\tilde{i}}_N \\ \dot{\tilde{u}}_{bus} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-\alpha_{0s}}{L_0/3} \\ \dfrac{\alpha_{0s}}{C} & \dfrac{-1}{R_s C} \end{bmatrix} \begin{bmatrix} \tilde{i}_N \\ \tilde{u}_{bus} \end{bmatrix} + \begin{bmatrix} \dfrac{u^*_{bus}}{L_0/3} \\ \dfrac{-i_{Ns}}{C} \end{bmatrix} (1-\tilde{\alpha_0}) \tag{37}$$

where i_{Ns}, α_{0s} are the equilibrium states of the equivalent boost converter.

Under rated condition, the equivalent load R_s of the equivalent boost converter can be calculated approximately by

$$R_s \approx \frac{u^{*2}_{bus}}{P_n} = \frac{30^2}{52.5} = 17\,\Omega \tag{38}$$

where u^*_{bus} is the DC-bus voltage reference.

Due to the equivalent boost function, a 15 V DC-source is sufficient for the drive [27]–[30]. Thus, i_{Ns}, α_{0s} can be calculated by

$$\begin{cases} \alpha_{0s} = \dfrac{u_{in}}{u^*_{bus}} = 0.5 \\ i_{Ns} = \dfrac{u^{*2}_{bus}}{u_{in} R_s} = 3.5\,(\mathrm{A}) \end{cases} \tag{39}$$

Consequently, the transfer function of the DC-bus voltage-loop is derived as

$$H2(s) = \frac{\tilde{u_{bus}}(s)}{\tilde{i_N}(s)} = \frac{\dfrac{-i_{Ns}}{C}s + \dfrac{\alpha_{0s}}{(L_0/3)C}u^*_{bus}}{\dfrac{u^*_{bus}}{L_0/3}s + \dfrac{u^*_{bus}}{R_s(L_0/3)C} + \dfrac{\alpha_{0s}}{(L_0/3)C}i_{Ns}} \tag{40}$$

For this plant, the proportional gain and integral gain of its PI controller are tuned as 19.9 and 0.003. After the tuning, the open-loop bode diagram is shown in Fig. 9. The gain margin (G.M.) is 80.5 dB and the phase margin (P.M.) is 60 degree. The corresponding step response is shown in Fig. 10. It can be seen that the setting time is less than 0.1 s.

Therefore, the DC-bus voltage-loop PI outputs the neutral current reference i^*_N. i^*_0 can be obtained according to the proportional relation in (11). The zero-sequence current-loop PI outputs the zero-sequence voltage reference u^*_0. By using the inverse Park transformation, phase-voltage references (u^*_{AN}, u^*_{BN} and u^*_{CN}) are obtained. By applying the carrier-based PWM (CBPWM), the control signals are generated.

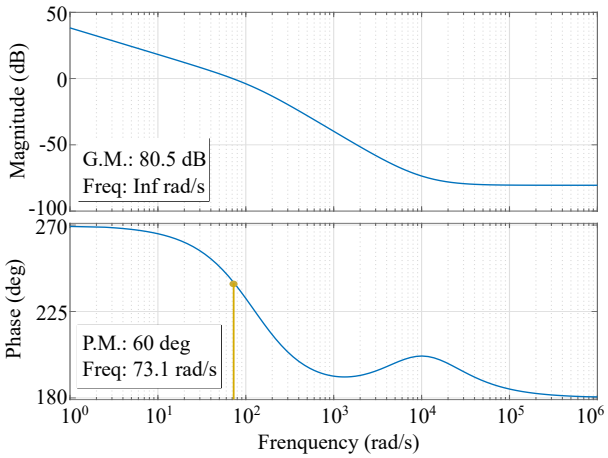

Fig. 9. Open-loop bode diagram of the DC-bus voltage-loop after the tuning.

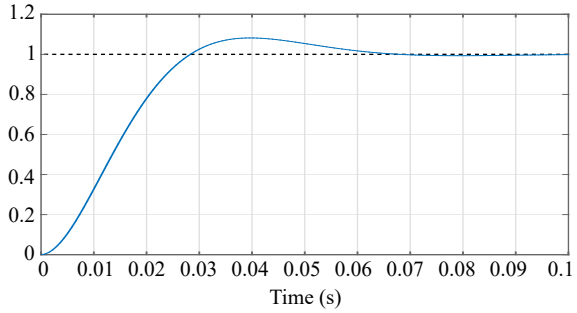

Fig. 10. Step response of the DC-bus voltage-loop after the tuning.

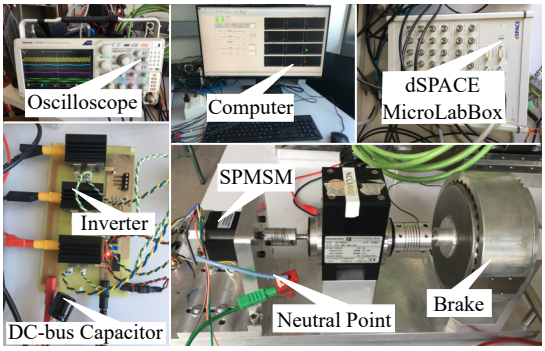

Fig. 11. Test-bench.

B. Fault-Tolerant Mode

The d-0 axes current references in the fault-tolerant mode are non-constant. It is well known that deadbeat controller has the advantages of high bandwidth, fast response and optimum tracking ability [31] [32]. Therefore, a deadbeat current controller is developed to track the changeful trajectories.

By applying Euler forward approximation to the SPMSM model, the d-q-0 currents at the $(k+1)^{th}$ moment can be expressed by

$$\begin{bmatrix} \bar{i}_d(k+1) \\ \bar{i}_q(k+1) \\ \bar{i}_0(k+1) \end{bmatrix} = \underbrace{\begin{bmatrix} 1-\frac{RT_s}{L_d} & \frac{\bar{\omega}_e(k)L_qT_s}{L_d} & 0 \\ -\frac{\bar{\omega}_e(k)L_dT_s}{L_q} & 1-\frac{RT_s}{L_q} & 0 \\ 0 & 0 & 1-\frac{RT_s}{L_0} \end{bmatrix}}_{\boldsymbol{A}} \begin{bmatrix} \bar{i}_d(k) \\ \bar{i}_q(k) \\ \bar{i}_0(k) \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{T_s}{L_d} & 0 & 0 \\ 0 & \frac{T_s}{L_q} & 0 \\ 0 & 0 & \frac{T_s}{L_0} \end{bmatrix}}_{\boldsymbol{B}} \begin{bmatrix} \bar{u}_d(k) \\ \bar{u}_q(k) \\ \bar{u}_0(k) \end{bmatrix} + \underbrace{\begin{bmatrix} 0 \\ -\frac{\bar{\omega}_e(k)\psi_f T_s}{L_q} \\ 0 \end{bmatrix}}_{\boldsymbol{C}} \tag{41}$$

where $\boldsymbol{A}$, $\boldsymbol{B}$ and $\boldsymbol{C}$ are the matrices of the discrete equation.

In order to eliminate current errors at the $(k+1)^{th}$ sampling interval, the d-q-0 currents at the $(k+1)^{th}$ moment should follow

$$\begin{cases} \bar{i}_d(k+1) = \bar{i}_d^* \\ \bar{i}_q(k+1) = \bar{i}_q^* \\ \bar{i}_0(k+1) = \bar{i}_0^* \end{cases} \tag{42}$$

By replacing (42) into (41), the required d-q-0 voltages at the k^{th} moment are

$$\begin{bmatrix} \bar{u}_d(k) \\ \bar{u}_q(k) \\ \bar{u}_0(k) \end{bmatrix} = \boldsymbol{B}^{-1} \left(\begin{bmatrix} \bar{i}_d^* \\ \bar{i}_q^* \\ \bar{i}_0^* \end{bmatrix} - \boldsymbol{A} \begin{bmatrix} \bar{i}_d(k) \\ \bar{i}_q(k) \\ \bar{i}_0(k) \end{bmatrix} - \boldsymbol{C} \right) \tag{43}$$

In addition, as analyzed in Section III, the DC-bus capacitor has to absorb and release some instantaneous energy under the post-fault operation. That is to say the DC-bus voltage will oscillate with the frequency of the neutral current. Therefore, a low pass filter (LPF) is employed to obtain the mean of u_{bus}. The cut-off frequency of the LPF is lower than the fundamental frequency. The DC-bus voltage PI controller is still used to obtain i_{Nh}^* and i_{0h}^*. i_{qh}^* is still obtained by the speed-loop PI. Then, the post-fault current references are calculated according to these formulas presented in Table. II. With the proposed deadbeat current controller (43), u_d^*, u_q^* and u_0^* are obtained. Finally, by using the inverse Park transformation and CBPWM, the control signals of the remaining two phases are generated.

V. Experimental Results

Experimental validations are carried out on the SPMSM whose parameters are consistent with Table. I, to verify the effectiveness of the proposed scheme and its overall control strategy. Thanks to the equivalent boost function, a 15 V DC-source is supplied to the proposed drive. The algorithms are implemented on a dSPACE MicroLabBox platform. The test-bench is shown in Fig. 11. The OPF is simulated by a circuit breaker connected in series with phase A.

A. Healthy Operation

Fig. 12 depicts the experimental results of the proposed drive operating under the healthy condition with speed and load step tests. The experimental settings are as follows: n^* is 1000 rpm before 1 s. It is increased to 2000 rpm at 1 s while it is reset to 1000 rpm after 5 s. A 100 mN·m load is imposed at 10 s and removed at 15 s. In Fig. 12, it can be seen that the rotor speed can track the reference well during the acceleration and deceleration processes. Facing with load disturbances, it shows about 50 rpm fluctuations but turns to stable state rapidly. In the whole experiment, the ripple of electromagnetic torque is around 11 mN·m. The DC-bus voltage reaches 30 V even if a 15 V DC-source is supplied. This demonstrates the existence of an equivalent boost function in the drive system. u_{bus} shows around 0.5 V voltage dip and rise during the speed step tests, but it recovers to 30 V quickly. In addition, it can be seen that i_N increases from 0 to 3.8 A when the system has an acceleration request. Then, it decreases to -0.6 A when the motor decelerates sharply. This is because the motor operates as a generator in this case. Under the condition of 1000 rpm and 100 mN·m, the mean of i_N is around 1.8 A and the the ripple of u_{bus} is around 0.4 V. Consequently, this experiment verifies the effectiveness of the proposed overall control strategy, in which the motor and the DC-bus voltage can be regulated simultaneously.

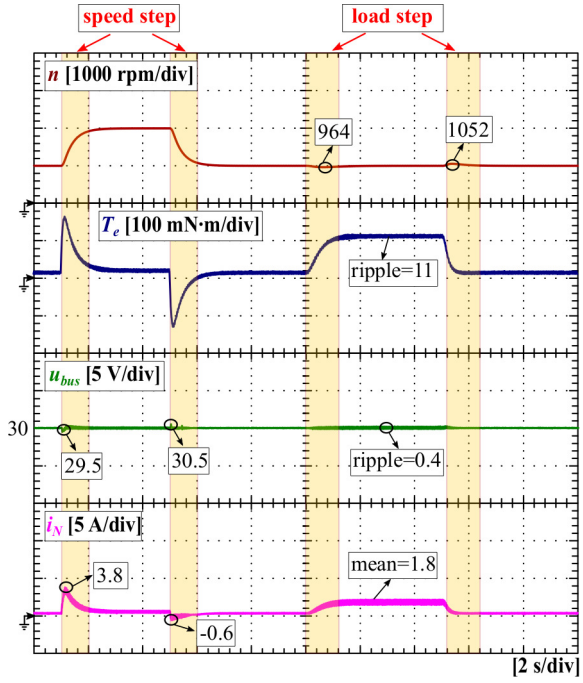

Fig. 12. Experimental results of the proposed drive operating under the healthy condition with a 15 V DC-source.

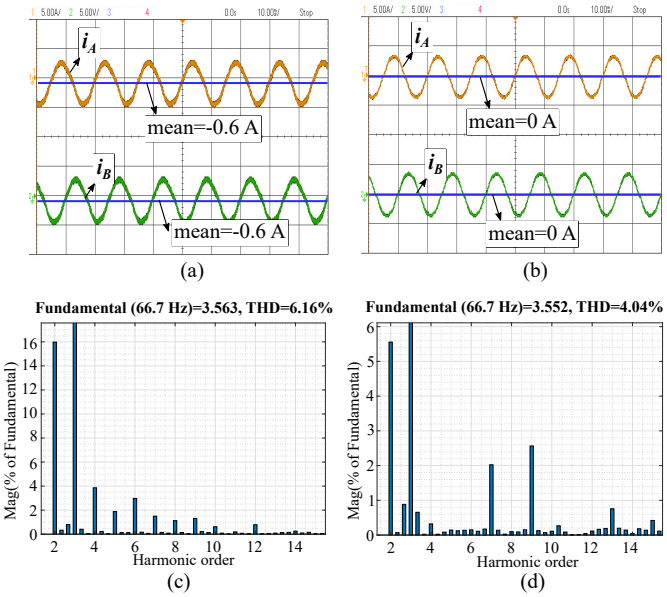

Fig. 14. Phase-current comparisons between the proposed and the conventional drives under the healthy operation (1000 rpm and 100 mN·m). (a) i_A and i_B of the proposed drive. (b) i_A and i_B of the conventional drive. (c) FFT analysis of the phase-currents in the proposed drive. (d) FFT analysis of the phase-currents in the conventional drive.

In order to clarify the advantages and disadvantages of the proposed drive, a contrast experiment is carried out on the same motor but fed by the conventional topology (the neutral point is unused but the parameters of VC are consistent). For the conventional drive, a 30 V DC-source is required. Relevant experimental results are shown in Fig. 13. By comparison, it can be seen that the motor performance (including the speed control and torque performance) is similar between the two drives. Therefore, it can be concluded that the motor performance can be maintained when its neutral point is connected to a DC-source.

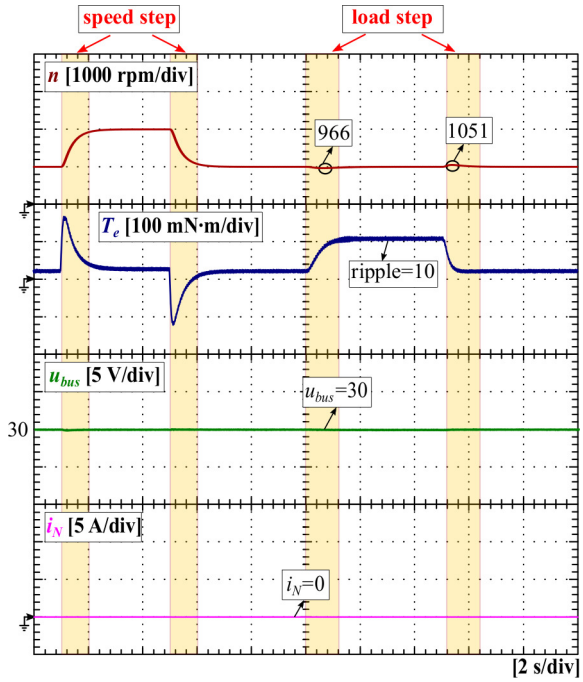

Fig. 13. Experimental results of the conventional drive (neutral point is unused) operating under the healthy condition with a 30 V DC-source.

Fig. 14(a) and Fig. 14(b) illustrate the detailed phase-currents of the two drives under the healthy operation (1000 rpm and 100 mN·m). First, it can be seen that the mean of phase-currents in the proposed drive is around -0.6 A. This means that a 0.6 A zero-sequence current flows into the motor. In terms of the conventional drive, the mean of its phase-currents is 0 A. Second, it is visible that the current ripple is larger in the proposed drive. In order to quantify the total harmonic distortion (THD), fast fourier transform (FFT) analyses are shown respectively in Fig. 14(c) and Fig. 14(d). According to the FFT results, it can be concluded that the current THD in the proposed drive increases by 2.12% compared to that in the conventional drive. This is a drawback to the proposed drive in order to win over a free boost function.

B. Post-Fault Operation

Fig. 15 shows the fault-tolerant test of the proposed drive operating under 2000 rpm without load condition. First, under the healthy operation, n is stable at 2000 rpm. The ripple of T_e is about 10 mN·m. u_{bus} is boosted at 30 V. i_{dh} is 0 A and i_{qh} is 0.58 A. i_{0h} and i_{Nh} are respectively -0.15 A and 0.45 A. Thus, it can be calculated that the zero-sequence current proportion γ is around 0.26. Second, when the OPF occurs, i_A becomes 0 A instantly. Without the fault-tolerant control strategy, T_e and i_q show big fluctuations with 50 mN·m and 1.6 A, respectively. The ripple of u_{bus} increases to 2 V as well. The ripples of i_d, i_0 and i_N are respectively 1.4, 0.4 and 1.2 A. Third, once the fault-tolerant mode switches on,

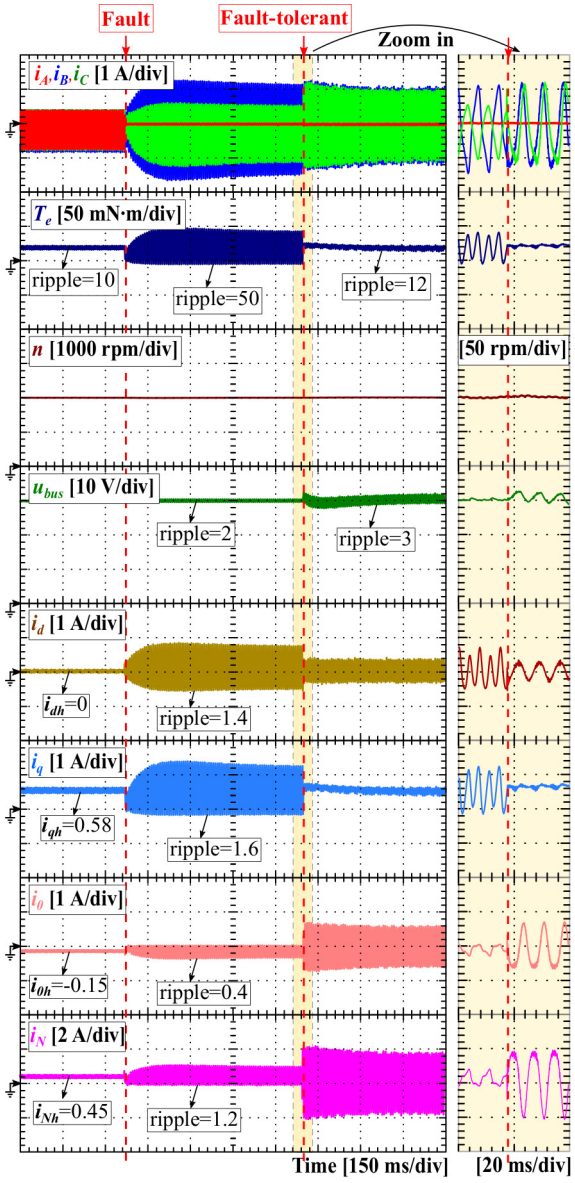

Fig. 15. Experimental results of the fault-tolerant test under 2000 rpm without load condition.

the performance of T_e and i_q is preserved rapidly. The ripple of T_e decreases to 12 mN·m, which is in the range of the values obtained under the healthy operation. For greater detail, enlarged views are displayed to the right of each graph. It can be seen that i_d is a cosine curve, which is in line with the theoretical waveform presented in Fig. 6. Similarly, i_0 is also similar to the theoretical curve. The period of i_d and i_0 is the same as that of i_B and i_C, which is the fundamental period (T_f = 7.5 ms). As analyzed in Section III, for maintaining the constant output power, the DC-bus capacitor has to absorb and release some transient energy. Therefore, it can be seen that u_{bus} is synchronized with i_N and the ripple of u_{bus} increases to 3 V. However, it needs to be emphasized that the mean of u_{bus} is still around 30 V.

For verifying the tracking performance of the proposed deadbeat current controller, Fig. 16 illustrates the detailed comparison between the theoretical and actual phase-current

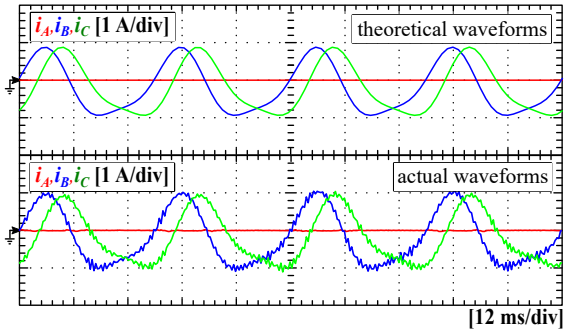

Fig. 16. Detailed comparison between the theoretical and actual phase-currents under the fault-tolerant operation (2000 rpm without load).

waveforms. It can be seen that the actual i_B and i_C show good agreement with the theoretical results. As analyzed before, they are no longer the standard sinusoidal waves with a 60° phase-shift.

In order to check the fault-tolerant performance when the motor operates under load condition, Fig. 17 depicts relevant experimental results. First, under the healthy operation, n is controlled at 2000 rpm steadily. T_e is about 60 mN·m, which is almost half of the nominal torque. The torque ripple is around 9 mN·m. u_{bus} is still boosted at 30 V stably. i_{dh} is 0 A and i_{qh} is about 1.79 A. i_{0h} is -0.46 A and i_{Nh} is 1.37 A. Second, when the OPF occurs, the ripple of T_e increases to 150 mN·m dramatically. Meanwhile, the ripple of i_q arises to 4.2 A. The ripples of i_d, i_0 and i_N are respectively 4, 1.0 and 2.5 A. Third, thanks to the fault-tolerant controller, T_e returns to 60 mN·m quickly with oscillations of around 13 mN·m. In the enlarged views, i_d is still a cosinoidal waveform as analyzed. Moreover, the period of i_d and i_0 is still consistent with the fundamental period. With the increase of motor's power, the peak value of i_N increases to 5.6 A while it is about 1.8 A under the no-load condition. This means the transient energy absorbed or released by the DC-bus capacitor also increases. As a result, it can be seen that the ripple of u_{bus} increases to 6 V. However, the mean of u_{bus} is still about 30 V due to the DC-bus voltage controller. The detailed comparison between the theoretical and actual phase-current is illustrated in Fig. 18. It can be seen that the actual i_B and i_C are still consistent with the theoretical waveforms.

When the motor operates at the fault-tolerant mode, it still has dynamic requirements, such as speed regulation and load change. Thus, in order to further validate the practicability, dynamic tests under the post-fault operation are implemented, as shown in Fig. 19. The setup of this experiment is as follows: n^* is 1000 rpm before 2 s. It is set to 1500 rpm between 2 and 5 s while it is reset to 1000 rpm after 5 s. A 50 mN·m load is imposed at 10 s and removed at 15 s. According to the experimental results, it can be seen that i_A is always 0 A because of the OPF. The motor speed can still track the referenced signal well. The torque performance is still maintained during the acceleration, deceleration, loading and deloading processes. When the motor accelerates instantly, u_{bus} declines to 22 V firstly. Thanks to the control for the mean of u_{bus}, i_{0h}^* decreases from -0.07 to -0.37 A (i.e. i_{Nh}^*

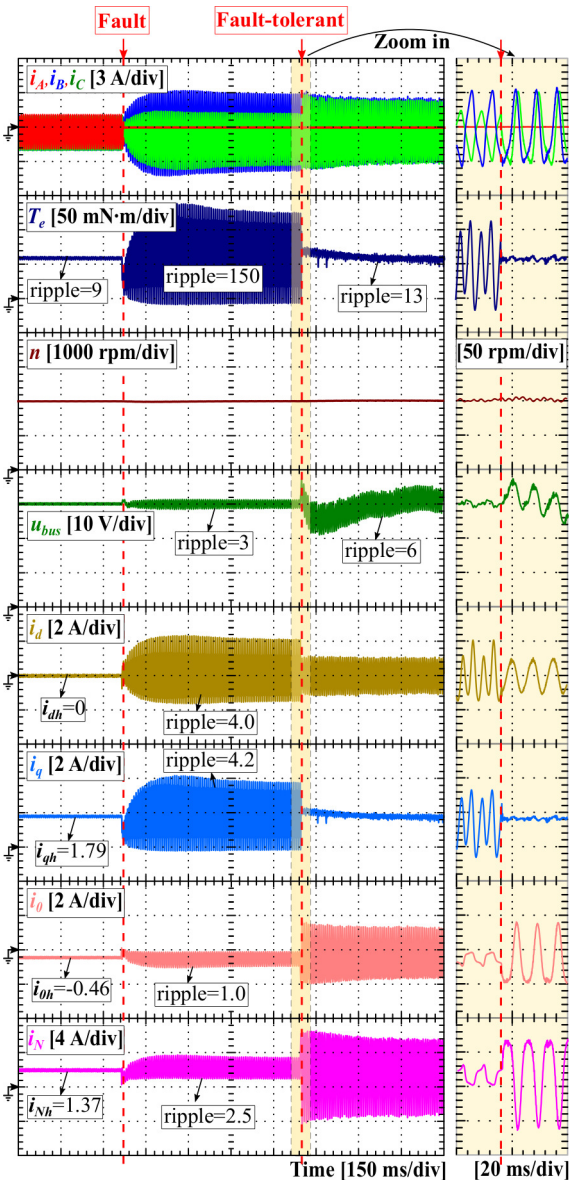

Fig. 17. Experimental results of the fault-tolerant test under 2000 rpm with load condition.

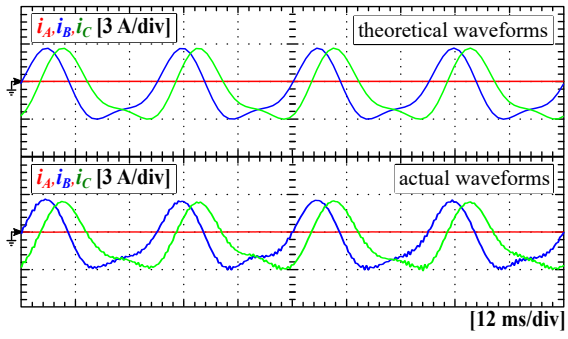

Fig. 18. Detailed comparison between the theoretical and actual phase-current waveforms under the fault-tolerant operation (2000 rpm with load).

increases from 0.21 to 1.11 A) rapidly in order to provide more power to the drive system. Therefore, the mean of u_{bus} can return to 30 V. Similarly, i^*_{0h} can also adjust cleverly during

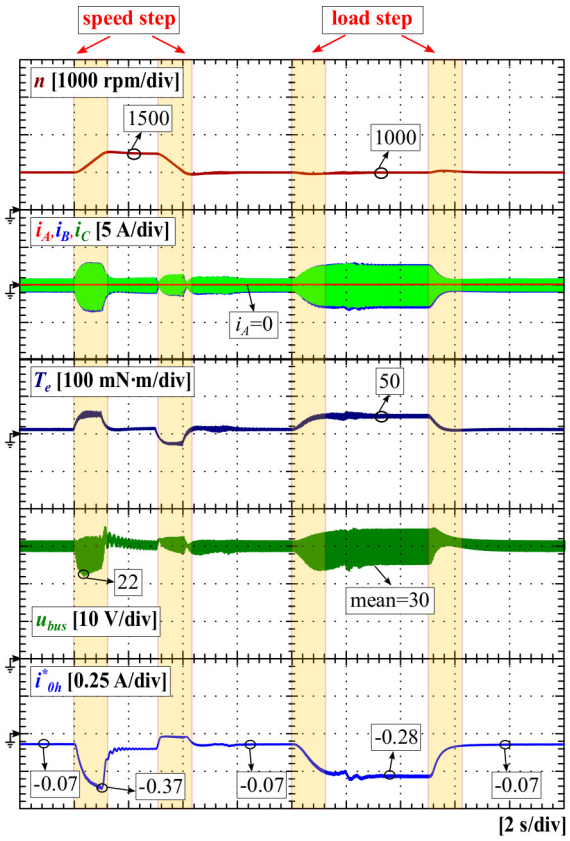

Fig. 19. Experimental results of the proposed drive under the post-fault operation with dynamic tests.

TABLE III
CHARACTERISTICS OF THE PROPOSED FAULT-TOLERANT THREE-PHASE SPMSM DRIVE WITH COMPARISON TO THE EXISTING TOPOLOGIES

Topology	Split capacitors	Auxiliary leg	TRIAC	Boost function
Proposed drive	NO	NO	0	YES
3L-PCM	YES	NO	3	NO
(3+1)L-PAL	NO	YES	3	NO
3L-NCM	YES	NO	1	NO
(3+1)L-NAL	NO	YES	1	NO

the load change processes. It changes from -0.07 to -0.28 A then returns to -0.07 A again. This demonstrates that it is feasible to obtain suitable i^*_{0h} by using a controller to regulate the mean of u_{bus}.

Consequently, according to the theoretical analyses and experimental validations, the characteristics of the proposed fault-tolerant three-phase SPMSM drive compared to the existing topologies are summarized in Table. III.

VI. CONCLUSION

In this paper, an innovative fault-tolerant three-phase SPMSM drive and its overall control strategy were proposed. First, the proposed drive is able to reach a higher DC-bus voltage thanks to the equivalent DC/DC boost converter function. However, the rise (2.12%) of current THD even the issue of iron core saturation caused by the zero-sequence current should be noticed in practical applications. In order

to control the DC-bus voltage, a new control-loop is added into the conventional VC framework by considering the zero-sequence components. Second, the proposed drive has the self-healing ability towards OPFs neither using split capacitors nor adding auxiliary inverter legs. Moreover, it needs no TRIAC to reconfigure the circuit structure. In order to maintain the motor performance under the post-fault operation, a cosinoidal d-axis current reference and a nonsinusoidal zero-sequence current reference were proposed. For tracking the non-constant references, a deadbeat current controller was developed. The convincing experimental results verified the effectiveness of the innovative drive and its control strategy. In the healthy operation, the DC-bus voltage can be boosted to twice the DC-source voltage. In the fault-tolerant operation, the torque performance can recover rapidly once the fault-tolerant control strategy works.

Consequently, the proposed drive has the advantages of low cost, volume, weight and structure simplicity compared to these existing fault-tolerant three-phase topologies. The study of this paper enriches the categories of fault-tolerant three-phase drives. From the view of application, the proposed solution seems to have significant value in EVs because a free DC/DC boost converter function and an economical fault-tolerant solution can be provided simultaneously by one three-phase two-level VSI.

VII. Appendix

The Clark transformation is

$$\boldsymbol{T_c} = \frac{2}{3}\begin{bmatrix} 1 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{A.1}$$

The rotation transformation from α-β-0 to d-q-0 coordinates is

$$\boldsymbol{T_r} = \begin{bmatrix} cos(\theta_e) & sin(\theta_e) & 0 \\ -sin(\theta_e) & cos(\theta_e) & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{A.2}$$

The Park transformation is

$$\boldsymbol{T_p} = \frac{2}{3}\begin{bmatrix} cos(\theta_e) & cos(\theta_e - \frac{2\pi}{3}) & cos(\theta_e + \frac{2\pi}{3}) \\ -sin(\theta_e) & -sin(\theta_e - \frac{2\pi}{3}) & -sin(\theta_e + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{A.3}$$

The inverse Park transformation is

$$\boldsymbol{T_p^{-1}} = \begin{bmatrix} cos(\theta_e) & -sin(\theta_e) & 1 \\ cos(\theta_e - \frac{2\pi}{3}) & -sin(\theta_e - \frac{2\pi}{3}) & 1 \\ cos(\theta_e + \frac{2\pi}{3}) & -sin(\theta_e + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{A.4}$$

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