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Design of a 1.5 GHz Low jitter DCO Ring in 28 nm CMOS Process

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Abstract—The immunity of jitter with respect to supply voltage is one of the desirable characteristics of digitally controlled oscillators (DCO) for clocking applications. This paper presents a design of such an oscillator with a high frequency resolution and small area in 28 nm technology. In order to reduce the dependence of the oscillator frequency on its voltage supply, differential amplifiers are used as inverters (delay cells) and a bias circuit with a stable voltage output is employed to bias the oscillator. From post-layout simulations, this DCO achieves a dynamic range from 1.13 to 1.54 GHz with the use of differential delay cells, the variation of the output frequency is less than 4.5% over all the frequency range, for VDD variation of 10%. The frequency control has 9.2 bits, giving an average frequency step of 722 kHz. This DCO achieves a phase noise of -74 dBc/Hz@1MHz or an jitter equivalence of 2.3 ps. The maximal power consumption of this DCO at maximum frequency is 840 μ W, which is a low figure comparing to the state-of-the-art implementation with typical power of sub-milliwatts for the similar frequency range.

Index Terms—All-Digital Phase Locked Loop (ADPLL), Digitally controlled oscillator (DCO), differential inverter ring

I. INTRODUCTION

As the functionality of electronic circuits and systems-on-chip (SoCs) expands, generation and distribution of clock signals becomes more and more challenging [1]. Over recent years, there has been a need of reliable clock generation systems for a wide range of applications in telecommunications [2], distributed computation and ultra-low phase noise frequency generation [3]. As a consequence, frequency generator must be of high purity while being easily controllable by digital interfaces, consume low power and occupy a minimum possible area. All-Digital Phase-Locked Loops (ADPLLs) architectures respond to such requirement. They can easily be integrated into digital environment since they only use digital blocks and they are compatible with the design flow of digital integrated circuits [4].

Digital phase synthesis techniques require a digitally controlled oscillator (DCO). The controlled oscillator can be realized through an LC-tank [5] or a inverters ring circuit [6]. An ADPLL with an LC-tank based oscillator is proven to be able to generate low phase noise signals, while an ADPLL with an inverted ring based oscillator offers a wider tuning range with lower power consumption on a smaller chip area. Low area and power consumption requirements are particularly important in solution when an array of oscillators is used (beam forming applications, distributed all-digital PLLs, etc. [7], [8]). For such applications it is desirable to avoid use of LC tanks

which are area-hungry, and to prefer ring based oscillator architecture.

The aim of this study is to propose a design of an inductorless low jitter ring DCO in 28 nm CMOS technology with a relatively narrow frequency tuning range, but suitable for Very-Large-Scale Integration (VLSI) applications, such as clock generation/distribution networks. We target the frequency range of 25% around 1.5 GHz with a frequency step of ≈ 1 MHz. The paper is organized as follows. In Section II, the specifications and the design of the oscillator are discussed. Then the results of post layout simulations are presented and analyzed in Section III.

II. DIGITALLY CONTROLLED OSCILLATOR DESIGN

A. Digitally Controlled Oscillator Architecture

In this section, the architecture of the proposed 5-stage ring DCO is discussed. The implemented architecture is shown in Fig 1. The oscillator uses five differential amplifiers as delay cells, and the output frequency is controlled by the load capacitance of each amplifier. One of the major issues in DCO design is the dependence of the output frequency on power supply variations and the pollution of the supply network by the transition of heavily loaded oscillator cells. In order to minimize these negative factors, the use of delay cells based on differential current logic is preferred.

The intrinsic jitter of a differential ring oscillator increases with the number of stages [9], so the latter is set to a relatively low value of five. Such a number of stages allows one to equally distribute the tuning circuits among the stages while keeping an acceptable aspect ratio of the whole layout.

The frequency control is achieved by reconfigurable capacitive tanks, connected in parallel to the outputs of the stages. The sum of all capacitors connected to the oscillator nodes, controlled by the digital input code, is linearly related to the generated frequency. Hence, the frequency control is achieved by a DAC (Digital to Analog Converter) implementing a function "Code \rightarrow Capacitance".

For controlled oscillators used in the PLLs, the monotonicity of the transfer function is of primary importance, otherwise the PLL may experience unstable behavior in the zones where the characteristic slope sign is reverse with regard to the nominal one. The worst situation for the monotonicity of the DAC characteristic is when the conversion is achieved by cells having weight proportional to the powers of 2 (a binary encoding). Yet such an implementation is the most simple for

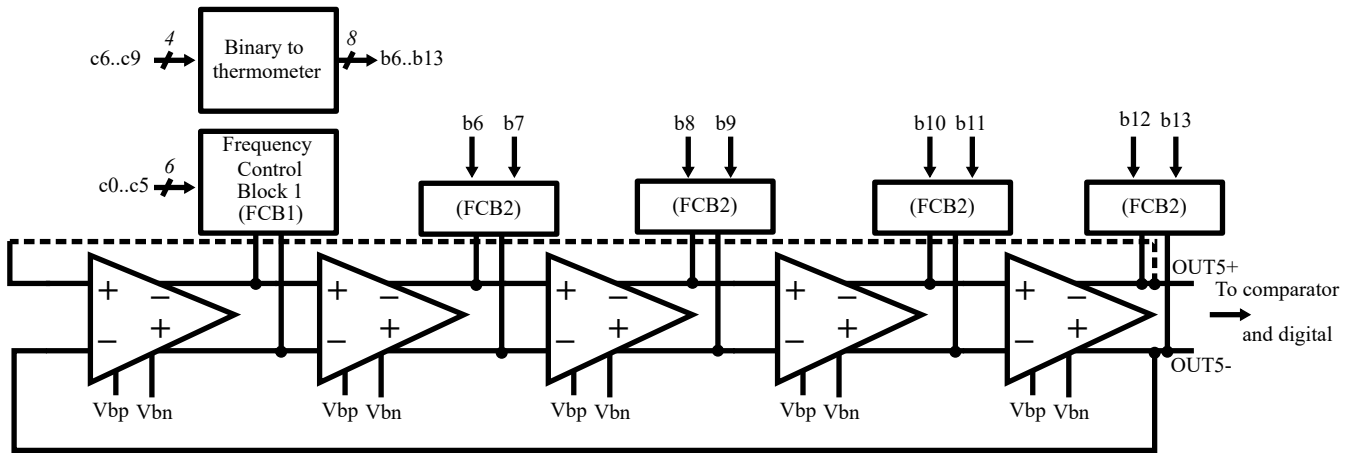


Fig. 1. High level block diagram of the proposed 5-stage ring (delay cell) DCO.

the control and from the point of view of the area saving (for N bits, only N tuning cells is necessary). On the contrary, the best monotonicity is achieved by a thermometer coding, but at a price of high coding complexity and a higher area (2^N tuning cells is necessary).

A compromise is often to combine these two coding scheme, by using the thermometer coding for highest significant bits (a coarse tuning), and a binary coding for the lowest significant bits (a fine tuning). In this implementation two kinds of Frequency Control Blocks (FCBs) are used. FCB1, used to generate the least significant bits of the control (fine control) word is controlled by a binary code, and FCB2 implementing the most significant bits (coarse control) is controlled by a thermometer code. In order to equally distribute the capacitance among all the stages of the ring oscillator, the block FCB1 (64 LSB steps) is put on the first stage, and 4 blocks FCB2 (8 steps of 64 LSB width) are connected to the remaining stages. With the equal FCB2 split across all the amplifiers, this architecture gives us a control frequency resolution of $8 \cdot 64 + 64 = 576$ codes steps or 9.2 bits.

B. Differential Amplifier and Bias Circuit

The frequency of the DCO is determined by the delay of an individual current-mode inverters, which have the same architecture as a differential amplifier, but having a quasilinear load. Its full schematic is shown in fig.2. A linear load allows one to keep the current source transistor M_0 in saturation mode for all operating time: this is the main mechanism isolating the delay cell from the VDD and substrate noise. The delay is defined by the RC constant of the load resistance implemented by the transistor pair (M_4/M_6 and M_3/M_5) and by the capacitors of the output nodes, which are the MOS capacitance of the transistors connected to the output nodes. A proper operation of the cell supposes that the load is resistive (quasilinear): in this case, the oscillation frequency does not depend on the supply voltage at the first order. A linear load is obtained by a special design of the transistor pairs M_4/M_6 and M_3/M_5 as proposed in [10], and explained in fig. 3a,b. The actual I-R characteristic of the load is provided in fig. 3c. Two

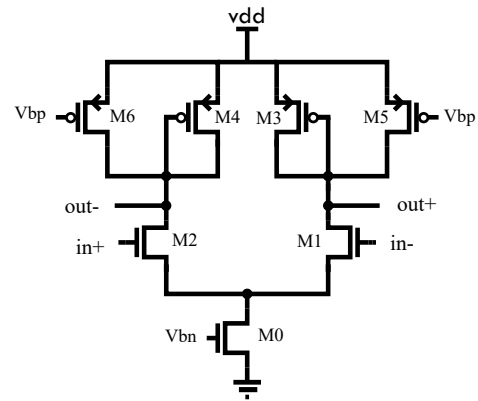


Fig. 2. Transistor schematic of the differential amplifier used as a delay cell in this study with the transistor size in Table I

TABLE I
TRANSISTOR SIZE AND BIAS VOLTAGE VALUE OF THE DIFFERENTIAL AMPLIFIER (DELAY CELL)

	Value
M0	14.4 μ / 250 n
M1/M2	5 μ / 120 n
M3/M4	7 μ / 80 n
M5/M6	4 μ / 80 n
Vbn	500 mV
Vbp	500 mV

bias circuits are required: the current source biasing (NMOS bias) and the load biasing (PMOS bias). In order to ensure the bias circuit convergence and stability, a starter transistor (not represented in the figure) is added to both bias circuit.

With the previous parameter, the output swing of the amplifier is over the range 0.6 to 1 V. The V_{gs} voltages of the transistors M_0 , M_5 and M_6 are generated by a quad generator as described in [11] (see. fig. 4). These circuits ensure a first-order independence of the generated voltages on the supply. To obtain the compatibility between the amplifier output range

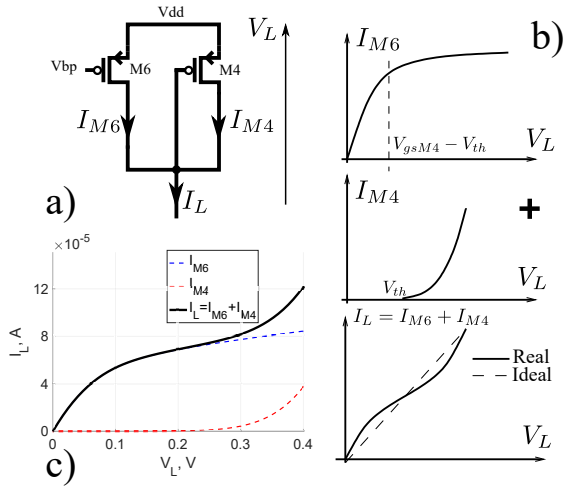


Fig. 3. Principle of linear load design in the differential delay cells: a) electrical schematic, b) operational principle, c) simulated characteristic of the implemented circuit.

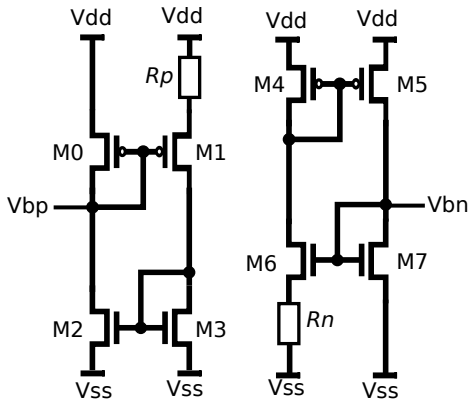


Fig. 4. PMOS (left) and NMOS (right) bias voltage generators for the differential delay cells.

TABLE II
TRANSISTOR SIZE OF PMOS AND NMOS BIAS CIRCUIT

PMOS (W/L)		NMOS (W/L)	
M0	10 μ /500n	M4	15 μ /3 μ
M1	50 μ /500n	M5	15 μ /3 μ
M2	13.65 μ /3 μ	M6	40.2 μ /500n
M3	14 μ /3 μ	M7	8.4 μ /500n
R _P	5 k Ω	R _N	3.8 k Ω

(400 mV) and classical digital stage voltage range (1 V), a comparator is added. The comparator architecture is based on the amplifier one to ensure a 50% duty cycle at the output.

The average power consumption of one amplifier is 105 μ W and is constant over all its frequency range due to the transistor M0 operating in saturation mode, and the current injected in the supply buses is close to be constant. This is very different from ring oscillators based on conventional CMOS inverters, where the supply buses are highly polluted by the switching currents of the delay cells.

In order to ease the layout design and reduce the parasitic

resistance and capacitance, the frequency control blocks FCB1 and FCB2 are integrated to their associated amplifier layout. The area of their layout is 8 μ m \times 12 μ m. The transistor size and characteristics of the differential amplifier are shown in Table II.

C. Frequency Control Blocks

There are several ways to alter the frequency in a ring DCO. The frequency control can be implemented via current modulation, modification of the output capacitance of the inverters with switches and MOS varactance [12] or only MOS varactance [13]. The latter approach has been chosen in this project. As explained previously, for the monotonicity of the transfer function, a hybrid binary/thermal control is chosen. The schematic view of these blocks FCB1 and FCB2 blocks is shown in Fig. 5(a) and Fig. 5(b).

The varactance are realized with low-VT PMOS transistor. The load MOS capacitance are directly connected between the output of the differential amplifiers and the digital control bits. This architecture has the advantages of removing the switches which bring extra capacitance and slow down the circuit. In the proposed architecture, the control bit c_0 to c_5 and b_6 to b_{13} are connected to the gate of the transistor. When the control bit are high, the transistor are blocked, providing a small capacitance at the output of the amplifier. On the other case, when the control bit are low, the PMOS transistors are in strong inversion thus providing a higher total capacitance, slowing down the oscillations and reducing the output frequency. One condition to ensure good oscillations is to keep the PMOS transistors in strong inversion on all the dynamic range of the amplifier. With a dynamic range of the amplifier being [600 mV- 1V] and by choosing low-VT transistor, this minimum value of 600 mV is enough to keep the transistor in strong inversion mode.

In order to achieve a high frequency resolution and minimizing the mismatch effect, an hybrid frequency control word (FCW) scheme is used with both incremental and binary control. As explained in the architecture description, this topology uses a binary code to control the six LSB (on FCB1) while the others four bits are controlled with a thermal code (FCB2). However the use of a binary-to-thermometer code block increases the area of the architecture. This choice represents a good trade off between the area and complexity of this digital block which generates the FCW.

III. RESULTS

This DCO was designed using a 28 nm CMOS technology and the supply voltage of the process is 1 V. All the results in this section are from post-extraction layout simulations. The layout of the DCO with the bias is shown in fig.6. The area of 1 DCO, the binary-to-thermal converter and the bias circuit (NMOS and PMOS) is 52 \times 108 μ m². The bias circuit is large but can be common to several DCO or ADPLL, thus reducing the effective area to each DCO.

The transfer function of the DCO for several power supply voltage values is shown in fig.7. With a typical power supply of V_{DD} = 1 V, the output frequency range of the DCO is

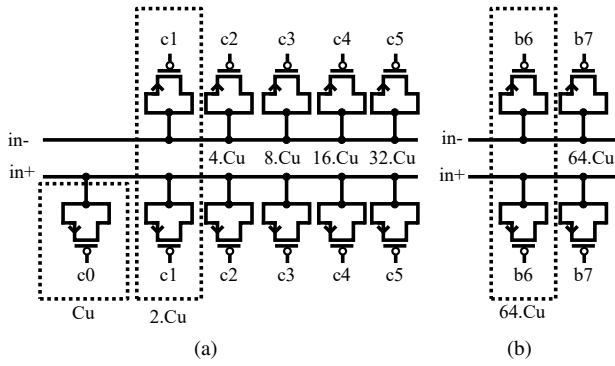


Fig. 5. Transistor schematic of the frequency control block (a) FCB1 (b) FCB2

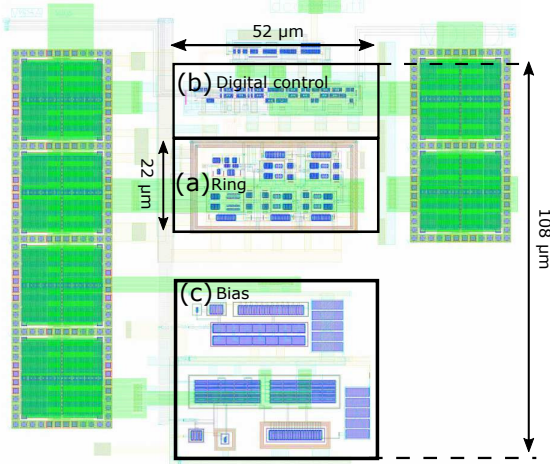


Fig. 6. Layout of (a) 5-stage differential ring oscillator with frequency control code, (b) binary to thermometer block and (c) NMOS and PMOS bias circuit

TABLE III
TABLE OF THE SYSTEM PERFORMANCE

Parameter	Value
Power supply	1 V
Ring Area	50 $\mu\text{m} \times 22 \mu\text{m}$
Digital Area	52 $\mu\text{m} \times 18 \mu\text{m}$
Frequency range	1.13- 1.54 GHz
Control code	576
Power (Ring)	660 μW
Power (bias)	81 μW
Power (FCW)	102 μW
RMS Jitter	2.3 ps

1.127-1.543 GHz, spread among 576 input codes, giving an average frequency step of 722 kHz. When the supply voltage increases to $V_{DD}=1.1$ V, the output frequency of the DCO increases of 55.6 MHz for the lower code (input code=80 in the figure), representing a rise less than 4% from the initial value. For an upper code of 480, there is a frequency rise of 38 MHz, representing also less than 4% of the DCO frequency. At the same time when the power supply drops

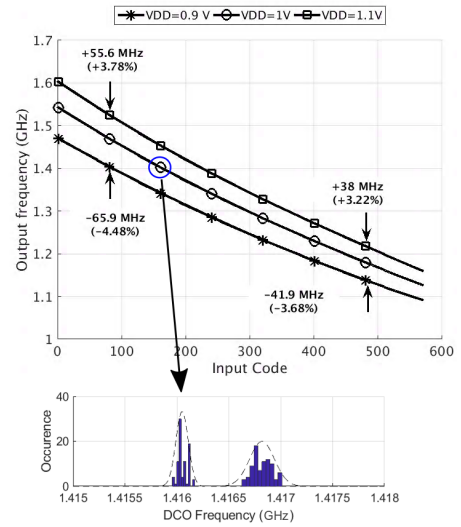


Fig. 7. Transfer function of the DCO for several voltage supply with a Monte Carlo simulation of 2 code with a variation of a LSB

to $V_{DD}=0.9$ V, variation from ideal case goes from -4.48% for the low input code to -3.68% for the upper input code. From these simulations, one can see that this circuit has low frequency variation with a frequency variation $<4.5\%$ for a 10% voltage supply variation. In order to make sure binary code do not overlap with process variation in FCB1, a Monte Carlo analysis of two codes with one LSB difference is also shown. In the same way, the design of FCB1 and FCB2 ensure a non overlapping between the binary and the thermal coding scheme

This insensitivity to power supply also stabilize over the frequency range the power consumption of this DCO. The inverter ring and the comparator consumes 660 μW , dominated by DC power consumption. The total power of both NMOS and PMOS bias circuit is 81 μW . Compared to analog core, the digital power consumption core changes with the frequency. The digital core includes the binary to thermal code, and a frequency divider, halving the ring frequency. The power consumption of this converter goes from 102 μW to 80 μW with respective ring frequency of 1.5 and 1.15 GHz.

To evaluate the influence of the different noise sources on the DCO performance, a periodic steady state (PSS) simulation is realized. In this simulation, the noise of each transistor is taken into account. Moreover, a non ideal power supply is also implemented, to modelized resistance and inductance from wire bonding. The influence of the power supply variation is also investigated. The results of these simulations is shown in fig.8. In this case, the system frequency is 1.31 GHz. One can see that the system is not affected by the power supply variation, induced by current peak, and the phase noise of this DCO achieves -74 dBc/Hz@1MHz. With these values, one can see that this DCO is not sensitive to the power supply, as long as the saturation mode is respected for the bias transistor. In the same way, the RMS jitter has been simulated with a PSS simulation and the period-to-period jitter is 2.3 ps.

The system performance of this DCO are shown in table III.

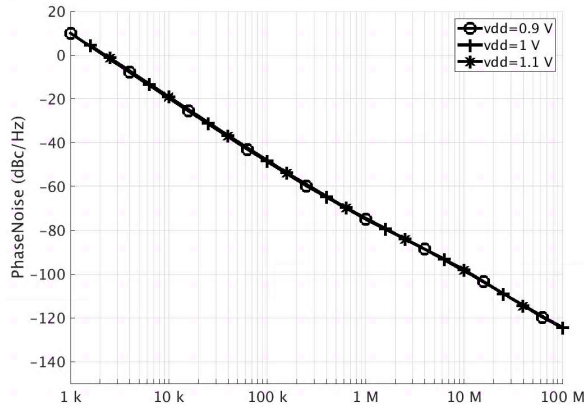


Fig. 8. Phase noise of a free-running DCO for several supply voltage

Without taking into account the voltage bias which can further be used for several ADPLL in a network, this work achieves a power consumption of $1.7 \mu\text{W}/\text{MHz}$ at the central frequency of 1.3 GHz. The Figure-of-Merit (FoM) of this system is $-135.5 \text{ dBc}/\text{Hz}$ at 1.3 GHz with a Phase Noise (PN) of $-74 \text{ dBc}/\text{Hz}$ at 1 MHz. This architecture achieves a good trade-off between higher power consumption and jitter DCO, and low power DCO with a smaller frequency range and higher noise.

TABLE IV
TABLE OF THE SYSTEM PERFORMANCE

	[14]	[15]	[16]	This work
Tech(nm)	45	65	65	28
Supply(V)	1.1	1.2	0.85	1
Freq.(GHz)	0.547-10.49	1.5-3.5	0.9-1.4	1.13-1.54
Resolution(bit)	-	8	13	9
Power(mW)	0.783^3	6	2.25	0.84
Area(μm^2)	170	156×92	90×210	108×52
PN (dBc/Hz)	-99.5^1 (@10MHz)	-	-96^2 (@1MHz)	-74^1 (@1MHz)
Jitter (ps)	-	1.6^1	-	2.3^1
FoM (dBc/Hz)	-145.9	-	-162	-135.5
FoM _T (dBc/Hz)	-207	-	-188	-163.2

$$\text{FoM (dBc/Hz)} = \mathcal{L}(\Delta f) - 20 \cdot \log_{10} \left(\frac{f_{\text{osc}}}{\Delta f} \right) - 10 \cdot \log_{10} \left(\frac{P_D}{1 \text{ mW}} \right)$$

$$\text{FoM}_T \text{ (dBc/Hz)} = \text{FoM} + 20 \cdot \log_{10} \left(\frac{FTR}{10} \right)$$

¹ Post-layout simulation

² Chip measurement

³ no DAC or frequency control implementation

IV. CONCLUSION

This work shows the design and the implementation of a 5-stage ring DCO in 28nm CMOS process. All the results from this paper are from post-extracted simulations. With the chosen number of stage and the binary/thermal frequency control, this DCO achieves a frequency range of 1.13-1.54 GHz. The frequency control has 576 codes, giving an average frequency step of 722 kHz. This small frequency step and range are possible by using transistors as capacitance without switches and also with the hybrid binary incremental control

scheme. This binary/thermal control also realized a excellent trade-off between the area of the capacitance and complexity of the circuit. This DCO achieves a phase noise of $-74 \text{ dBc}/\text{Hz}@1\text{MHz}$ or an equivalent of 2.2 ps. The maximal power consumption of this DCO at maximum frequency is $843 \mu\text{W}$, which is a low figure comparing to the state-of-the-art implementations with typical power of sub-milliwatts for the similar frequency range.

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