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# Monitoring of Gate Leakage Current on SiC Power MOSFETs: An Estimation Method for Smart Gate Drivers

Julien Weckbrodt , Nicolas Ginot , Christophe Batard , and Stephane Azzopardi

**Abstract**—Silicon Carbide (SiC) power transistors are more and more used in electric energy conversion systems. SiC power semiconductor devices, such as SiC metal-oxide-semiconductor field-effect transistor (MOSFET) can operate at higher frequency and higher temperature compared to Silicon power MOSFET or insulated-gate bipolar transistor. However, the maturity of the SiC technology is moderate compared to the well-known Silicon-based power semiconductor devices. Recent research works on reliability of SiC power MOSFET identified gate leakage currents as an ageing indicator. The monitoring of ageing indicators during normal operation may definitely help to predict damages and simplify the maintenance on the energy conversion systems. Due to the low amplitude of gate leakage currents, its direct measurement is difficult even under laboratory conditions and requires an offline characterization. This article presents a new method for estimating the gate leakage current using the gate drive circuit. The proposed method takes advantage of the internal structure of the typical gate drivers used to command SiC power MOSFETs.

**Index Terms**—Driver circuits, leakage currents, power system monitoring, semiconductor device reliability, silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistor (MOSFET), smart gate drivers.

$I_{L,DRIVER}$	Average leakage current due to the drive system.
$I_{L,DUT}$	Estimated gate leakage current.
$I_{L,MES}$	Average leakage current measured.
$I_{L,TH}$	Theoretical gate leakage current.
$m$	Modulation coefficient (PWM signal).
$R_{DS(on)}$	ON-state resistance.
Res	Targeted resolution (%).
$R_{GS}$	Gate-source resistance.
$T$	Switching period of the command signals.
$T_L$	Time required to reach $\Delta V_S$ (= acquisition time).
$T_{L,CAL}$	Time required to reach $\Delta V_S$ during calibration.
$T_{SINE}$	Period of the modulating signal.
$V_{DC}$	Power voltage source.
$V_{DD}$	Supply voltage of the gate driver.
$V_{GS}$	Gate-source voltage.
$V_S$	Source potential.
$V_{TH}$	Threshold voltage.
$\alpha$	Duty cycle of the command signal.
$\Delta V_S$	Authorized source potential variation.

## NOMENCLATURE

$C_1, C_2$	Decoupling capacitors.
$C_{GD}$	Miller capacitance.
$C_{GS}$	Gate-source capacitance.
$cpt$	Size of the counter (algorithm implementation).
$dt$	Temporal step for acquisition (in seconds).
$f$	Frequency of the modulating signal.
$I_D$	Online drain current.
$I_{DSS}$	Drain-source leakage current.
$I_{GSS}$	Gate-source leakage current (static measurement).
$I_{LOAD}$	Online load current.

## I. INTRODUCTION

THE very interesting electrical performances of silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) transistors make this component extremely promising for the future of power electronics in a wide range of applications. Indeed, the higher power density of SiC components and their characteristics under high temperature are appreciated for a compact design of power converters. Lots of works have been carried out for several years in order to highlight the limits in terms of lifespan as well as relevant ageing indicators. For example, power cycling, repetitive overcurrent, and repetitive short-circuit (SC) tests were applied to these components and their behavior until failure has been analyzed.

The channel resistance of a SiC MOSFET is considerably high compared to a silicon MOSFET. This is due to a lower inversion carrier mobility at the SiC/SiO<sub>2</sub> interface and electrons trapping resulting in the depletion of inversion charge density. In order to minimize the channel resistance, SiC MOSFETs are designed with a smaller gate oxide thickness compared to silicon ones. Due to a higher bandgap energy and a smaller oxide thickness, tunneling current through the gate oxide [1]–[4] and charge trapping in the gate oxide are reinforced [5], [6].

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Concerning ageing tests, the repetition of SCs is certainly the most severe one. The failure temperature was estimated at approximately  $650\text{ }^{\circ}\text{C} \pm 100\text{ }^{\circ}\text{C}$  near the aluminum metallization melting temperature [7]. As described in [8], two failure mechanisms have been pointed out during SC stress. The first failure mechanism is related to the increase of leakage current until the parasitic NPN transistor is turned on, leading to the destruction of the device. The second one is related to the degradation of: the gate oxide, source pads and the  $\text{SiO}_2/\text{SiC}$  interface. These degradations are linked to the extremely high temperature level reached during SC tests and can result in strong degradation or permanent damages. Some papers, including [8] also reveal that during SC tests, tunneling currents result in a transient gate leakage current that has never been observed with silicon power devices [2], [9], [10].

These peculiarities are also put forward to explain a particular turn-ON failure mode which has been shown on some particular devices or under particular electrical constraints during SC [9], [11]. Nevertheless, it seems that this failure mode results in a resistive SC between gate and source which can be explained by aluminum melting resulting in a path between gate and source as depicted in [12].

Ageing tests have been performed using repetitive SC cycles. Some of them start with a very low SC duration and the pulse length is regularly increased until failure. In the case of 1.2 kV devices, the results clearly show that irreversible damage appears. The drain saturation current decreases and the gate leakage current increases. The drain current evolution is not continuous which may indicate a cumulative physical degradation of the device. At the same time a permanent leakage current in reverse bias also increases gradually. In the case of 10 kV SiC MOSFETs, an increase of the on-state resistance ( $R_{\text{DS(on)}}$ ) was observed without significant degradation of the threshold voltage ( $V_{\text{TH}}$ ) or the gate-source leakage current ( $I_{\text{GSS}}$ ). Failure analysis shows that aluminum metallization layer has undergone a severe reconstruction leading to the appearance of large voids at the contact interface which explains the  $R_{\text{DS(on)}}$  evolution [12], [13]. Even if SiC MOSFETs are relatively robust to single pulse SC events up to about 50% of their nominal voltage rating [14], it has been highlighted that the device failure appears before  $10\text{ }\mu\text{s}$  which is the minimum duration a silicon insulated-gate bipolar transistor is able to sustain. It seems that the failure is related to the degradation of the gate structure due to the very high temperature reached during these tests. Other tests under repetitive SC conditions show different degradations leading to the increase of the threshold voltage and the gate-source leakage current. The gate structure is once again identified as the weakest point [14].

A similar analysis was done after overcurrent pulses [15]. The formation of a conductive path through the oxide yielding was observed leading to the inability to sustain drain-source voltage. It was concluded from experimental tests and simulation results that this failure mode is mainly caused by thermal issues due to the localized heat at the interface between the gate oxide and JFET region. After repetition of several SC events with high temperature variations, failure analysis has pointed out cracks around the oxide region of the degraded device but not in the

TABLE I  
SiC MOSFET—EXAMPLES OF COMMERCIALY AVAILABLE PRODUCTS

Type	Reference	Manufacturer	$I_{\text{GSS}}$ datasheet
1.2 kV / 12 A (TO-247)	SCT10N120	STmicroelec.	< 100 nA
1.2 kV / 25 A (TO-247)	LSIC1MO120E0080	Littlefuse	< 100 nA
1.2 kV / 40 A (TO-247)	SCH2080KE	Rohm Co.	< 100 nA
1.2 kV / 40 A (TO-247)	APT40SM120	Microsemi	< 100 nA
1.2 kV / 60 A (TO-247)	C2M0040120D	Cree Inc.	< 250 nA
1.2 kV / 180 A (module)	BSM180D12P3C007	Rohm Co.	< 500 nA
1.2 kV / 300 A (module)	CAS300M12BM2	Cree Inc.	< 100 nA

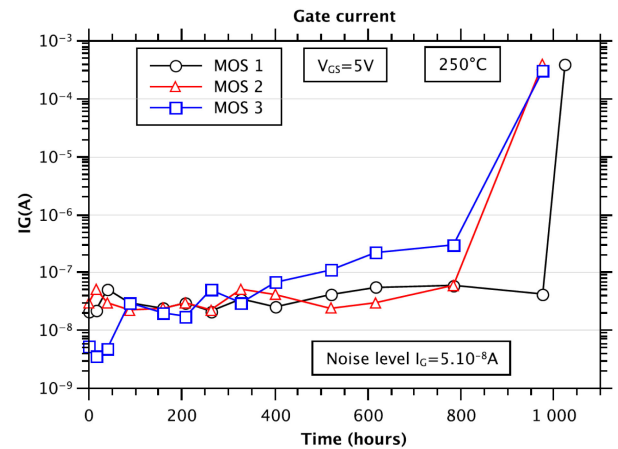


Fig. 1. Evolution of gate leakage current during an ageing test [20].

gate oxide itself even though gate oxide is often referred as the most sensitive part of the SiC MOSFETs [16], [17].

Other studies have pointed out that at relatively low stress (low bias voltage and short SC duration), when the effect of gate oxide degradation and metal reconstruction are eliminated, the ageing of the devices results in a  $V_{\text{TH}}$  decrease and an  $I_{\text{DSS}}$  increase due to the generation of holes in the oxide [5]. Authors show that the holes can be refilled with time and the degradation reversed when the device is placed under the ambient temperature of  $200\text{ }^{\circ}\text{C}$ . It has also been demonstrated that an injection of holes in the gate oxide is the dominant degradation mechanism during repetitive avalanche ageing, and also results in a  $V_{\text{TH}}$  decrease [6].

Power cycling leads to an on-state resistance increase due to the ageing of the die and the bond wires. It seems that accelerated ageing has a significant effect in the degradation of the bond wires due to overheating [18]. In [19], ageing tests within safe operating area were performed and authors have showed that  $R_{\text{DS(on)}}$  of SiC MOSFETs changes as the device ages, but they have pointed out that  $I_{\text{GSS}}$ ,  $I_{\text{DSS}}$ , and  $V_{\text{TH}}$  also evolve. The variations in  $I_{\text{DSS}}$ ,  $I_{\text{GSS}}$ , and  $V_{\text{TH}}$  indicate that the gate-oxide is the most affected area in SiC MOSFETs. Referring to the Table I, the  $I_{\text{GSS}}$  parameter is typically in the nA-range. In [19]–[21], the authors demonstrated a remarkable evolution of  $I_{\text{GSS}}$  value at the end of the lifetime of the SiC power devices (up to a few mA). An example of gate current leakage monitoring during ageing tests is provided in Fig. 1. Due to a strong evolution during the ageing process, the gate leakage current is proposed as a practical degradation signature for health monitoring aspects.

The  $I_{\text{GSS}}$  parameter represents the gate-source leakage current with the drain connected to the source. This nA-scale current

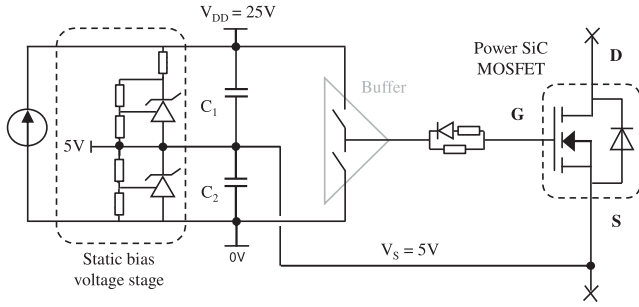


Fig. 2. Typical supply strategy for driving SiC power MOSFET.

is extremely low compared to the typical on-line drain current  $I_D$ .  $I_{GSS}$  is typically obtained by off-line measurement using a curve tracer or a fA-meter [19]. As a result, gate leakage current measurement during normal operation of the device under test (DUT) represents a real challenge. However, online monitoring of the gate leakage current could anticipate power converter failures. Studies have reported a method for online detection of the gate leakage current in SiC MOSFET [21]–[23]. This technique consists in measuring the gate resistance voltage using a differential amplifier to obtain the gate current. This circuit can be easily embedded in a gate driver but sub-mA currents cannot be measured by this method because of the low value of the gate resistance. In this article, an online method for gate leakage current estimation is presented. The proposed principle enables estimation of low leakage currents using a specific gate driver design.

Most of SiC MOSFET power modules require a +20 V/−5 V gate-source voltage for optimal switching, a single 25 V power supply is therefore used in gate drivers for driving SiC power MOSFET. A buffer is required in the gate driver to charge the gate-source capacitance  $C_{GS}$  and the Miller capacitance  $C_{GD}$  in order to switch the device as fast as possible. A command signal is applied on the buffer to drive the power component. In the design presented in Fig. 2, the peak currents are provided by capacitors  $C_1$  and  $C_2$ .

The average gate current is equal to zero in an ideal MOSFET due to the capacitive behavior of the gate-source interface. If the ground voltage (0 V) of the gate driver is chosen at the lowest potential of the drive circuit as shown in Fig. 2, the source voltage must be biased at 5 V by a static bias voltage stage. The 25 V power supply is generally obtained by an isolated dc–dc converter.

The proposed method is explained in the Section II. The implementation of the proposed method on a smart gate driver is presented in Section III. In Section IV, the experimental setup is described. Finally, experimental results are provided to demonstrate the feasibility of this new monitoring feature.

## II. THEORETICAL ANALYSIS OF THE PROPOSED METHOD

Since the direct measurement of gate leakage current is difficult for sub-mA values, an indirect method was investigated. The proposed method exploits the classical structure of gate drivers detailed in Fig. 2. The principle consists in disconnecting the

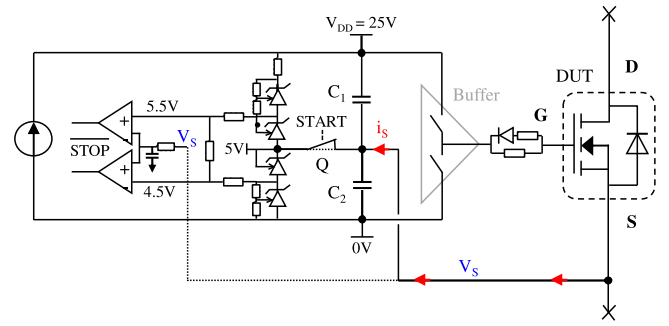


Fig. 3. Proposed integration method for gate leakage estimation.

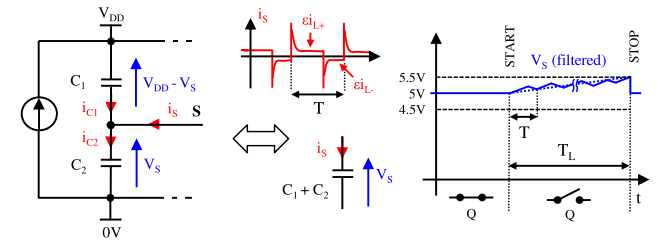


Fig. 4. Dynamic approach for gate leakage modeling.

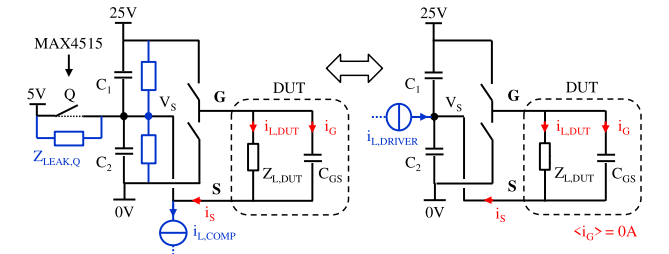


Fig. 5. Leakage currents on the gate driver.

static bias voltage stage from the capacitive bridge ( $C_1$ ,  $C_2$ ) during the estimation process. Meanwhile, the source potential variation is monitored to deduce the gate leakage current. As shown in Fig. 3, during the estimation process, the source potential variation is enabled within a range of  $\Delta V_S = \pm 0.5$  V around its bias voltage 5 V. The time  $T_L$  required to reach this positive or negative threshold is then used to deduce the gate leakage current value. The estimation process is therefore based on the integration of a low current over a long period of time  $T_L$ .

For the leakage current analysis, a dynamic approach is proposed in Fig. 4, that leads to

$$i_{C1}(t) = C_1 \frac{d(V_{DD} - V_S)}{dt} = -C_1 \frac{dV_S}{dt} \quad (1)$$

$$i_{C2}(t) = -C_2 \frac{dV_S}{dt} \quad (2)$$

$$i_S(t) = i_{C2}(t) - i_{C1}(t) = (C_1 + C_2) \frac{dV_S}{dt}. \quad (3)$$

The current  $i_S$  can be expressed as a function of the gate leakage current  $i_{L,DUT}$ . Regarding the model proposed in Fig. 5, the gate current  $i_G$  is defined as the current required to charge

the gate-source capacitance under normal switching conditions

$$i_S(t) = i_G(t) + i_{L,DUT}(t), \langle i_G \rangle = 0 \quad (4)$$

$$V_S = \frac{1}{C_1 + C_2} \int_0^{T_L} i_{L,DUT}(t) dt + V_S(t = 0). \quad (5)$$

The integration of (5) requires the modeling of the gate leakage current within the power semiconductor device. Considering a resistive model, the voltage variation after  $n$  period of the pulsewidth modulation (PWM) signal ( $T$ ) can be expressed as follows:

$$\Delta V_{S,n} = \frac{1}{C_1 + C_2} \left[ n \int_0^{\alpha T} \varepsilon i_{L+} dt + n \int_{\alpha T}^T \varepsilon i_{L-} dt \right] \quad (6)$$

$$\Delta V_{S,n=T_L/T} = \frac{n T}{C_1 + C_2} \underbrace{[\alpha \varepsilon i_{L+} + (1 - \alpha) \varepsilon i_{L-}]}_{\langle i_S \rangle} \quad (7)$$

where  $\varepsilon i_{L+}$  and  $\varepsilon i_{L-}$  are, respectively, the gate leakage currents during the turn-ON and the turn-OFF. As a result, after  $T_L = n T$ , the resulting average leakage current measured  $I_{L,MES}$  by the proposed method is obtained by using

$$\langle i_S \rangle = I_{L,MES} = I_{L,DRIVER} + I_{L,DUT} = (C_1 + C_2) \frac{\Delta V_S}{T_L} \quad (8)$$

where  $I_{L,DRIVER}$  is the parasitic average leakage current due to the gate drive system and  $I_{L,DUT}$  the gate leakage current of the DUT. For low leakage currents,  $T_L$  is typically very long compared to the switching period  $T$  of the PWM signal.

As described in Fig. 5, the resulting leakage current  $I_{L,MES}$  represents the total leakage currents seen by the source (S) including the leakages of the system  $I_{L,DRIVER}$  which itself includes leakages on the capacitors, the leakage current of  $Q$ , the input current of the comparator stage ( $i_{L,COMP}$ ). As a result, a calibration (CAL) must be performed in order to optimize the precision of the gate leakage estimation system. The leakage value obtained at the CAL is then used as a reference for the entire lifetime of the DUT. Obviously, the leakage currents of the system will also vary during this period, so the leakage value obtained by this method can only estimate the real gate leakage current value in order to detect an evolution during the lifetime.

The proposed method can be implemented as an off-line as well as an online monitoring feature. Offline measurement can be performed when the power converter is not powered. During  $T_L$ , if  $I_{L,DRIVER}$  is null, the source voltage increases when the DUT is turned-on ( $V_{GS,ON} = 20$  V) and decreases when the DUT is turned-OFF ( $V_{GS,OFF} = -5$  V). The source voltage variation can be explained by the charge/discharge of  $C_1 + C_2$  under constant leakage current, depending on the state of the DUT. For example, when the power transistor is switched on,  $C_1$  is discharged while  $C_2$  is charged due to a positive gate leakage current.

Although off-line measurement is interesting for a precise estimation of the gate leakage current, the most relevant application for the proposed method is online monitoring. In normal operation, the DUT can be driven by various types of signals corresponding to various applications. Considering a resistive behavior of the gate-source junction  $R_{GS}$ , the theoretical average

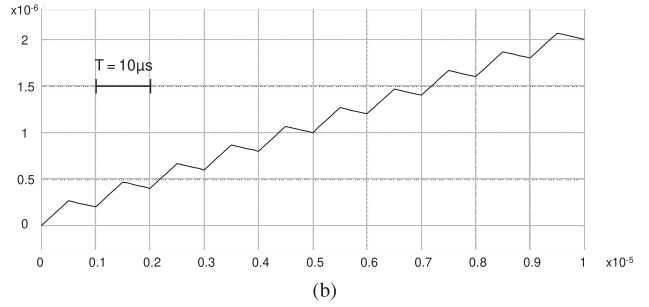
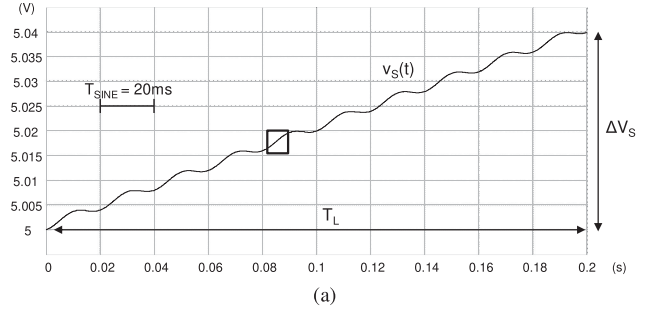


Fig. 6. Simulation of  $v_S(t)$  (a) and zoom at switching period scale (b) for a gate leakage current of 75 nA ( $R_{GS} = 1$  M $\Omega$ ) using a PWM command signal.

leakage current obtained by the proposed method is expressed as follows:

$$I_{L,TH} = \frac{1}{R_{GS}} (\alpha(t) \cdot (V_{GS,ON} - V_{GS,OFF}) + V_{GS,OFF}) \quad (9)$$

where  $\alpha(t)$  is the duty cycle of the gate-source voltage signal  $V_{GS}$  and  $V_{DD}$  is the supply voltage ( $V_{DD} = 25$  V).

Consequently, for  $\alpha = 20\%$ , the leakage currents are compensated during the switching period and the source voltage is stabilized at 5 V. For any other duty cycle value, a variation on the source voltage can be observed when there is a current leakage. For online monitoring, the efficiency of the proposed method depends on the application. However, in the case of a power inverter application, the duty cycle  $\alpha(t)$  is defined by

$$\alpha(t) = \frac{1 + m \cdot \cos(2\pi ft)}{2} \quad (10)$$

where  $m$  is the modulation coefficient and  $f$  the frequency of the modulating signal.

A simulation of the source voltage variation in power inverter mode is provided in Fig. 6. In this case, the average duty cycle is equal to 50% and the theoretical gate leakage current is defined as

$$I_{L,TH} = \frac{V_{GS,ON} + V_{GS,OFF}}{2 \cdot R_{GS}} = \frac{15}{2 \cdot R_{GS}}. \quad (11)$$

An offline characterization as well as an on-line estimation in a power inverter configuration can be realized using the circuit presented in Fig. 3. The proposed method is therefore particularly relevant for online monitoring considering a power inverter application. The major drawback of this method is the requirement of CAL.



TABLE II  
COMPARISON OF PROTECTION FEATURES IN GATE DRIVER BOARDS

Gate driver board	PT62SCMD17	CGD15HB62LP	CGD15HB62P1	This work
dv/dt immunity	50 kV/ $\mu$ s	100 kV/ $\mu$ s	50 kV/ $\mu$ s	> 125 kV/ $\mu$ s
Short-circuit detection	X	X	X	X
Soft Shut Down (SSD)	-	X	-	X
Under Voltage Lockout (UVLO)	X	X	X	X
$V_{DS(on)}$ monitoring	threshold detection	threshold detection	threshold detection	precise measurement
Gate leakage current estimation	-	-	-	X
Communication features across the galvanic isolation	-	-	-	X

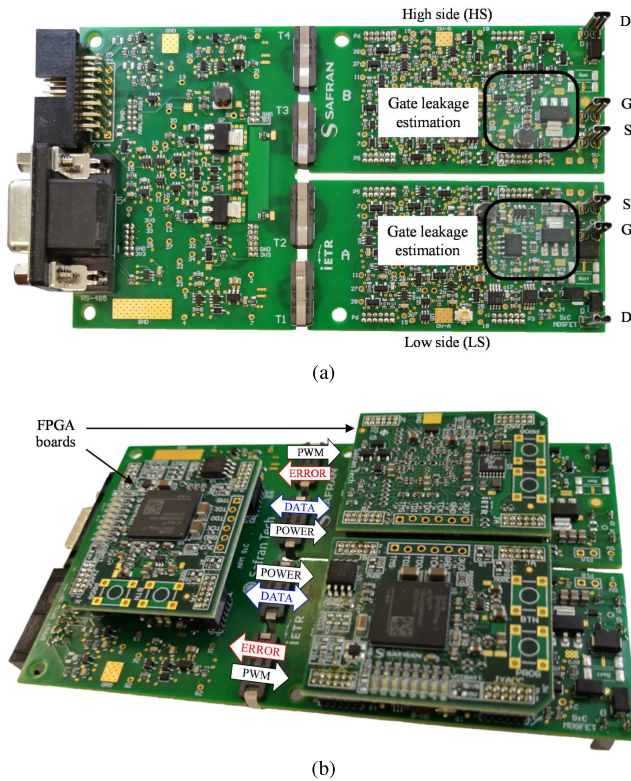


Fig. 10. Implementation in a smart driver board for health monitoring. (a) Top view. (b) Bottom view.

As shown in Fig. 9, the authorized source voltage variation was chosen at  $\Delta V = \pm 0.5$  V to ensure a  $V_{GS}$  signal between  $-5.5$  and  $+20.5$  V in the worst case. The threshold value must be chosen taking into account the targeted performances of the estimation process and the safety conditions for the  $V_{GS}$  signal.

### B. Proposed Solution Integrated in an Industrial Gate Driver

The proposed solution was also implemented in a smart driver board which integrates Spartan-7 FPGA boards on the primary and secondary circuits. As illustrated in Fig. 10, this board was specifically designed for health monitoring and integrates advanced monitoring features, such as the proposed estimating method,  $V_{DS(on)}$  measurement, communication features in addition to other conventional protection features (galvanic isolation, SC detection, soft shut-down...). Table II proposes a comparison between conventional gate driver boards and the board presented in Fig. 10. In this design, the FPGA are used for data management and leakage current calculation using (7).

The resources required by the calculation of the value of the gate leakage current depends on the targeted resolution. Indeed, if  $cpt$  is the counter size and  $dt$  is the temporal step of this counter (in seconds), the step in current in the worst case  $\Delta i_{L,min}$  can be expressed as follows:

$$\Delta i_{L,min} = 2 \cdot (C_1 + C_2) \cdot \frac{|\Delta V_S|}{T_{L,max}} = 2 \cdot (C_1 + C_2) \cdot \frac{|\Delta V_S|}{cpt \cdot dt} \quad (12)$$

Equation (12) is a consequence of the behavior of the voltage variation which can be positive or negative. Consequently, the worst case corresponds to the current value which cancel the (7). In this case, the voltage derivation  $\Delta V_S$  is theoretically equal to zero and  $T_L$  is infinite. In practice, the acquisition time is limited, the counter size and the step time are then defined to meet the targeted resolution. Equations (13) and (14) can be used to define these two parameters

$$dt = (C_1 + C_2) \cdot \frac{|\Delta V_S|}{i_{L,max}} \cdot \frac{Res}{1 + Res} \quad (13)$$

$$cpt = \frac{i_{L,max}}{i_{L,min}} \cdot \frac{1 + Res}{1 - Res} \cdot \frac{1}{Res} \quad (14)$$

where Res is the targeted resolution (%).

The proposed circuit requires a small number of components as this method requires no Adc converter for acquisition, the high logic level duration of the STOP signal is used to calculate the leakage current. However, the integration of FPGA is not mandatory for the proposed method since the duration of the measurement can be directly compared to the CAL one. The design of this board will not be more detailed in the present article since communication features and data management are not necessary to demonstrate the principle of gate leakage current estimation.

The board was also tested in a power inverter configuration using an inductance of  $700 \mu$ H as described in Figs. 11 and 12. The gate driver board was tested during operation at 47 kVAR under  $V_{DC} = 540$  V using a 100 kHz PWM signal with a modulation coefficient of 90%.

Since the hypothesis of a resistive gate-source junction during the ageing was confirmed, the same measurement protocol was used to test the proposed circuit on a power SiC MOSFET module (DUT: CAS300M12BM2). Additional gate-source resistances were used to emulate a gate leakage current during operation in power environment since it is impossible to control precisely the leakage currents of the DUT.

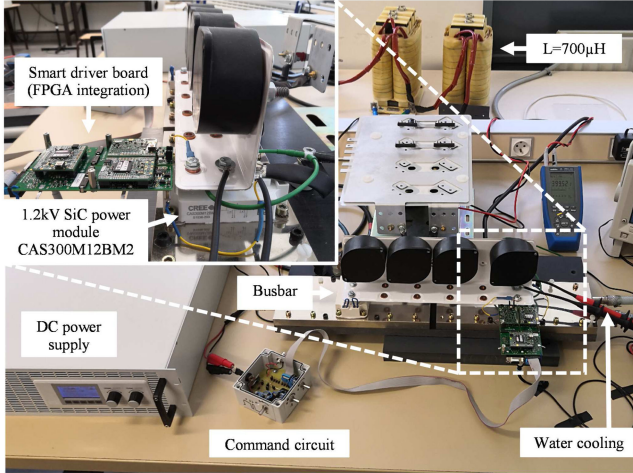


Fig. 11. Validation on a power SiC module (CAS300M12BM2).

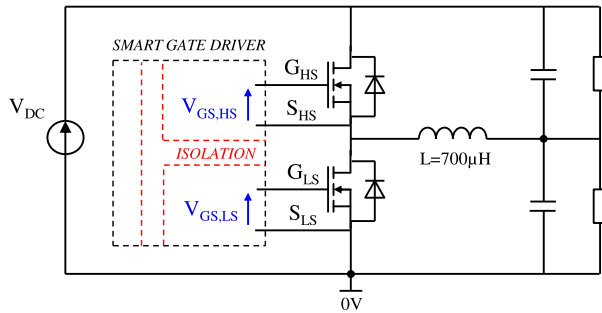


Fig. 12. Power inverter with capacitive midpoint.

## IV. RESULTS

### A. Gate Leakage Current Emulation Using an External $R_{GS}$

A CAL has been performed with a 1.2 kV power SiC MOSFET (C2M0040120), a component which has never been used in a power converter before. As  $I_{GSS}$  is typically in the fA-range for “new” components, the source voltage variation observed at the CAL is mainly due to the leakages of the system  $I_{L,DRIVER}$ . As shown in Fig. 9, the source voltage decreases during  $T_{L,CAL} = 45.5$  s corresponding to  $I_{L,DRIVER} = -413$  nA on the test circuit. About 20 trials were performed in order to check the repeatability for the CAL:  $43$  s  $< T_{L,CAL} < 46.2$  s was observed, corresponding to a leakage current between  $-437$  and  $-407$  nA so the precision of the proposed method is maximum 30 nA at low current. The  $I_{L,DRIVER}$  value is different from a circuit to another depending on the parasitic elements of the components used. A CAL at “new” state is therefore required to reach the minimal detection limit of 30 nA.

As explained in Section IV, external gate-source resistances  $R_{GS}$  were added to reproduce the ageing of the DUT. The leakage currents values corresponding to the waveforms given in Fig. 9 are summed up in Table III. For example, the addition of a 150 M $\Omega$  gate-source resistance corresponds to a theoretical gate leakage current of  $I_{L,TH} = 50$  nA. The experimental results show a negative variation during 53 s which corresponds to  $I_{L,DUT} = 58$  nA after subtraction of the calibrated value. In

TABLE III  
RESULTS CORRESPONDING TO THE WAVEFORMS

$R_{GS}$ added ( $\Omega$ )	Introduced $I_L$	$T_L$ ( $\Delta V_S$ +/-)	$I_{L,MES} = I_{L,DRIVER} + I_{L,DUT}$	Estimated $I_{L,DUT}$
CAL ( $R_{GS} \rightarrow \infty$ )	0 nA	45.5s (-)	-413 nA	0 nA
150 M $\Omega$	50 nA	53 s (-)	-355 nA	58 nA
50 M $\Omega$	150 nA	82.3 s (-)	-229 nA	184 nA
10.35 M $\Omega$	725 nA	54.8 s (+)	+345 nA	758 nA
7.14 M $\Omega$	1.05 $\mu$ A	25.8 s (+)	+729 nA	1.14 $\mu$ A
3.26 M $\Omega$	2.3 $\mu$ A	8.6 s (+)	+2.19 $\mu$ A	2.6 $\mu$ A
“aged” device (no extra $R_{GS}$ )	2 mA*	11.88 ms (+)	+1.58 mA	1.58 mA

\* $I_{GSS} = 2$  mA measured using ammeter ( $V_{GS} = 20$  V); waveform in Fig. 14.

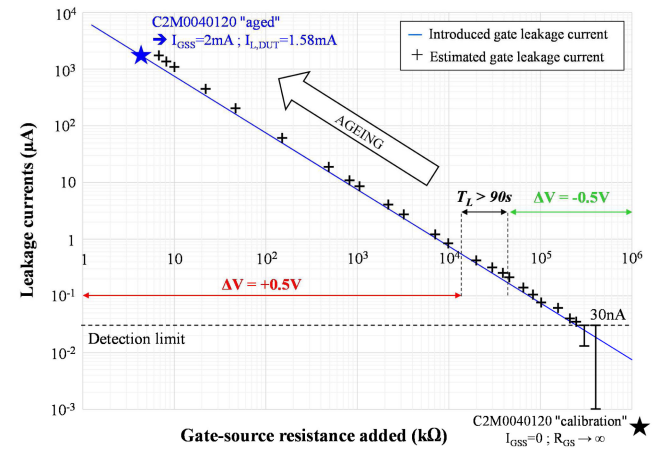


Fig. 13. Hypothesis validation using the gate leakage estimation circuit at 25 °C (online monitoring).

the case of an gate leakage current of 1.05  $\mu$ A, a positive variation was observed during 25.8 s which corresponds to  $I_{L,DUT} = 1.14$   $\mu$ A.

Results provided in Fig. 13 show the relevance of the proposed method. With the proposed circuit, a gate leakage current as low as 50 nA was clearly identified. However, the source potential variation can be positive or negative which means that for a particular gate leakage current value, the acquisition time is too long ( $T_L > 90$  s). In the investigated case, gate leakage currents between 200 and 500 nA cannot be automatically estimated using the presented method. In Fig. 13, the corresponding points where obtained by measuring the  $\Delta V_S$  value after 90 s. This problem can be solved by adding a positive leakage current to the system in order to have a positive variation during the CAL.

In this case, the source potential variation would be positive at any time ( $\Delta V_S = 0.5$  V) and the acquisition time should be chosen ( $T_{L,CAL} < 90$  s) so that the gate leakage current could only result in a shorter acquisition time.

### B. Validation of Hypothesis Using an “Aged” Component

The estimated value is related to the  $I_{GSS}$  value but the gate leakage current obtained by this method is different as the measurement is realized under different conditions. A static measurement is required for  $I_{GSS}$  characterization, whereas an on-line monitoring was performed in order to estimate the gate leakage current evolution.



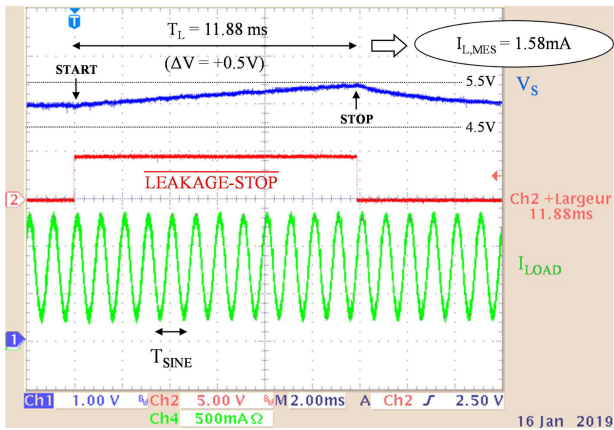


Fig. 14. Source voltage variation with the “aged” device (C2M0040120).

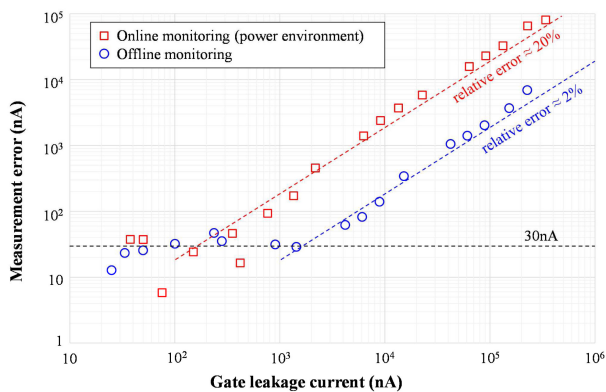


Fig. 15. Comparison between offline and online monitoring at 25 °C using the proposed method (DUT: CAS300M12BM2).

As mentioned in Section III, an “aged” device (C2M0040120) was also tested to validate the hypothesis of a resistive behavior of the gate-source junction for “aged” devices. The component used was precisely characterized before the estimation process:  $I_{GSS} = 2$  mA was measured on this device using a fA-meter ( $V_{GSS} = 20$  V). A gate leakage current of 1.58 mA was found with the proposed estimation method. The associated waveform are presented in Fig. 14.

In this case, the source potential variation is positive and the acquisition time is very short ( $T_L = 11.88$  ms) compared to the CAL time  $T_{L,CAL}$ . The measurement error is about 20% but the targeted application is health monitoring of power semiconductors so only the gate leakage current variation from the calibrated value is monitored. For example, a first warning threshold could be set at 1  $\mu$ A, then, a critical threshold could be set at 10  $\mu$ A. These values are chosen considering the DUT endurance tests. A precise measurement of the real value is not the objective of this article.

### C. Temperature and Precision Considerations

The measurements presented in Fig. 15 confirmed a detection limit about 30 nA and a relative error of 20% for the online monitoring mode. The offline measurement using the same method is more accurate than the online characterization as a relative error of 2% can be reached.

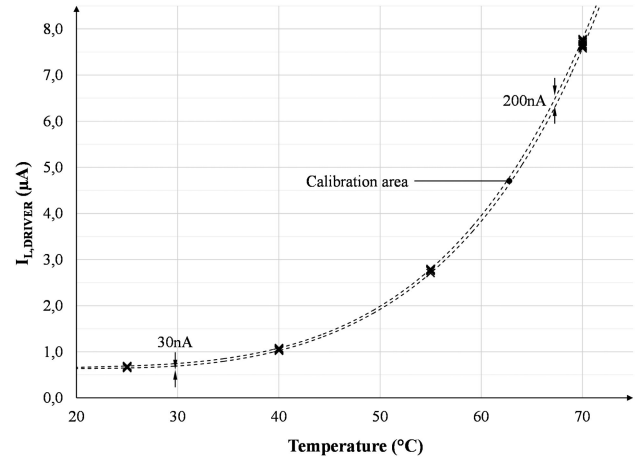


Fig. 16. Leakage current due to the measurement circuit versus temperature (CAL on the smart driver board).

In Fig. 16, the reproducibility of the CAL was tested under different temperatures to highlight the behavior of the parasitic leakages due to the circuit under temperature. The first limitation of this approach is therefore the behavior of the circuit leakages under temperature. The sensitivity of the measurement circuit to temperature is probably mainly due to the choice of the capacitors  $C_1$  and  $C_2$  (Ref: GRM21BR61H475KE51L) which were used to increase the density of integration in the board presented in Fig. 7. The choice of class I capacitors (ex: C0G) would be better for this circuit. A table of CAL under different temperatures can solve this issue at the price of the integration of a temperature sensor and a more complex CAL process. For each temperature, ten measurements were performed demonstrating once again a minimal precision of 30 nA.

Since the leakage current of the circuit depend on the leakages of each component, the  $I_{L,DRIVER}$  value is not reproducible from a design to another, the calibrated value is valid only in a given board. Another limitation is the ageing of the components used for the estimation circuit itself, such as the capacitors  $C_1$  and  $C_2$ .

## V. CONCLUSION

The gate leakage current is considered as a pertinent ageing indicator for SiC power MOSFET due to the thickness of the gate oxide and the larger bandgap of these transistors. This parameter is typically less than 100 nA in undamaged components, but it can rise until several  $\mu$ A or mA at the end of the lifetime of the device. Direct measurement of this sensitive parameter is impossible during normal operation because of the working environment and the low value of the leakage currents. A gate leakage estimation using an integration method has been proposed using a smart gate driver. The results demonstrated the ability to identify gate leakage currents as low as 50 nA from their calibrated value. The estimated value does not correspond to a precise measurement of  $I_{GSS}$  due to approximations but the proposed method can provide an estimation of the gate leakage currents during operation. The proposed method need to be tested directly in an accelerated ageing protocol to confirm the ability to detect an ageing on SiC devices. An attention has to be

accorded to the choice of the measurement circuit components and their behavior under temperature. The proposed circuit can be easily embedded in a gate driver for an online monitoring application. As a result, the proposed solution offers new perspectives for health monitoring aspects in power electronics.

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